

DISCRETE AND INTEGRATED ELECTRONICS

VOLUME ONE



ANALYSIS AND DESIGN
FOR
ENGINEERS AND ENGINEERING TECHNOLOGISTS

STEPHEN R. FLEEMAN

DISCRETE AND INTEGRATED ELECTRONICS

VOLUME ONE

**ANALYSIS AND DESIGN
FOR
ENGINEERS AND ENGINEERING TECHNOLOGISTS**

STEPHEN R. FLEEMAN
Associate Professor and Electrical Engineer Emeritus

Cover Design: Douglas M. Decker

Cover Photograph: Umberto on Unsplash

Copyright © 2019 by Stephen R. Fleeman

CONTENTS

Preface vii

Volume One

1 Solid-State Physics and the P-N Junction 1

1-0	Study Objectives	2
1-1	Why Study Solid-State Physics?	2
1-2	The Atom and Electrical Conductors	4
1-3	Semiconductors	11
1-4	Semiconductor Crystals and Covalent Bonding	13
1-5	Conduction in Pure (Intrinsic) Semiconductor Crystals	15
1-6	Doped Semiconductors	19
1-7	Organic Semiconductors	22
1-8	The P-N Junction	27
1-9	The Forward-Biased P-N Junction	35
1-10	The Reverse-Biased P-N Junction	39
1-11	The Diode	44
	Problems for Chapter 1	45

2 Diodes and Circuit Analysis 51

2-0	Study Objectives	51
2-1	The Diode V-I Characteristic Curve	52
2-2	The Shockley Diode Equation and the DC Load Line	66
2-3	The Ideal Diode Model	70
2-4	The Knee-Voltage Diode Model	72
2-5	The Reverse Current Source Diode Model	77
2-6	Zener and Avalanche Diodes	77
2-7	The Ideal Zener Diode Model	81
2-8	Static and Dynamic Resistance	83
2-9	The Zener Dynamic-Resistance Diode Model	86
2-10	Using Thevenin's Theorem	92
	Problems for Chapter 2	98

3 Diode Applications and Additional Devices 104

3-0	Study Objectives	104
3-1	Diode Clippers and Limiters	105
3-2	Diode Clamper Circuits	109
3-3	Temperature Effects on P-N Junction Operation	113
3-4	NTC and PTC Thermistors	119
3-5	Varistors	125
3-6	Light-Emitting and Laser Diodes	127
3-7	Photoconductive Cells, Photodiodes, and Solar Cells	137
3-8	Frequency Effects on P-N Junction Operation	150
3-9	The Schottky Diode	154
3-10	The Varactor Diode	156
	Problems for Chapter 3	157

4 DC Power Supplies: Rectification and Filtering 170

4-0	Study Objectives	171
4-1	Linear Versus Switching DC Power Supplies	171
4-2	The Load	173
4-3	The Single-Phase AC Power Distribution System	175
4-4	Average and RMS Values	177
4-5	The Transformer	186
4-6	The Half-Wave Rectifier	192
4-7	Full-Wave Rectifiers Using a Center-Tapped Transformer	202
4-8	Full-Wave Bridge Rectifiers	207
4-9	Dual-Complementary Full-Wave Rectifiers	213
4-10	Filter Capacitor Considerations	215
4-11	Simple Capacitor Filters	218
4-12	Ripple Factor	221
4-13	Light-Loading Constraint	223
4-14	Ripple Voltage Equation	224
4-15	Rectifier Average and Peak Repetitive Currents	229
4-16	Nonrepetitive Diode Surge Current	235
4-17	Capacitor Ripple Current	238
4-18	Transformer Secondary Current	241
4-19	Diode Rectifier Specifications	243
4-20	Three-Terminal IC Voltage Regulators	248
	Problems for Chapter 4	250

5 Bipolar Junction Transistors 269

- 5-0 Study Objectives 270
- 5-1 The Basic BJT Structure 270
- 5-2 Unbiased Transistors 271
- 5-3 BJT Operation 273
- 5-4 BJT Connections and Current Gain 279
- 5-5 Leakage Currents 283
- 5-6 The Transistor Convention 286
- 5-7 V-I Curves 287
- 5-8 Finding the Q-point 298
- 5-9 The BJT Amplifier 306
- 5-10 The Transistor Switch 311
- 5-11 The Clapper 313
- Problems for Chapter 5 323

6 Field-Effect Transistors 332

- 6-0 Study Objectives 332
- 6-1 The JFET Structure 333
- 6-2 Operation of the JFET 336
- 6-3 FET Configurations and V-I Curves 346
- 6-4 The FET Transfer Equation 354
- 6-5 The Depletion-Enhancement MOSFET 356
- 6-6 Enhancement MOSFETs 361
- 6-7 Finding the Q-point 365
- 6-8 The FET Signal Process and Applying Superposition 371
- 6-9 CMOS – The Logical Choice for Linear 376
- 6-10 MOSFET Latching Circuit 380
- 6-11 Insulated Gate Bipolar Transistor (IGBT) 384
- Problems for Chapter 6 385

Answers to Selected Odd-Numbered Problems 392

Index for Volume One 400

Volume Two

- 7 BJT and FET Biasing**
- 8 Voltage Amplifier Models**
- 9 Inverting Voltage Amplifiers**
- 10 Non-Inverting Voltage Amplifiers**
- 11 Differential and Cascaded Amplifiers**
- 12 Frequency Response**
- Answers to Selected Odd-Numbered Problems**
- Index for Volume Two**

Volume Three

- 13 Op Amp Negative Feedback**
- 14 Additional Op Amp Amplifier Circuits**
- 15 Introduction to Power Amplifiers**
- 16 Oscillators**
- 17 AC Power Control**
- 18 DC Power Supplies: Regulation and Protection**
- Answers to Selected Odd-Numbered Problems**
- Index for Volume Three**
- Master Index for Volumes One - Three**

Preface

Who Should Read this Book?

Discrete and Integrated Electronics was written to help anyone who is interested in learning the basic concepts in electronics which lead to the analysis and design of electronic circuits. This includes:

- Electrical and Electronic Engineering Technology students pursuing a degree or certificate.
- Electrical Engineering students who desire to understand the applications underpinning the topics and mathematics found in their studies.
- Mechanical Engineering students struggling to understand the relevance of their required course in engineering circuit analysis.

In general, it can be used in an instructor-led course, an on-line course, or for self-study. The reader should have completed a basic course in DC circuit analysis. Completion or enrollment in an AC circuit analysis class is recommended, but **not** required. Basic algebra is used with a hint of plane trigonometry.

What Features are Included?

- Objectives at the beginning of each chapter to help you guide your studies.
- Illustrations to help you grasp every concept.

- Narrated examples to help you understand the *whys* and not just the *hows*.
- Step-by-step screen captures that illustrate the use of National Instruments (NI) Multisim to verify concepts and approximations incorporated in the textbook.
- Latest technology like organic semiconductors and the OLEDs (Organic Light Emitting Diodes) employed in televisions and displays.
- Practical examples like operation and *design* of a DC power supply.

Why is *Discrete and Integrated Electronics* a Kindle eBook?

- The advantages offered by eBooks include *lower cost* when compared to traditional printed textbooks.
- eBooks provide greater portability when contrasted with the effort required to lug traditional textbooks around.
- Nearly zero chance you will lose your textbook. This covers its misplacement or theft.
- Amazon provides a *free* Kindle application for personal computers.
- Kindle eBooks are also compatible with iPads, Android tablets, and smart phones.
- eBooks provide compatibility with instructor-led, on-line, and distance education course formats.

- Natural resources are preserved since printing, storage, and distribution of traditional textbooks are eliminated by digital eBooks.

What is “NI Multisim”?

Multisim is a computer program that allows you to enter an electrical schematic graphically. It is a widely-used circuit simulation program. It is popular in both industry and academia. Studica (www.studica.com) provides a student-version of Multisim for under \$50 USD.

Who or What is a “Stephen R. Fleeman”?

Now retired, Professor Fleeman was an educator and electrical engineer. He has 39 years of teaching at the university and college level while working concurrently as an electrical engineer at an aerospace company for 31 years. He wrote this textbook to combine that teaching experience and practical engineering savvy.

Dedication

I am thankful for the engineering experiences provided by Hamilton Sundstrand, Precision Governors, and Kaney Aerospace. I delighted in my teaching experiences at Rock Valley College and Purdue University.

I am grateful for my faculty colleagues at Rock Valley College: Professor Linden Griesbach (always willing to examine my mathematical derivations and make suggestions), Professor Joe Etminan (always eager to help in anyway needed) and Dr. Tom Lombardo (always available to offer suggestions to help me make my teaching more effective).

Family support is an immeasurable help to achieving one’s goals. I owe a debt of thanks to my three sons Kirt, Brennan, and Blake.

Kirt is a man purely comfortable in his own skin. Brennan is an accomplished electrical engineer in his own right. Blake is a gifted physician and healer. They each make very proud.

Most importantly, I thank my beautiful wife Claudia who supports me in every endeavor. Beyond being my wife and helpmate, she is an artist, author, and engineer. She is a lady who can handle a chain saw, pour concrete, design and construct furniture, and grow and nurture mystical gardens and yards. Beyond those incredible talents, she also provides our family with artisan dinners.

Stephen R. Fleeman

1

Solid-State Physics and the P - N Junction

Electrons serve as the energy-conveying medium in electrical and electronic circuits. We encounter the term “electronics” quite regularly. Let’s give it a definition. Electronics is a branch of physics that deals with the emission, the behavior, and the effects associated with the movement of electrons through a vacuum, gas, an electrical conductor, or a semiconductor. Electron movement through electrical conductors is important in both electrical and electronic circuits. Electron movement through a vacuum (or a gas) is less important in the study of *modern electronic devices*.¹ Our focus in this chapter is to obtain an understanding of the charge carrier movement through semiconductor materials. The p - n junction is also introduced. The p - n junction is fundamental to the operation of virtually all electronic devices (such as diodes, transistors, and both analog and digital integrated circuits). Frankly, our desire is to achieve a basic understanding and avoid much of the mathematics that underlies semiconductor physics. This chapter covers the following topics:

- Why Study Solid-State Physics?
- The Atom and Electrical Conductors
- Semiconductors
- Semiconductor Crystals and Covalent Bonding
- Conduction in Semiconductor Crystals
- Doped Semiconductors
- Organic Semiconductors
- The P - N Junction
- The Forward-Biased P - N Junction
- The Reverse-Biased P - N Junction
- The Diode

¹ The dawn of modern electronics used vacuum tubes extensively. The operation of vacuum tubes, including the cathode ray tube (CRT), television picture tubes and computer monitors relied on electron movement through a vacuum. These devices are no longer in mass production.

1-0 Study Objectives

After completing this chapter, you should be able to:

- Name the eight (8) sources of energy.
- Define the term *transducer*.
- Explain the difference between positive and negative ions.
- Describe metallic bonding.
- Relate an electron's orbital radius to its energy level.
- Explain the creation of energy bands and define the valence- and conduction-energy bands.
- Define the electron volt (eV).
- Distinguish between the energy diagrams for conductors, semiconductors, and insulators.
- Explain the meaning of the term *bandgap*.
- Define the terms trivalent, tetravalent, and pentavalent.
- Explain covalent and ionic bonding.
- Describe the generation of holes and free electrons in a pure semiconductor.
- Describe hole movement.
- Explain the characteristics and the uses of donor and acceptor impurities.
- Explain the differences between *p*- and *n*-type semiconductors.
- Name the majority and minority carriers in *p*- and *n*-type semiconductors.
- Explain the meaning of “organic electronics” and its advantages.
- Describe the formation of the *p-n* junction including the depletion region and its associated barrier potential.
- Explain the differences between forward and reverse bias of a *p-n* junction.
- Distinguish between reverse saturation current and surface leakage current.
- Describe the diode.

1-1 Why Study Solid-State Physics?

Without a basic knowledge of semiconductor physics, we are doomed to view electronic devices as being somewhat mystical in nature. To understand their operation, characteristics, and foibles², we need to understand how charge carriers move through them.

Solid-state devices are electronic circuit components that are constructed from (solid) crystals.

The crystalline materials used to make the various solid-state devices are called ***semiconductors***. Semiconductors have unique electrical properties. When conductors and insulators are exposed to various forms of energy, their electrical properties do not change significantly. However, the electrical characteristics of semiconductors are strongly influenced by various energy sources.

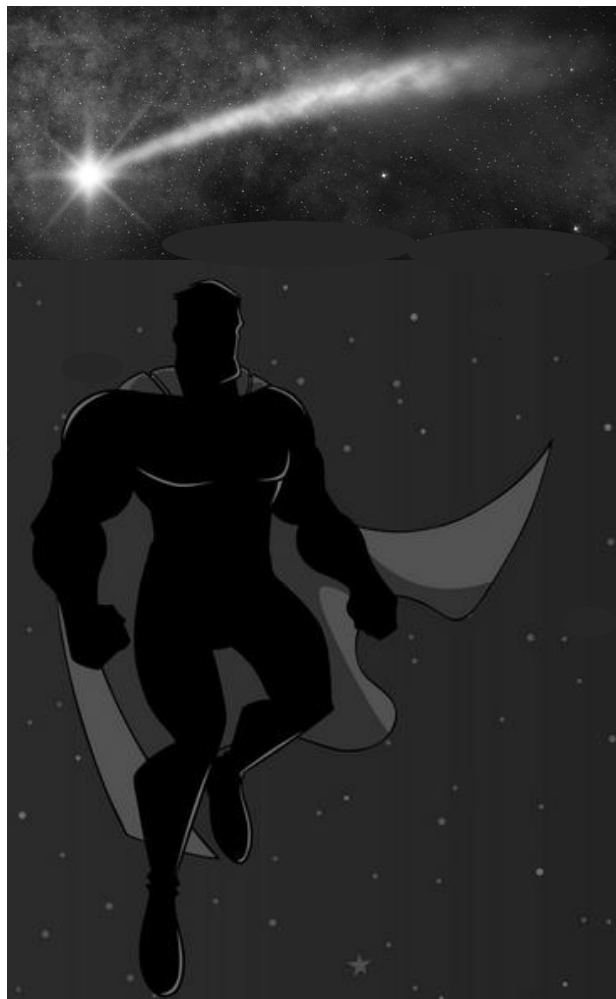
²To spare the reader the effort of using a search engine to look up this word or simply ignoring it, its definition is provided here.

A foible is a minor flaw or a shortcoming in character. Before the end of academic terms, most students have either identified or magnified foibles that describe their professor.

The sources of potential and kinetic energy are Chemical, Optical, Mechanical, Electrical, Thermal, Magnetic and Nuclear and can be remembered by using the mnemonic aid COMETMAN given in Fig. 1-1.

Optical energy is also called light energy. Thermal energy is the same as heat energy. Nuclear energy is synonymous with atomic energy. There are interrelations between these kinds of energy sources. For example, acoustical (sound) energy is also related to mechanical energy. COMETMAN helps us to remember the fundamental sources.

COMETMAN



Sources of
potential and
kinetic energy:

Chemical
Optical
Mechanical
Electrical
Thermal
Magnetic
Acoustical
Nuclear

Figure 1-1. COMETMAN

*A transducer is a device that converts one form of energy into another*³. Because semiconductors are sensitive to light, they can be used to make photoconductive cells (whose resistance decreases as the light intensity increases) and photodiodes. These transducers are used in light-detection and -measurement equipment. Varistors and zener diodes are devices whose resistance decreases dramatically if the voltage across them exceeds their breakdown voltage rating. (In fact, a varistor is sometimes referred to as a voltage-dependent resistor or VDR.)

Thermistors are used as transducers in temperature-measurement systems. Hall-effect devices convert changes in magnetic flux strength into resistance changes. Hall-effect devices are used in current-monitoring oscilloscope probes, proximity detection schemes, and as position/speed sensors to control the brushless DC motors found in computer hard disk drives.

To understand these and other solid-state devices, we need to have a basic understanding of the nature of semiconductors. This will not only help us understand the devices available currently, but also the new ones that are under development.

1-2 The Atom and Electrical Conductors

The smallest part of an element that retains the specific properties of that element is an *atom*. A simple model of the atom (proposed by Danish physicist Niels Bohr) depicts the atom with a central nucleus containing (no electrical charge) neutrons and positively charged protons. Extremely small negative electrons are arranged in orbits about the nucleus. The *magnitude* of the electrical charge of an electron is equal to the positive charge possessed by a proton. Therefore, *an atom with an equal number of protons and electrons has no net electrical charge*. If an atom loses an electron, it has a net positive charge. The atom is then called a *positive ion*. Conversely, if an atom gains an electron, it has a net negative charge and becomes a *negative ion*.

Copper is a good electrical conductor. The reason why copper is such a good electrical conductor becomes clear when we examine its atomic structure. In Fig. 1-2, we see the nucleus (center) of the copper atom contains 29 positively charged protons. (We shall ignore the neutrons since they do not contribute to the primary charge characteristics of an atom.) When copper is electrically neutral it has 29 negatively charged electrons orbiting its nucleus. The number of outermost orbiting electrons is called the *valence* of an atom. Copper has a valence of one (1). The chemical symbol for copper is *Cu*.

³ Two broad categories of transducers exist called *active* and *passive*. Active transducers convert one energy input into a different energy output. For example, a light-emitting diode (LED) is an active transducer because it converts its electrical energy input into an optical energy output. However, a photoconductive cell is a passive transducer since it converts light energy into an electrical resistance. To produce an electrical energy output, it also requires an electrical energy input. The photoconductive cell will then produce an electrical output that is proportional to its light energy input. *Active transducers require one energy input while passive transducers require two energy inputs.*

The Copper Atom

- An Excellent Electrical Conductor

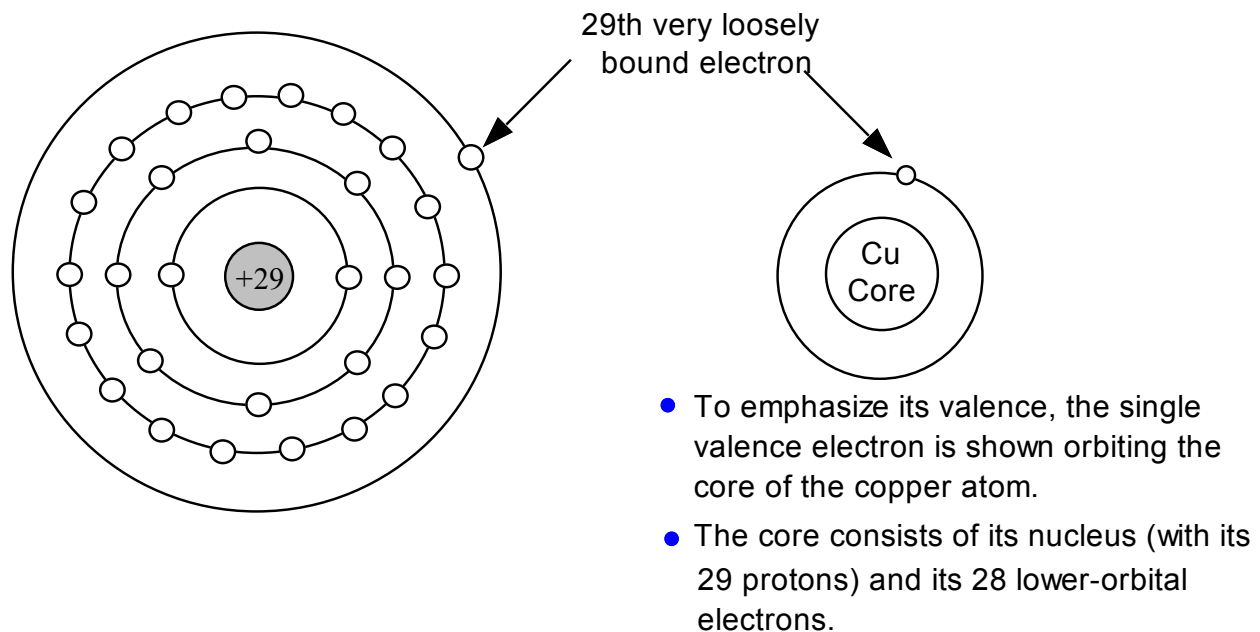


Figure 1-2.

Copper's 29th Electron is Essentially Free

The positive nucleus of an atom attracts the orbiting negative electrons. (Unlike charges attract one another.) The reason why the electrons are not pulled into the nucleus is due to their inertia. Specifically, *the electrostatic force drawing it toward the nucleus works with the electron's inertia to hold the electron in a stable circular orbit.*⁴ The closer an electron orbits the nucleus, the greater the attraction between it and the nucleus. The electrons closest to the nucleus compensate by orbiting with the greatest speeds. The electrons furthest from the nucleus are not attracted as strongly which means their required velocity is less. Consequently, the electrons in the larger orbits travel more slowly than the electrons in the smaller orbits.

Because the 29th electron of the copper atom is so far from the nucleus, it is very loosely bound. If the electrons orbiting an atom absorb additional energy, they can rise to a higher orbit. If they receive enough energy, they can become freed from their parent atom. Because of this characteristic, the 29th electron of virtually all copper atoms is free at room temperature (25°C or 77°F). Therefore, copper is classified as a good electrical conductor because it has an abundance of free electrons. It is described as having good conductivity. This characteristic is *not* unique to copper. *The best electrical conductors (silver, copper, and gold – in that order) all have a single valence electron.*

⁴ Some untutored people believe an outward *centrifugal* force exists. They reason this centrifugal force counters the attractive force between the electrons and the protons in the nucleus. This is *not* the case. This centrifugal force is a fiction – much like the Leprechauns found in Irish folklore.

Metallic Bonding

In the case of electrical conductors, a cloud of free (negative) electrons exists. These free electrons move about randomly. Because the conductor atoms have each lost an electron, they are positive ions. A cloud of electrons surrounds the positive ions and therefore bonds them together. This is called **metallic bonding** [see Fig. 1-3]. There are two other types of bonding - *covalent* and *ionic*. These will be explained later.

Metallic Bonding in an Electrical Conductor

- The cloud of negative electrons bonds the positive Copper ions together.

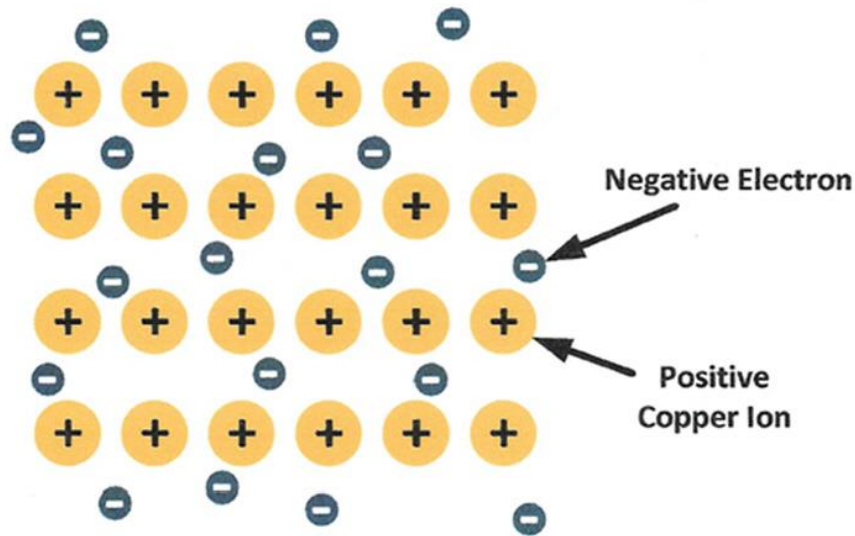


Figure 1-3.

Energy Levels

The law of conservation of energy states the total energy possessed by a body (e.g., an electron) remains constant. This means that at any point in space an electron's total energy is equal to the sum of its kinetic energy and its potential energy. An electron's kinetic energy (W_K) is given by Eq. 1-1.

$$W_K = \frac{1}{2} \text{mass} \times \text{velocity}^2 = \frac{1}{2} mv^2 \quad (1-1)$$

This means the outermost orbital electrons have the least amount of kinetic energy since they orbit so slowly compared to the innermost orbital electrons. However, their potential energy is the greatest.

Since an orbital electron is attracted to the nucleus, it must gain energy to be lifted to a higher orbit. When an electron moves to a higher orbit, it gains potential energy with respect to the nucleus. This is analogous to mechanical potential energy. When an object is lifted higher

above the earth, it gains potential energy with respect to the earth. The higher it is lifted the more work⁵ it can accomplish when it is released.

An electron can move to a higher orbit if it gains energy. An electron can gain (absorb) energy from light sources, heat (thermal energy), or from voltage sources. Figure 1-4 emphasizes the relationship between an electron's orbital radius and its energy level.

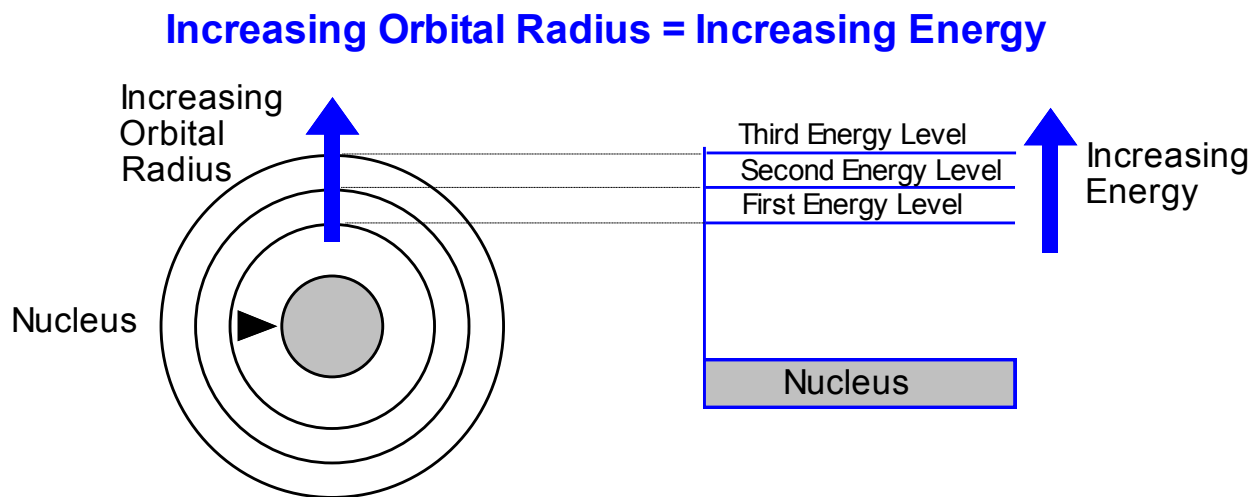


Figure 1-4.

Electrons Gain Energy to Rise and Lose Energy to Fall

Electrons can rise to a higher orbital if they gain enough energy. After an electron has been moved to a higher orbit (or energy level) it may fall back to its original energy level if it gives up its energy. Electrons give up their energy in the form of heat, light, or radiation (e.g., gamma rays). This is shown in Fig. 1-5.

While this discussion may seem extremely theoretical, it has significant practical value in explaining such things as why power transistors require heat sinks and how light-emitting diodes (LEDs) emit light. This will be explained fully when these topics are discussed.

⁵ In the mechanical world, work is often described as applying a force to a mass to move it over some distance. In the general sense, work is accomplished when the "flavor" of energy is changed. For example, a resistor converts electrical energy into thermal energy (heat). This is also work.

Electron Orbital Position is Affected by Its Energy

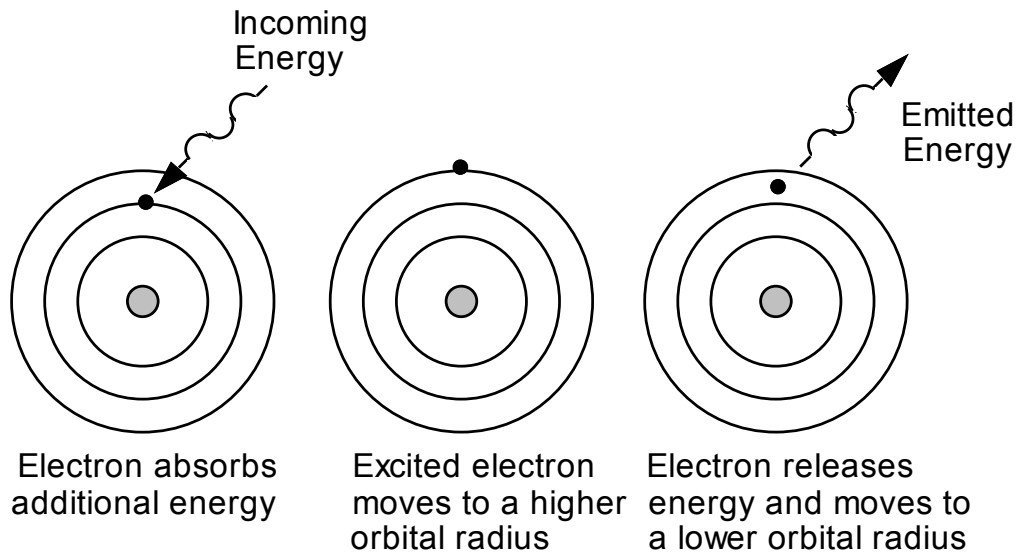


Figure 1-5.

Atoms in Crystals Have a Range of Possible Orbits Called Energy Bands

Crystals are solids with their atoms arranged in an orderly manner. Figure 1-6 shows the energy band concept. Isolated atoms will have distinct orbitals (energy levels). However, when atoms are brought close together (within two to three atomic diameters) considerable interaction will occur between them. This causes their orbital electrons to form bands of possible orbitals. These orbital bands are called **energy bands**. Consequently, when crystals are created, the proximity of the atoms causes the formation of energy bands.

Since the outermost orbital electrons are called an atom's valence electrons, their energy levels form the **valence energy band**. Electrons that gain enough energy to escape their parent atoms are called **free electrons**. Since free electrons support electrical conduction, they are said to lie in the **conduction energy band**. (The valence and conduction energy bands are depicted in Fig. 1-7.)

Formation of Energy Bands

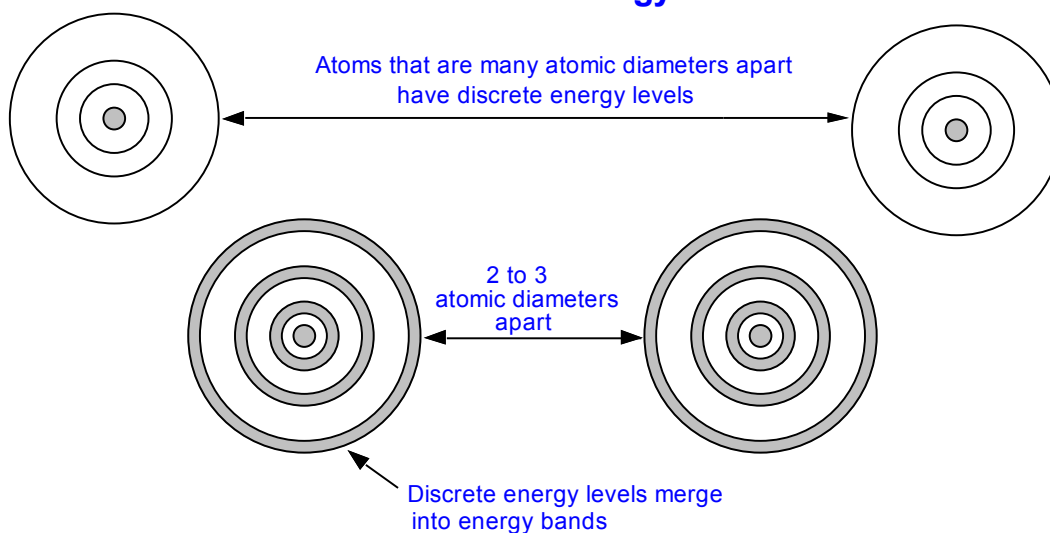


Figure 1-6.

Development of the Energy Diagram

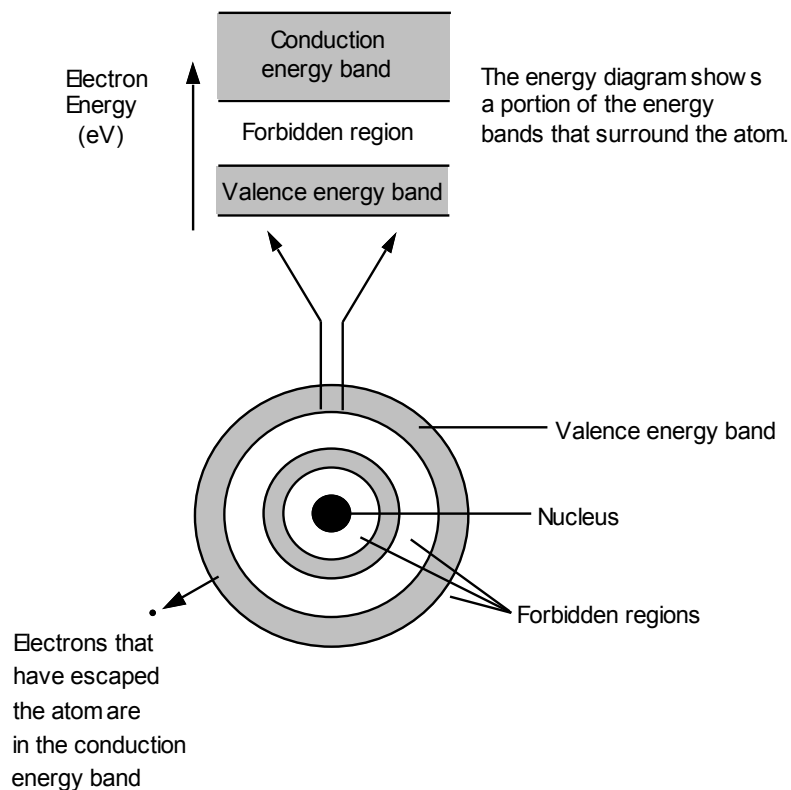


Figure 1-7.

Energy Levels are Measured Using Electron Volts (eVs)

The energy diagram for a given atom is developed in Fig. 1-7. Electron energy levels are usually described in terms of *electron volts (eVs)*. *An electron volt is a fundamental unit of energy.* To understand what an electron volt is, we first review the definition of a volt.

One volt is the potential difference between two points in an electric circuit when the energy required to move one coulomb of charge (electrons) between the two points is one joule.

The basic definition of a volt is given in Eq. 1-2.

$$V = \frac{W}{Q} \quad (1-2)$$

where V = electrical potential (volts)

W = energy (joules)

Q = charge (coulombs)

(Hence, one volt is a joule per coulomb: $1 \text{ V} = 1 \text{ J}/1 \text{ C}$.) We can apply Eq. 1-2 to solve for the energy required by an electron to rise or fall through a potential difference of one (1) volt. The charge of a single electron has a magnitude of 1.602×10^{-19} coulomb.

$$W = VQ = (1 \text{ V})(1.602 \times 10^{-19} \text{ C}) = 1.602 \times 10^{-19} \text{ J} = 1 \text{ eV}$$

The electron volt is equivalent to 1.602×10^{-19} J of energy. It should not be too much of a mystery why the electron volt is used. Which basic unit of energy would *you* rather remember 1 eV or 1.602×10^{-19} J? **Observe the vertical axis of the energy diagram in Fig. 1-7 has units of electron volts.**

Energy Diagrams for Conductors, Semiconductors, and Insulators

Observe in Fig. 1-7 that there are *forbidden regions* between the bands of orbitals. Electrons do not orbit in the forbidden regions. However, they can jump quickly over them⁶. Electrons must possess enough energy to jump from one energy band to a higher energy band. Electrons that do not have enough energy to jump across a forbidden region will remain where they are. For example, for an electron to make the jump from the valence energy band to the conduction energy band, it must have enough energy to make the jump or it will remain in the valence energy band.

Since we are only interested in the valence energy band and the conduction energy band, the energy diagram emphasizes these regions. The energy difference between the valence and conduction bands is called the *band gap*. The three basic classifications in the electrical conductivity of insulators, semiconductors, and conductors can be based on their respective energy diagram band gaps. Their definitions and examples are provided in Fig. 1-8.

The band gap for an electrical conductor is *zero*. This is because the valence and conduction bands *overlap*.

⁶ When an electron gains enough energy, it will cease to exist in the lower energy level and appear in the higher energy level instantly.

The Bandgap Indicates a Material's Nature

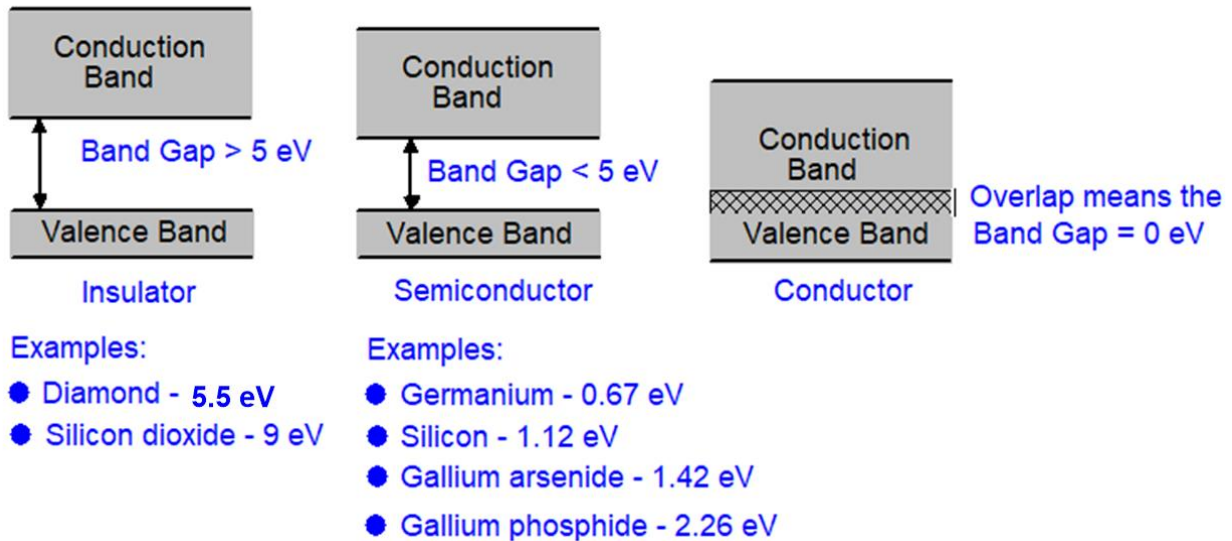


Figure 1-8.

1-3 Semiconductors

Semiconductors have an electrical resistance that falls between that of electrical conductors (ideally zero ohms) and electrical insulators (ideally infinite ohms). From an atomic viewpoint, all semiconductors have four (4) valence electrons. Therefore, they are described as being **tetravalent**. In Table 1-1, we see a partial periodic table of the elements. The various elements, their individual chemical symbols, and their respective total (electrically neutral state) number of electrons is provided. Two of the most popular semiconductors are the elements silicon (Si) and germanium (Ge). Silicon has a total of 14 orbital electrons while germanium has 32 orbital electrons [see Fig. 1-9].

The silicon and germanium atomic representations can be simplified further as shown in Fig. 1-9. The **core** of the silicon atom contains its nucleus and its ten lower-orbit electrons. This serves to emphasize its four valence electrons. In a similar fashion, the core of the germanium atom contains its nucleus and 28 of its lower-orbit electrons.

Table 1-1. A Partial Periodic Table of the Elements

Valence 3	Valence 4	Valence 5
Boron (B) 5	Carbon (C) 6	Nitrogen (N) 7
Aluminum (Al) 13	Silicon (Si) 14	Phosphorous (P) 15
Gallium (Ga) 31	Germanium (Ge) 32	Arsenic (As) 33
Indium (In) 49	Tin (Sn) 50	Antimony (Sb) 51

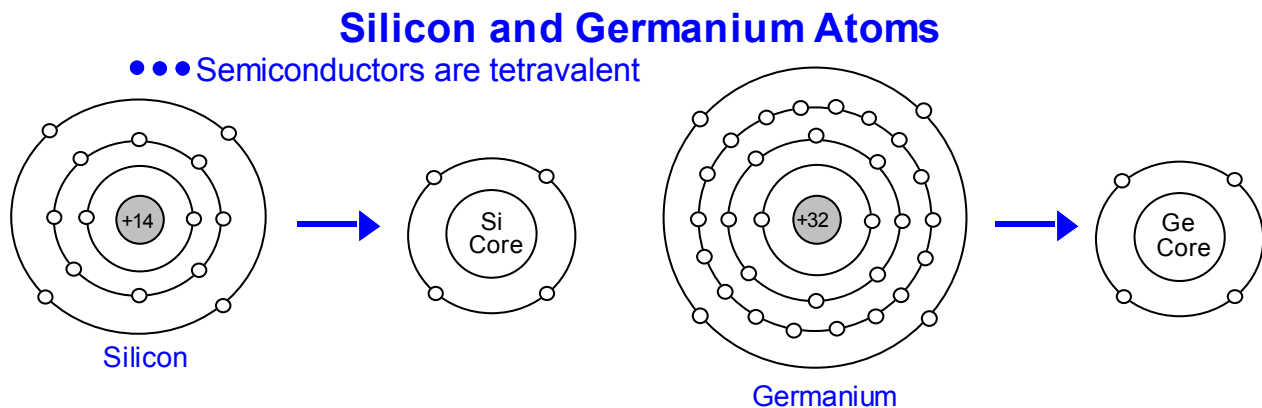


Figure 1-9.

Germanium was the first (1950's) semiconductor to be used in the commercial manufacture of solid-state devices but was replaced by silicon (1960's) because of silicon's superior performance. Today, silicon is still the most widely used semiconductor to make integrated circuits and solid-state devices. [However, silicon and germanium have been combined more recently (2000's) to form high-speed, low-power, low electrical noise **heterojunctions**⁷ for use in bipolar junction transistors and in field-effect transistors.] When solid-state transducers are produced, it is often necessary to employ semiconductors other than silicon to optimize their response. For instance, various **oxides** behave like semiconductors. Nickel and cobalt oxides are used to make thermistors (temperature transducers). Zinc oxide (ZnO) is used to produce transient-suppression devices called **varistors**. Cadmium sulfide (CdS) and cadmium selenide (CdSe) are used to make photoconductive cells (optical transducers).

⁷ Heterojunctions are formed by the interface between two dissimilar semiconductors. Dissimilar semiconductors have different bandgaps.

Intermetallic compounds between **trivalent** (valence 3) and **pentavalent** (valence 5) elements also act like semiconductors. Some of these include gallium arsenide (GaAs), gallium arsenide phosphide (GaAsP), and gallium phosphide (GaP).

Gallium compounds are used to make light-emitting diodes (LEDs), laser diodes, and high-speed electronic devices and integrated circuits. (High-speed electronic devices are significant to applications such as computers and communications equipment including consumer electronics products like cellular telephones.)

Newer Semiconductors

New combinations of materials are under development constantly. For example, silicon carbide has been used to make LEDs that emit blue light. (The gallium compound LEDs can only produce infrared, red, yellow, and green light.) ***Blue LEDs are now made from Indium-Gallium-Nitride, which is more efficient.*** Silicon carbide use has also been extended to produce precision integrated circuits that can operate at extremely high temperatures (e.g., 300°C or 572°F). As mentioned previously, silicon and germanium have been combined recently to form high-speed devices that rival the capabilities of the gallium-compound-based devices.

1-4 Semiconductor Crystals and Covalent Bonding

Pure semiconductors are described as being ***intrinsic***. When an intrinsic semiconductor is first melted and then carefully cooled, it forms a crystalline structure⁸ called a ***crystal lattice***. In a crystal lattice, each atom shares one of its valence electrons with each of its four neighboring atoms. An intrinsic semiconductor promotes this uniform structure since its atoms are identical. When atoms share valence electrons, the condition is described as ***covalent bonding*** [see Fig. 1-10].

Specifically, to form the crystalline structure, two covalent bonds are involved between each pair of atoms. The result is that each atom effectively ends up with eight valence electrons. *To be stable, the semiconductor atoms must have eight valence electrons.* Eight valence electrons is a “magic” condition. As further evidence of this, we examine elements that have eight valence electrons naturally. This is the case for the gases like neon, argon, and krypton. These elements are inert which means they are chemically inactive.

⁸ A **crystal** or **crystalline solid** is a solid material whose constituents (such as atoms, molecules, or ions) are arranged in a highly ordered microscopic structure, forming a crystal lattice that extends in all directions.

Semiconductor Crystals are Formed by Covalent Bonding

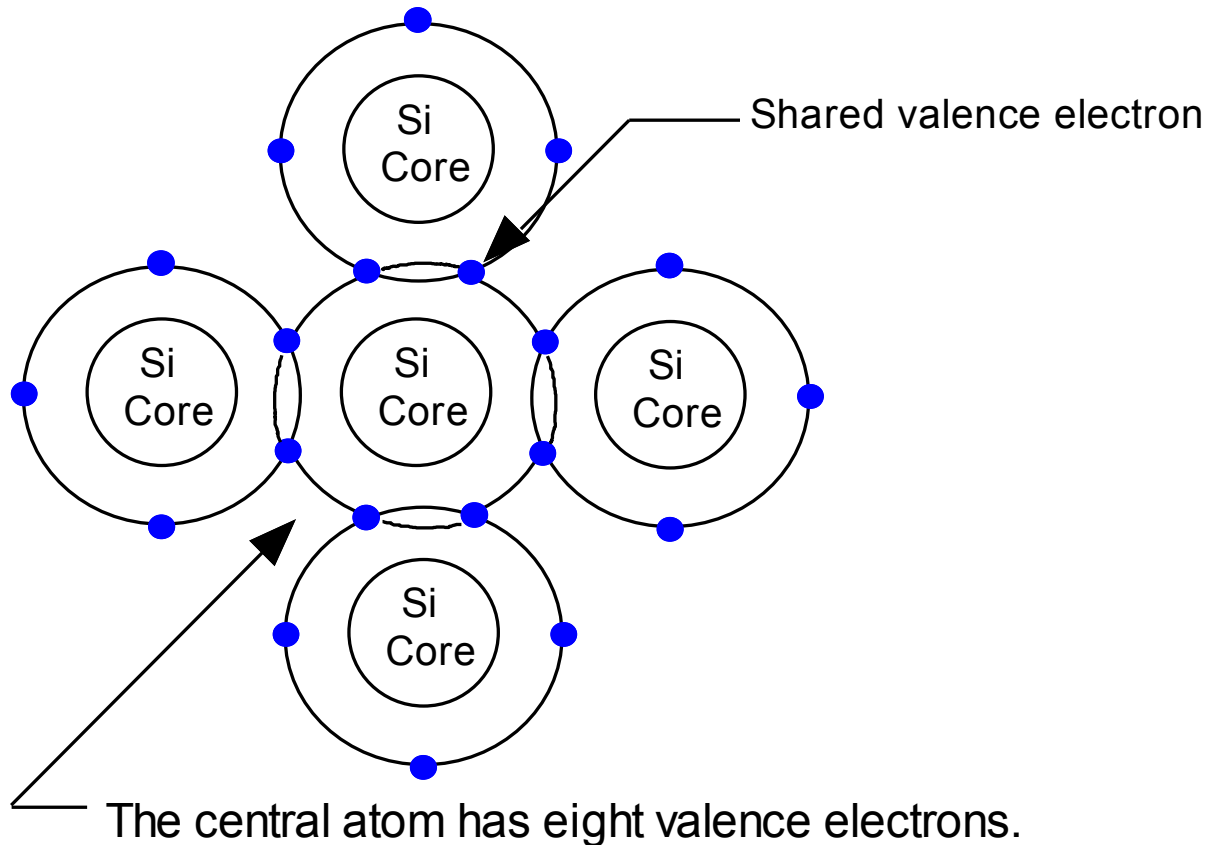


Figure 1-10.

To simplify discussions further, a **bonding diagram** such as that shown in Fig. 1-11 is often used. The bonding diagram for silicon has been indicated. However, the bonding diagram for germanium is virtually identical.

Semiconductor Compounds also Involve Ionic Bonding

Also shown in Fig. 1-11 is the crystalline structure for gallium arsenide (GaAs). Gallium is trivalent (valence 3) and it gives up an electron to the pentavalent (valence 5) arsenic atom when a gallium arsenide molecule is formed. Consequently, the gallium atoms become **positive ions** (Ga^+ ions) since they have each given up one of their electrons. The arsenic atoms become **negative ions** (As^- ions) since they have each gained an extra electron. Each positive gallium ion attracts a negative arsenic atom. The pair forms a molecule. The attraction between the pair of oppositely charged ions holds the gallium arsenide molecule together and is called **ionic bonding**.

When a crystal is formed, the ions are arranged alternately as shown in Fig. 1-11. The covalent bonding that occurs is like that in silicon but is reinforced due to the ionic bonding that occurs simultaneously. This is the reason the band gaps for the gallium compounds are so much larger than that for silicon [see Fig. 1-8].

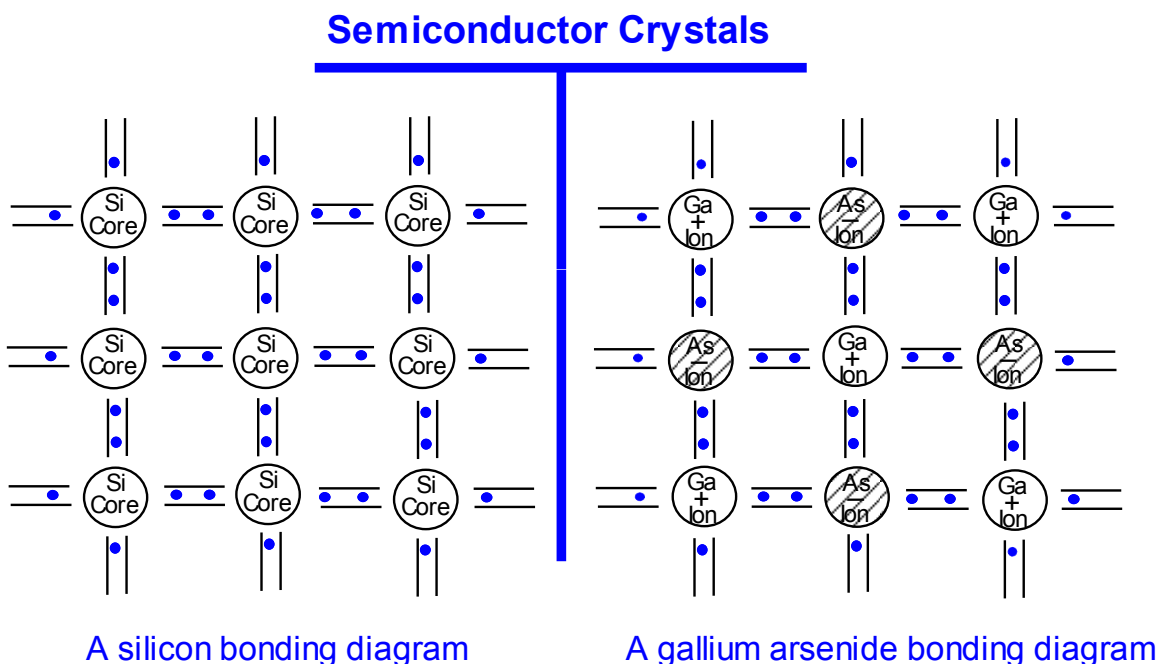


Figure 1-11.

1-5 Conduction in Pure (Intrinsic) Semiconductor Crystals

Now that we have a basic understanding of the structure of semiconductor crystals, we can investigate charge carrier movement. How a material conducts an electric current is very important. The operation of all solid-state devices is directly related to their mechanisms for the conduction of charge carriers.

In an intrinsic semiconductor with all the electrons taken up in covalent bonds, there are no free electrons [see Fig. 1-12]. The semiconductor will act like an insulator. However, this is only true when there is no thermal energy. (This is at a theoretical temperature called *absolute zero*.) At room temperature (25°C or 77°F) enough thermal energy exists to cause some of the electrons in the semiconductor to escape their parent atoms and become free electrons.

An Unexcited Silicon Crystal - no free electrons

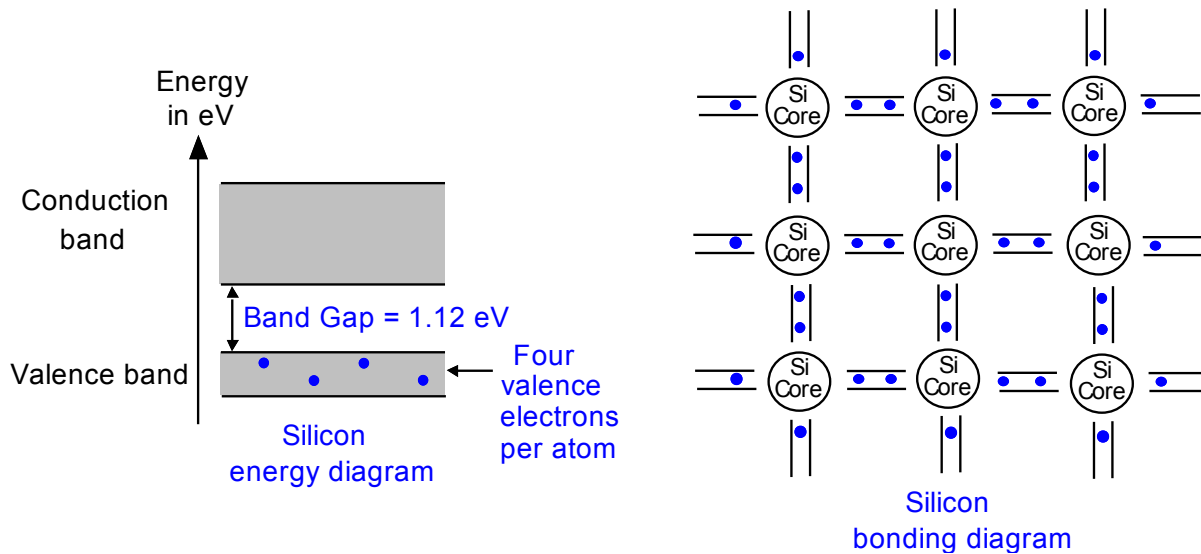


Figure 1-12.

Free Electrons and Holes Occur in Pairs

When an atom receives energy, it is typically absorbed by the orbital electrons. If a valence electron receives more than enough energy to jump from the valence energy band to the conduction energy band, it becomes a free electron. When a valence electron becomes free, it must break its covalent bond. A broken covalent bond is called a **hole** [see Fig. 1-13]. The silicon atom embedded in the crystalline structure becomes a positive ion. However, it is the broken covalent bond, or hole, which is significant here. Any free (conduction band) electron that loses enough energy to fall back to the valence energy band will be attracted to and captured by the hole. In this sense, *a hole behaves like a positive charge*. In a pure (intrinsic) semiconductor, every free electron produces a hole. Free electrons and holes occur in equal numbers. The operation of the most solid-state devices depends on not only the movement of free electrons, but holes as well.

An Excited Silicon Crystal -free electrons exist

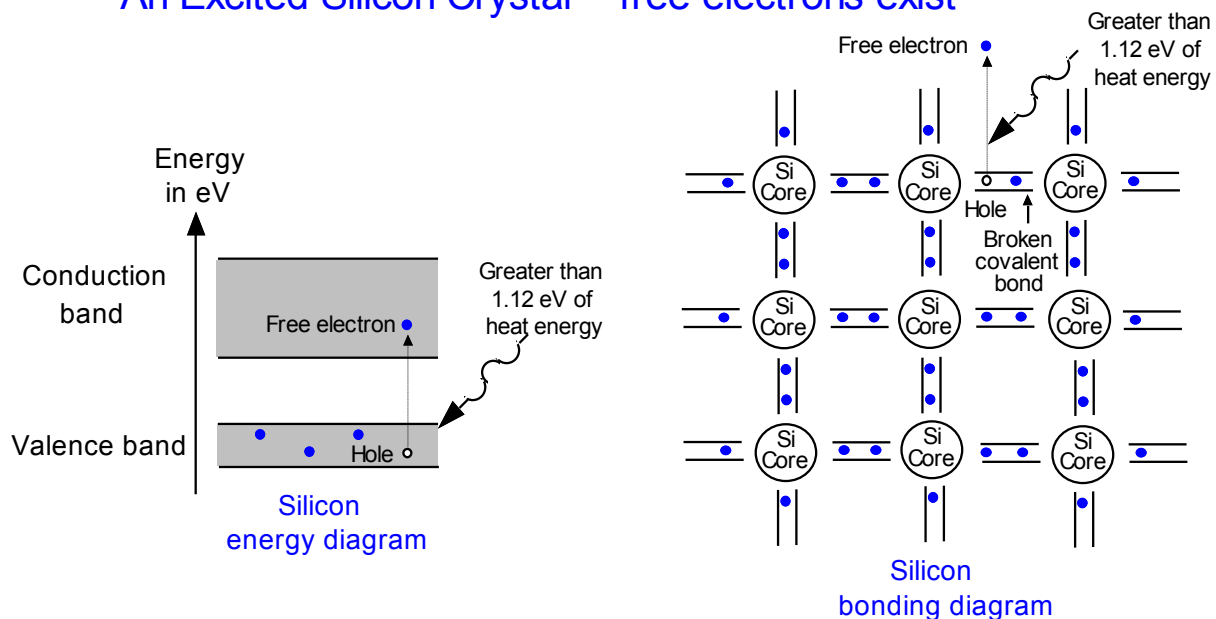


Figure 1-13.

Many beginning students find the concept of hole movement difficult. After all, if a hole is simply the absence of an electron, how can an absence move? However, consider the bubbles that rise to the surface in a liquid. What is a “bubble”? It is the absence of liquid. Liquid is dense in comparison. In fact, the liquid moves under the bubble to lift it toward the surface. The liquid is moving *down* such that the bubble moves *up*. This process is analogous to hole movement. Hole movement is depicted in Fig. 1-14.

Holes Flow Like Positive Charges

The “+” and “-” in Fig. 1-14 are used to represent an applied external voltage impressed across a semiconductor crystal. ***The valence electrons (just like conduction-band electrons) are attracted by the positive and repulsed by the negative.*** Since the valence electrons are attached to their parent atoms, they can only move into nearby vacancies (holes). As can be seen in the figure, the movement of the valence electrons toward the right means the holes must move to the left. The holes effectively move toward the negative and away from the positive. In this sense ***hole flow occurs and the holes act like positive charges.***

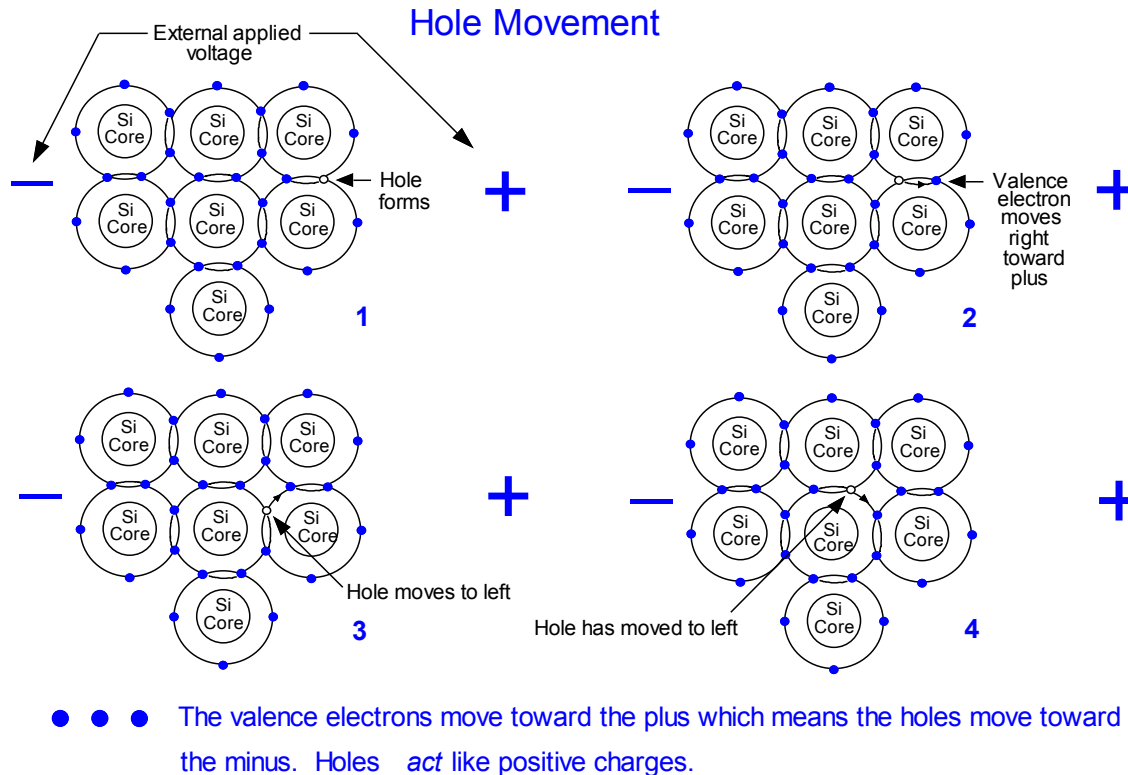


Figure 1-14.

The net movements of free (conduction band) electrons and the net movement of valence band electrons occur in the *same* direction. Although valence electrons cannot move as readily as free electrons, they are still repulsed by the negative pole and attracted to the positive pole of an external source. Since the holes move in the opposite direction of the valence electrons, they are repulsed by the positive pole and attracted to the negative pole. Thus, we have two distinct charge carrier movements - ***electron flow and hole flow***. Electron flow occurs in the conduction energy band, while hole flow occurs in the valence energy band. These are illustrated in Fig. 1-15.

Electron-Hole Movement in an Intrinsic Semiconductor

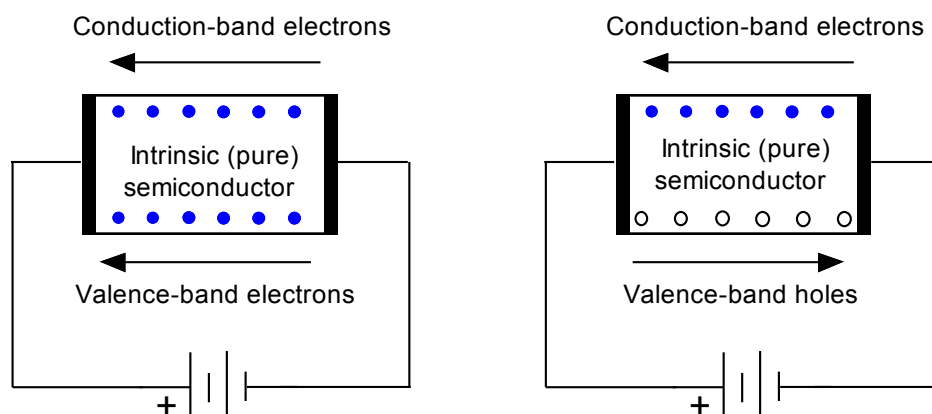


Figure 1-15.

1-6 Doped Semiconductors

In pure semiconductors we have an equal number of holes and electrons. However, by adding impurity atoms, it becomes possible to give a semiconductor crystal a majority of either holes or electrons. The reason for doing this is to make *p- and n-type semiconductors*. A semiconductor which has added impurities is called a *doped semiconductor*. Doped semiconductors are described as being *extrinsic*.

P-type Semiconductors

The formation of a *p*-type semiconductor is shown in Fig. 1-16. A trivalent impurity such as boron (with its chemical symbol B as shown in Table 1-1) is doped into the crystalline structure. This means an occasional silicon (or germanium) atom is replaced by a trivalent impurity atom. Consequently, a broken covalent bond is built into the crystal. A broken covalent bond is a hole and a hole acts like a positive charge in that it will attempt to attract and capture a free electron. The energy diagram for a *p*-type semiconductor is also shown in Fig. 1-16. Since the holes act like positive charges, the semiconductor, which has been doped with trivalent impurities, is called a *p*-type semiconductor. *The “p” designation is used to suggest the positive-acting nature of the holes built into the crystal.*

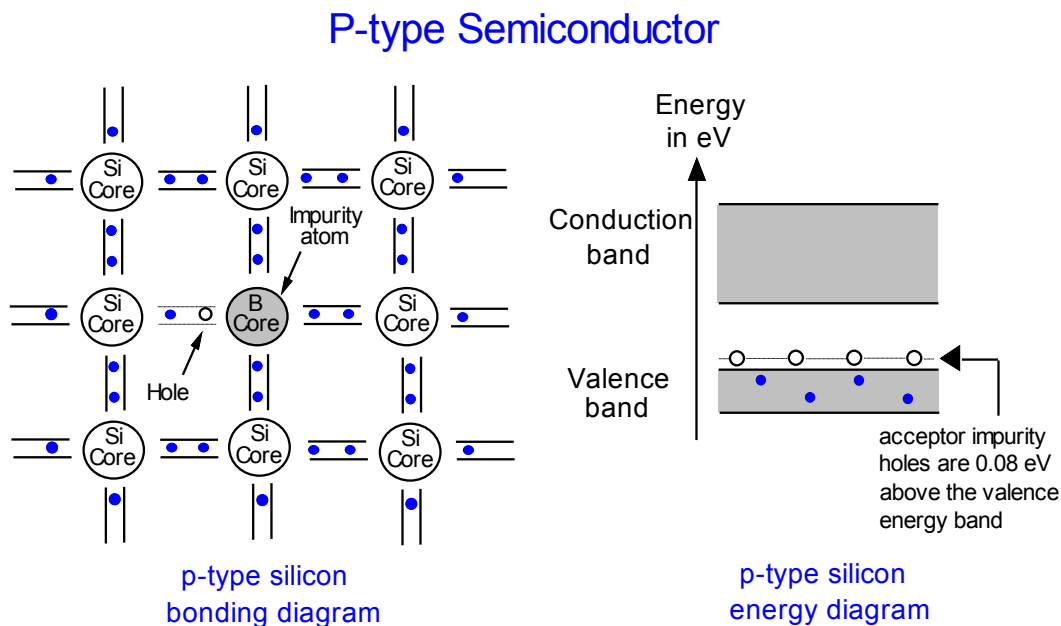


Figure 1-16.

Acceptor Impurities are the Trivalent Elements used to Dope in Holes

The energy diagram shows the trivalent boron produces holes that are only 0.08 eV above the valence energy band for the silicon atoms in the crystalline structure.

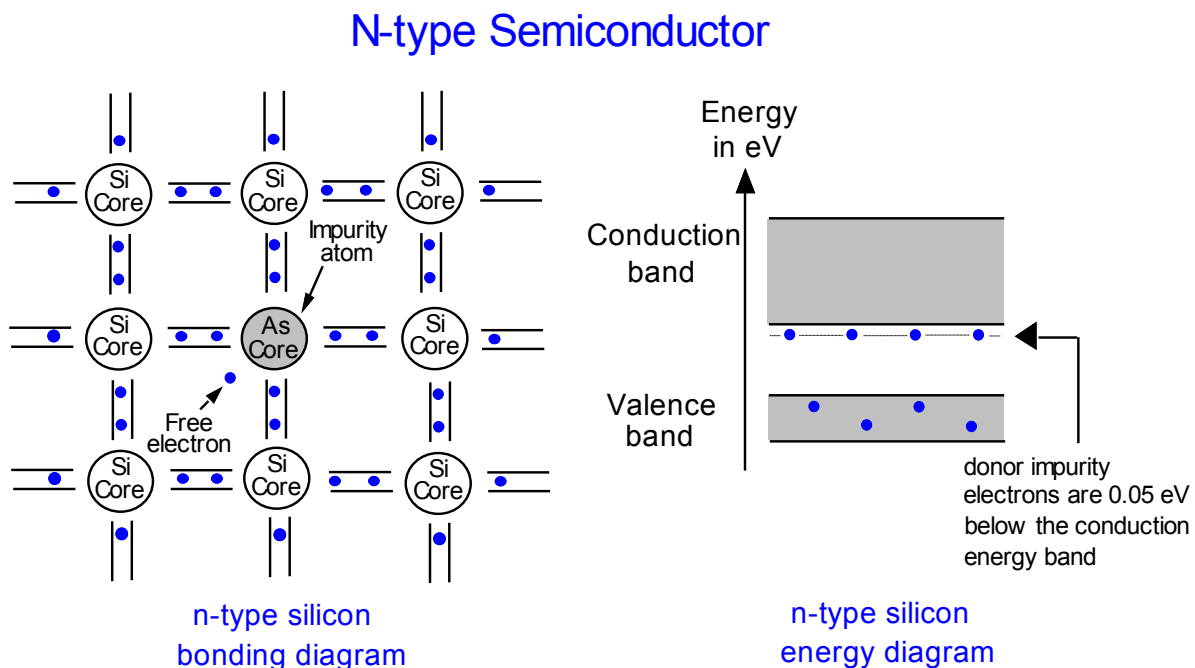
The band gap between the valence and conduction energy band remains at the much higher value of 1.12 eV for the silicon atoms. The trivalent impurities are referred to as being *acceptor impurities* since they will accept or capture free electrons.

N-type Semiconductors

The formation of an n -type semiconductor is shown in Fig. 1-17. A pentavalent impurity such as arsenic (Table 1-1) is doped into the crystalline structure. This means an occasional silicon (or germanium) atom is replaced by a pentavalent impurity atom. Since the pentavalent impurity has five (5) valence electrons, one of its electrons will not be taken up in a covalent bond. Therefore, when the crystalline structure forms the fifth electron tends to be very loosely bound to its parent (impurity) atom. In fact, at a temperature as “warm” as -200°C , enough thermal energy exists to ionize impurity atoms. Consequently, at room temperature (25°C) most of the impurity atoms are ionized. Therefore, many free electrons are built into the crystal. The energy diagram for an n -type semiconductor is also shown in Fig. 1-17. *The “ n ” designation is used to suggest the negative nature of the free electrons built into the crystal.*

Donor Impurities are the Pentavalent Elements used to Dope in Free Electrons

The energy diagram shows the pentavalent arsenic produces electrons that are only 0.05 eV below the conduction energy band for the silicon atoms in the crystalline structure. This serves to reinforce the fact that most of the donor-atom electrons will be free at room temperature. Again, the band gap between the valence and conduction energy band remains at 1.12 eV for the silicon atoms. The pentavalent impurities are referred to as being *donor impurities* since they donate free electrons.



Minority Carriers are Important

In the case of *p*-type semiconductors, there are many holes. Although holes are the majority carriers in *p*-type semiconductors, electrons are also present because an occasional silicon atom will experience thermal ionization [see Fig. 1-18]. While ionization results in the formation of another hole as well, it is the free electron that is significant here. ***Electrons are the minority carriers in a p-type semiconductor.***

In *n*-type semiconductors, there are many free electrons. Electrons are the majority carriers in *n*-type semiconductors. Thermal ionization will release another electron, but it is significant that a hole is also formed. ***Holes are the minority carriers in n-type silicon*** [see Fig. 1-18].

Thermal Ionization Produces Minority Carriers

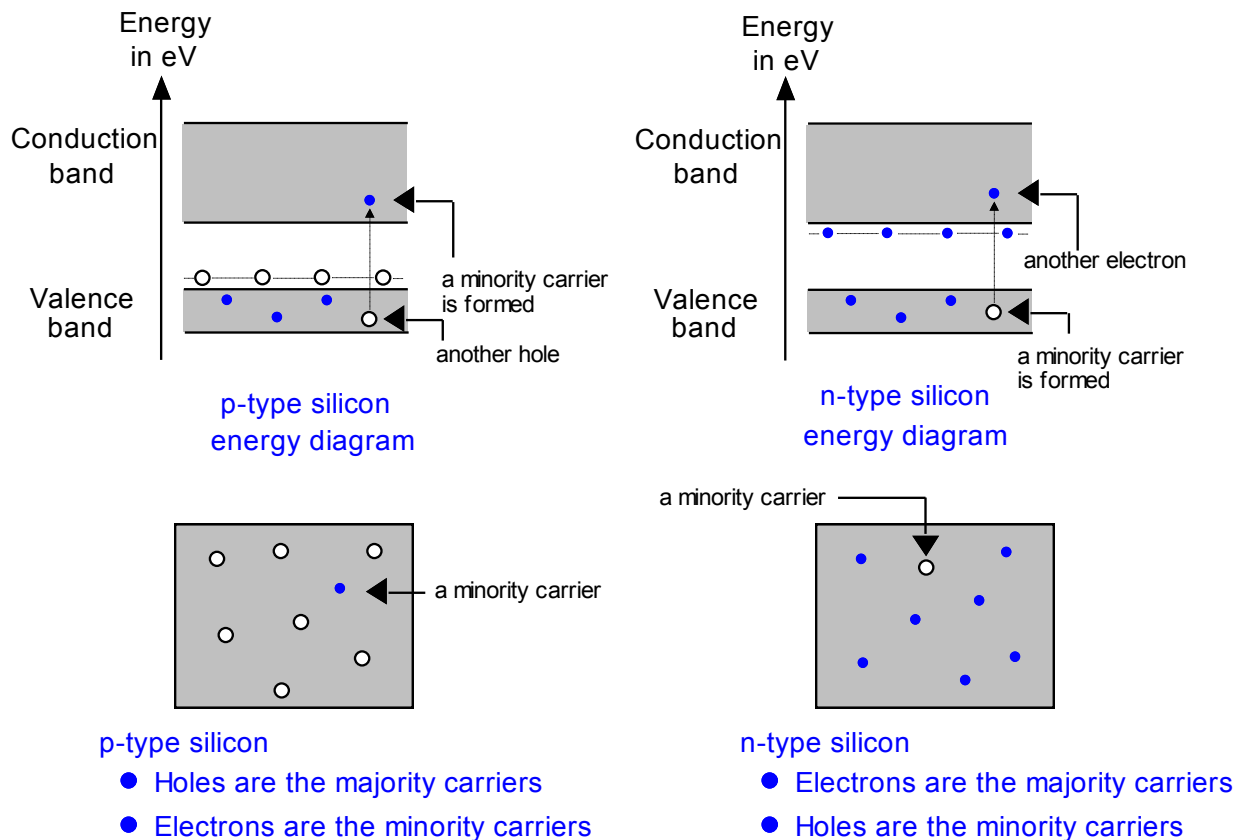


Figure 1-18

Raising the Temperature Increases the Number of Minority Carriers

The number of minority carriers is a strong function of temperature. These minority carriers will have a strong effect on the operation of solid-state devices. Consequently, the electronic devices tend to be very temperature sensitive. We will see exactly what this means as our studies progress. We will also see what steps are taken in the design of electronic circuits to minimize the influence of these effects.

1-7 Organic Semiconductors

Modern chemistry defines organic compounds to be based on carbon. In Table 1-1 we see that carbon is tetravalent just like silicon and germanium. It would make sense that carbon can be used as a semiconductor. There are some other considerations. Before we delve into them, we revisit silicon, which in an *inorganic* semiconductor.

Allotropes?

The term *allotrope* refers to two or more structures made from atoms of the same element. The atoms within the structures have different (bonding) arrangements. The properties of allotropes can vary dramatically. Silicon has two allotropes: *amorphous* and *crystalline*.

Amorphous silicon is a powdery substance that is brown in color⁹. The atoms in the structure are mostly connected throughout, but some atoms are *not* bonded to their maximum capacity. This makes amorphous silicon flexible, but not especially strong. Since silicon is a semiconductor, amorphous silicon is a great material for use in devices (transducers) that convert light energy into electrical energy. Amorphous silicon is used for solar modules (found in photovoltaic arrays) and solar cells that are used in calculators, watches, and more. Amorphous silicon is a low-cost option when compared to crystalline silicon. However, amorphous silicon is not as efficient nor as stable as crystalline silicon.

Crystalline silicon (also called polycrystalline or monocrystalline) is a metallic grey solid substance. Since the atoms in the structure are fully bonded throughout, crystalline silicon is stronger and more stable than amorphous silicon. Like amorphous silicon, crystalline silicon is used in solar panels and solar cells. It is also used extensively in integrated circuits in electronics, like the computer or smart phone you're using to view this text.

Allotropes of Carbon

Carbon comes in two *basic* allotropes, the soft black *graphite* found in pencils and the hard, sparkly *diamond* crystals found in jewelry stores. Why is graphite different from diamond? The atoms inside the two materials are arranged in different ways. This is what gives the two allotropes their completely different properties: graphite is black, dull, and relatively soft while diamond is transparent and the hardest natural material so far discovered. Each carbon atom in a **diamond** is covalently bonded to four other carbon atoms in a three-dimensional array.

There are several other allotropes of carbon. These include (among many others) *graphene* and *carbon nanotubes*. Graphene is derived from graphite.

Graphite has many layers. If we obtain a single layer, it will be *one atom thick*. When the bonding is included in the illustration, we obtain the “chicken wire” structure shown in Fig. 1-19.

⁹ Amorphous means without form – shapeless.

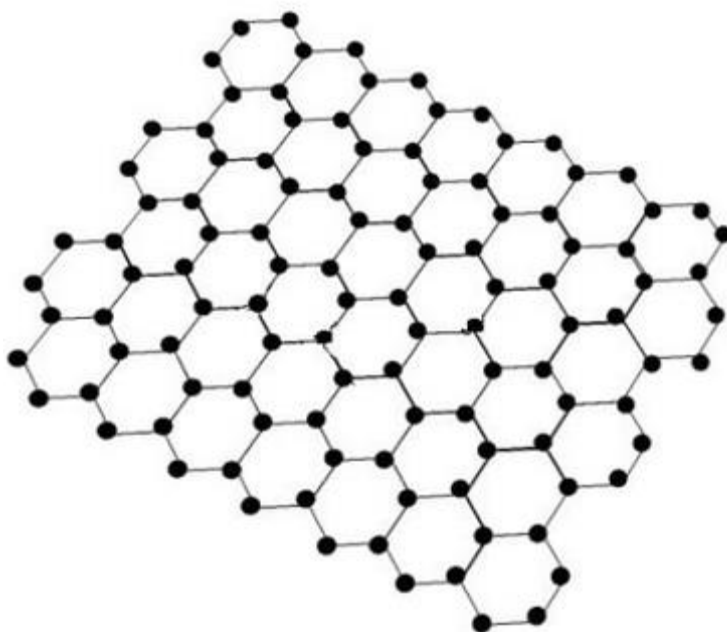


Figure 1-19

The dots in Fig. 1-19 represent the carbon atoms while the lines represent covalent bonds. Graphene was first discovered in 2004. Its properties (the way it behaves as a material) are remarkable and exciting. Briefly, it's incredibly strong and stiff, amazingly thin, almost completely transparent, extremely light, and an amazing conductor of electricity and heat. It also has some extremely unusual electronic properties.

- 100 to 200 times the tensile strength of steel
- Can be stretched (like rubber) 20 – 25% of its original length
- It is very light since it is only one atom thick. It has been estimated *one* gram of graphene could cover a football field.
- Graphene is better at conducting *heat* than silver or copper.
- Materials that conduct heat well also tend to conduct electricity well. Both processes transport energy using electrons. The flat, hexagonal lattice of graphene offers relatively little resistance to electrons.
- The electronic properties of graphene are also remarkable. The electrons travel faster and are much more mobile compared to inorganic technologies. This means the possibility the development of computer (digital) integrated circuits that are faster (and use less power) than other technologies.
- Because graphene is only one atom thick, it allows light to readily pass through it. This makes it work well in displays, HD televisions, and solar modules.

Carbon Nanotubes

Carbon nanotubes are constructed from graphene. The formation of a single-walled carbon nanotube (SWNT) is illustrated in Fig. 1-20. This is a *conceptual* drawing. The actual fabrication of nanotubes is a very involved process.

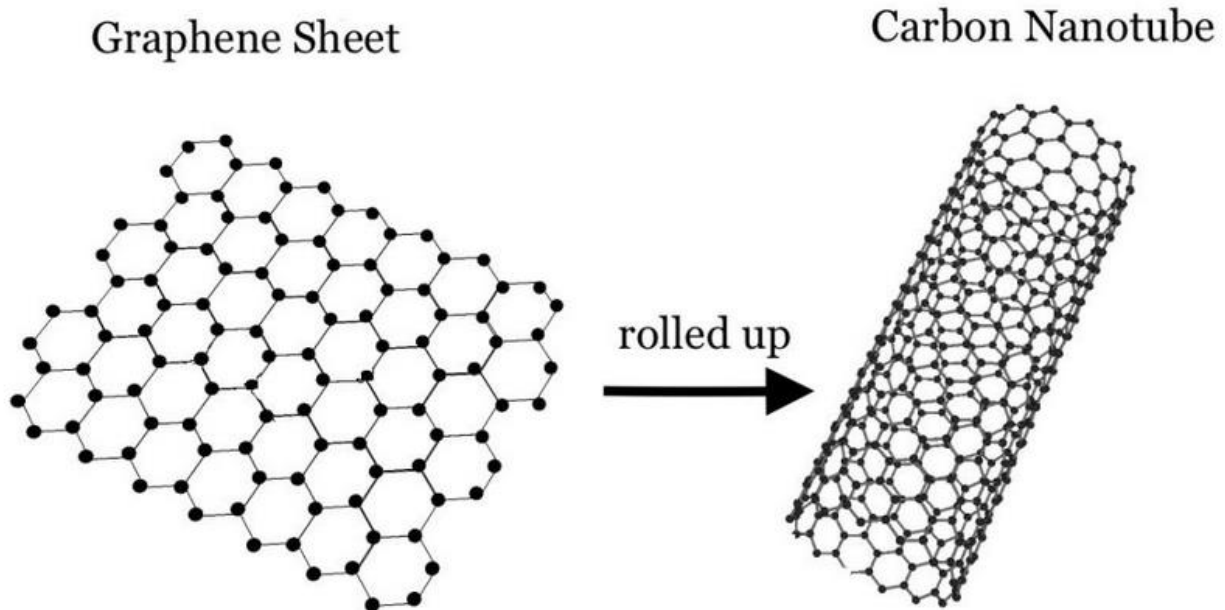


Figure 1-20

Carbon nanotubes have a diameter of about one nanometer. Because they are constructed from graphene, they have the same basic characteristics. Electrons travel through a nanotube as depicted in Figure 1-21. There are relatively few collisions between electrons and carbon atoms. This means the electrical resistance of the nanotube is extremely low.

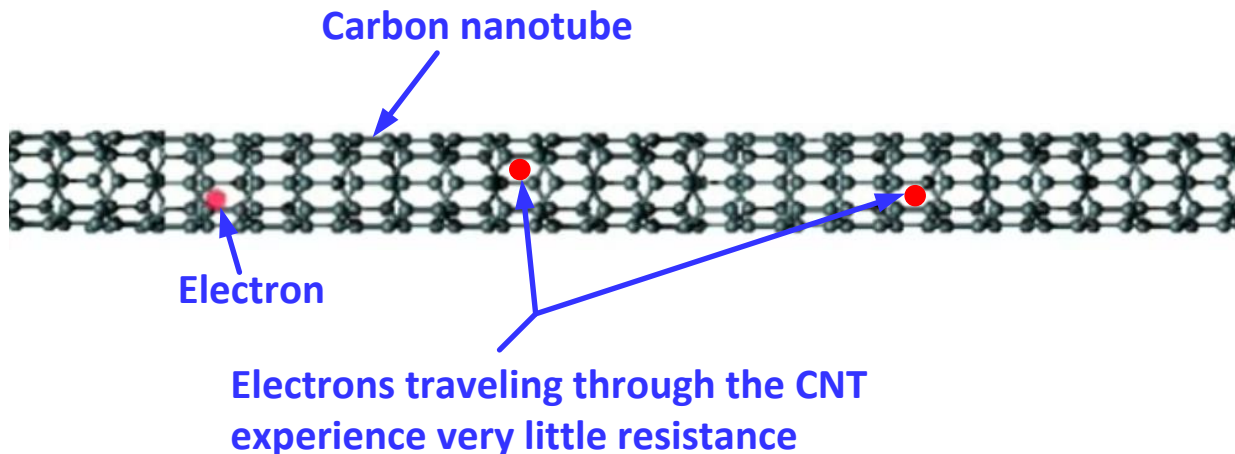


Figure 1-21

The electrical properties of a nanotube depend on how the hexagon arrangements are oriented with respect to its longitudinal axis. Three common arrangements are shown in Fig. 1-22. The arrangements are called *armchair*, *zigzag*, and *chiral*, respectively.

Carbon nanotubes with their hexagons are lined up in parallel to the longitudinal axis are in the armchair arrangement. ***Nanotubes with the armchair arrangement behave like electrical conductors.*** Their low resistance makes them superior to the best electrical metallic conductors (silver, copper, and gold).

Carbon nanotubes with the hexagons oriented in a circle around the nanotube are in the zigzag configuration. Carbon nanotubes with a twist such that the hexagons do not form any line are called chiral. The zigzag and chiral configurations of nano tubes will only conduct an electric current when extra energy in the form of light or an electric field is applied. This extra energy will free electrons from the carbon atoms. ***These nanotubes act like semiconductors.*** These semiconductors can be used to build electronic devices like light-emitting diodes and field effect transistors.

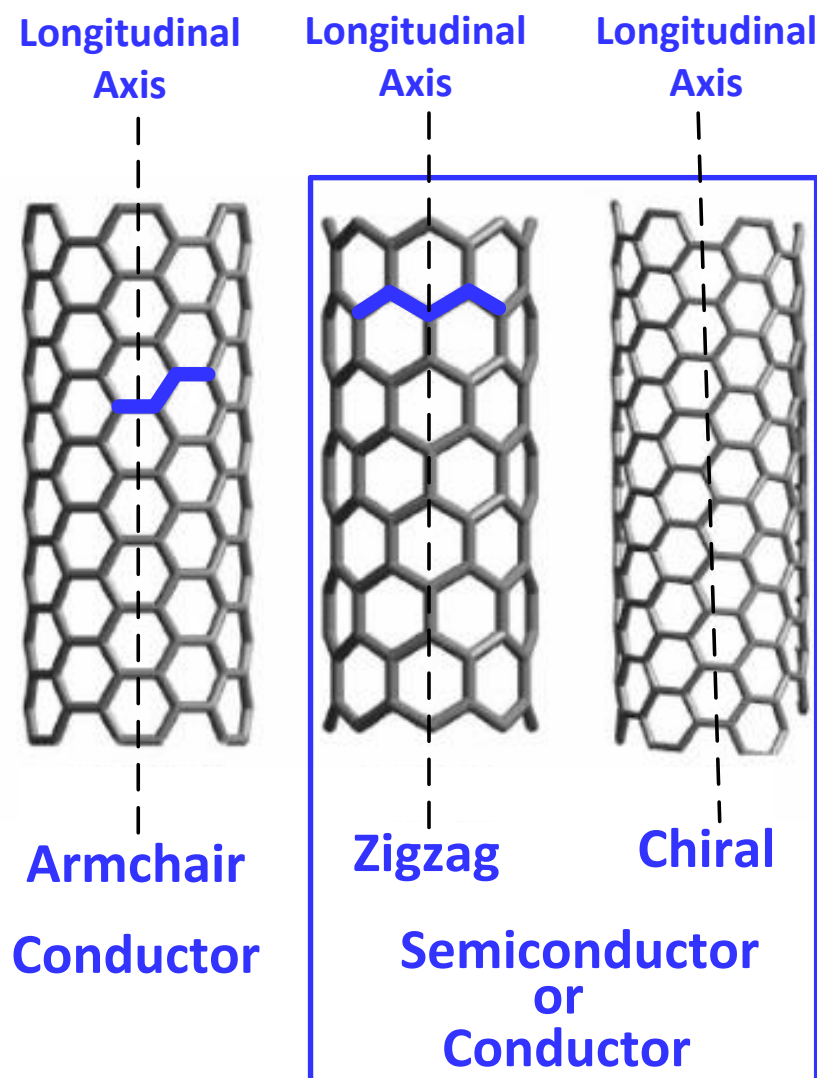


Figure 1-22

Figure 1-23 shows the image of carbon nanotubes as produced by using a scanning electron microscope (SEM).

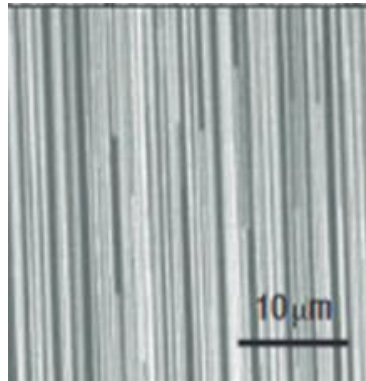


Figure 1-23

In this case, a 10-um distance is used to hold 5 SWNTs. SWNT are used to produce electronic devices. An example of an electronic device is a Field Effect Transistor (FET) is depicted in Fig. 1-24. The FET has three terminals called the drain, gate and source. FETs are covered in Chapter 6.

FET Construction Using Carbon Nanotubes

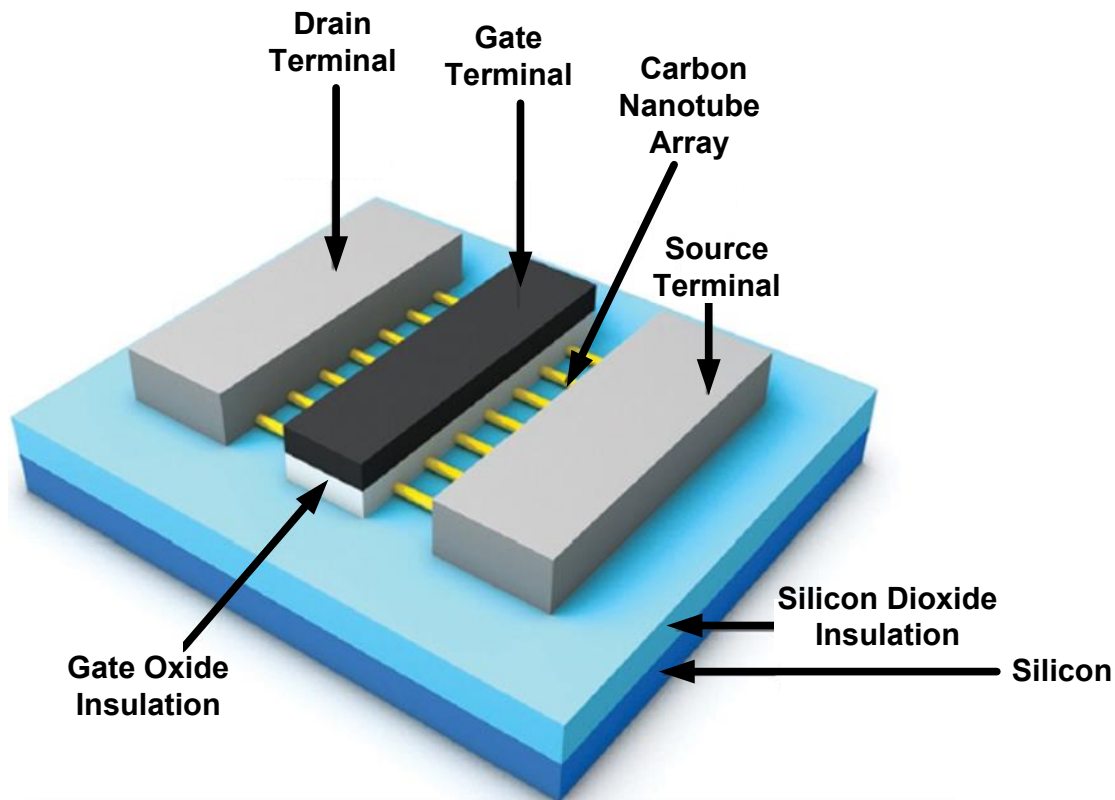


Figure 1-24

Organic semiconductors are less expensive to manufacture compared to inorganic semiconductors. Inorganic semiconductors are glass-like which means they are rigid and fragile. In contrast organic semiconductors can be flexible. Examine Fig. 1-25. Organic light-emitting diodes (OLEDs) are designed to produce red, green, and blue light. These three colors allow all other colors of visible light to be produced. Consequently, OLEDs are used in the manufacture of high-definition televisions (HDTVs), smart phone and computer displays, and large billboards.



Figure 1-25. OLED Display (Courtesy of Street Communication, www.streetcommunication.com)

1-8 The *P-N* Junction

Isolated *n*-type and *p*-type semiconductors are shown in Fig. 1-26. When these two separate materials are merged together to form a continuous crystal, the interface between them is called a ***p-n junction***¹⁰. The characteristics of the *p-n* junction are fundamental to the operation of virtually all solid-state devices - including integrated circuits.

The majority carriers in the *n*-type material are electrons while the minority carriers are holes. The majority carriers in the *p*-type material are holes while the minority carriers are electrons. Their respective energy levels are also indicated in Fig. 1-26. Although the *n*-type

¹⁰ Two separate materials are *not* brought together and fused. Very careful, controlled processing is used to make a single crystal with an *n* region adjacent to a *p* region.

semiconductor has an abundance of free electrons, it is electrically *neutral*. This is because each freed electron leaves behind a positive ion. The *p*-type semiconductor is also electrically neutral. The holes merely *act* like positive charges.

Isolated N- and P-type Semiconductors

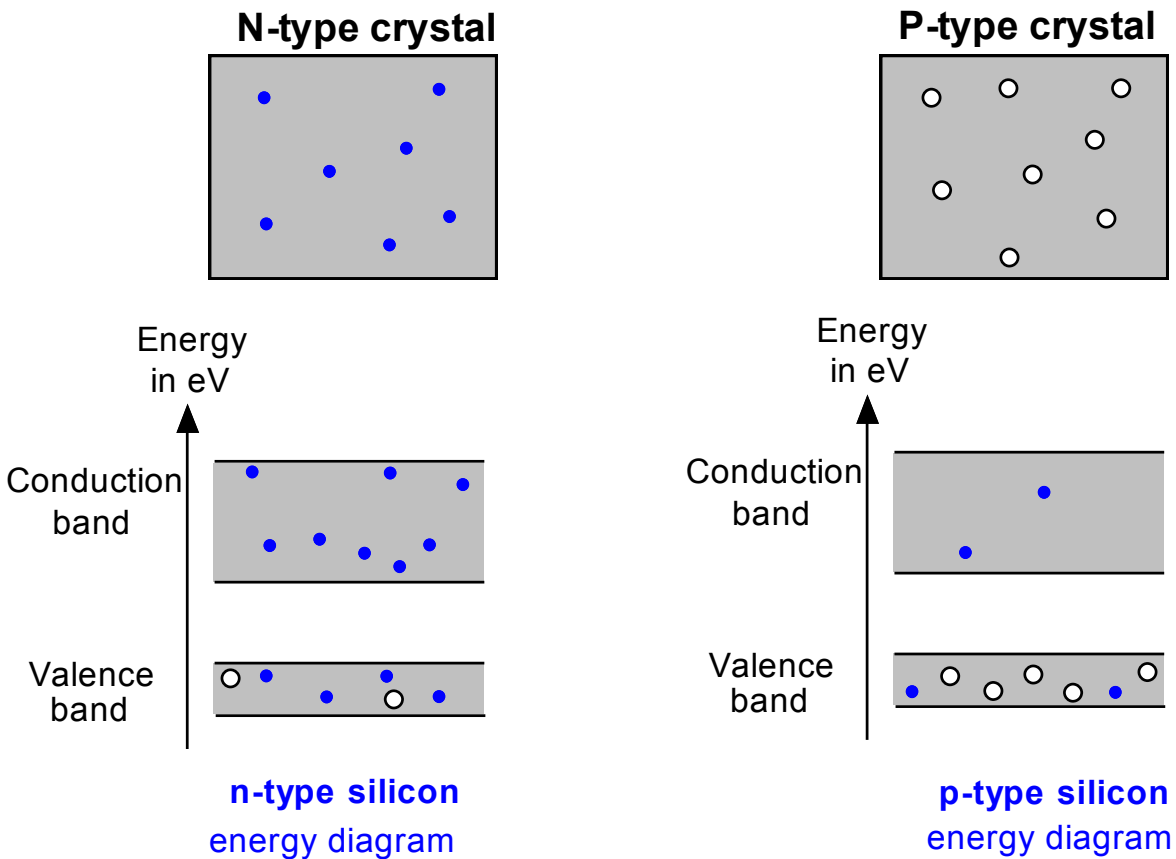


Figure 1-26

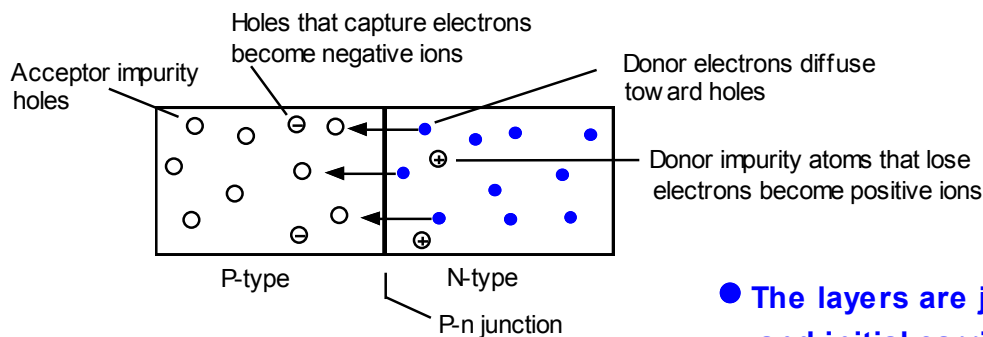
Solid-State Diffusion

Before we investigate the results of joining the separate *p*- and *n*-type semiconductors, we should understand the diffusion mechanism. **Diffusion** is the process by which mixtures of easily flowing materials (such as a drop of ink in a glass of water) naturally reach a final blend that is uniform in concentration. The solid-state diffusion of one material into another, even in small percentage concentrations, can cause dramatic changes in the characteristics of the resultant material. (Steel making is an example. When carbon is diffused into iron, the resultant metal is not only shiny, but much stronger as well.)

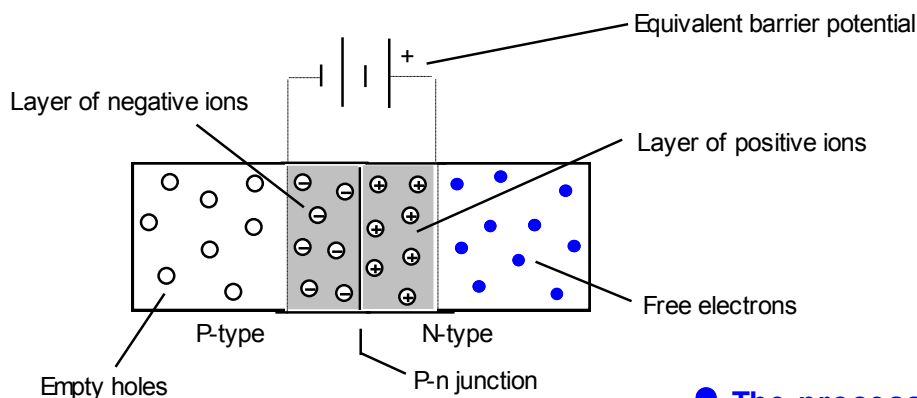
In the case of *n*- and *p*-type semiconductors, the joining of the two materials produces a diffusion of negative electrons from the *n*-type material into the *p*-type material. A diffusion of holes from the *p*-type material into the *n*-type material occurs simultaneously. As negative electrons leave the *n*-type material, the donor impurity atoms become positive ions. Therefore, a layer of positive ions forms on the *n* side of the *p*-*n* junction. On the *p* side of the junction, holes capture

negative electrons. Consequently, the acceptor impurity atoms become negative ions. A layer of negative ions forms on the p side of the p - n junction [see Fig. 1-27].

Forming a P-N Junction



- The layers are joined and initial carrier movement begins



- The process stops when the barrier potential becomes large enough

Figure 1-27

A Depletion Region Forms at the P - N Junction and Creates a Barrier Potential

The layer of ions that forms at the p - n junction is devoid or depleted of majority carriers. As a result, it is called the **depletion region**. Since the depletion region consists of immobile positive ions on the n -side and immobile negative ions on the p -side, an electric field exists between them. Whenever an electric field is impressed over a distance, a potential difference (voltage) is said to exist. The equivalent voltage is described as a **barrier potential**. The size of the barrier potential depends on the type of semiconductor. For instance, germanium has a barrier potential of approximately 0.3 V, silicon has a barrier potential of approximately 0.7 V, and the gallium compounds have barrier potentials that range from 1.2 to 1.9 V. *It is the barrier potential that stops the diffusion of the charge carriers across the junction.*

The Unbiased P - N Junction

An unbiased p - n junction is one that has no external DC voltage applied. In Fig. 1-28(a) we see the basic structure. As mentioned previously, a depletion region forms at the p - n junction interface. We shall see *the significant action occurs within the depletion region*. Consider Fig. 1-28(b). Thanks to covalent bonding each silicon atom has eight valence electrons. Thermal energy can liberate one of the valence electrons. The broken covalent bond is a hole.

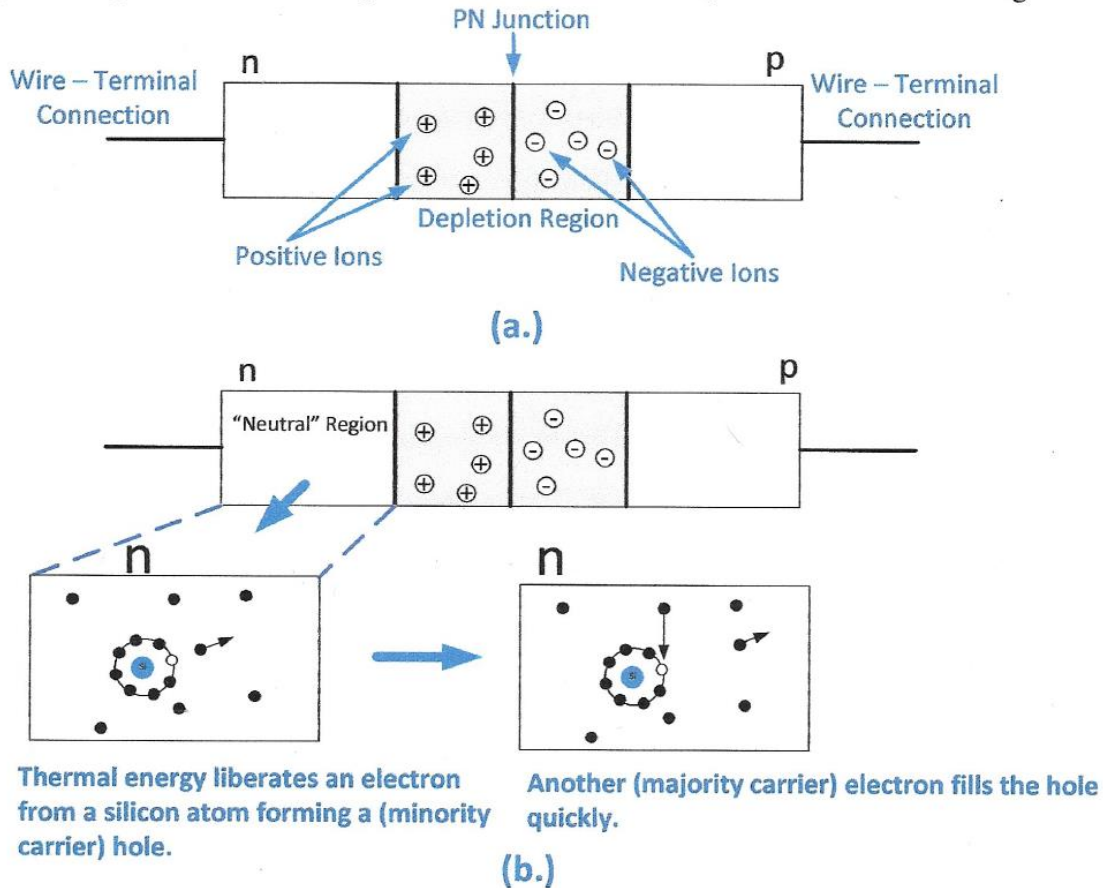


Figure 1-28

Figure 1-29 shows a similar condition exists in the p -region located to the right of the depletion region. Ionization of a silicon atom results in another majority carrier (hole) and a minority carrier (free electron). The abundance of holes means the free electron will recombine very quickly. *The n - and p -regions are essentially neutral. It is the action in the depletion region that is important.*

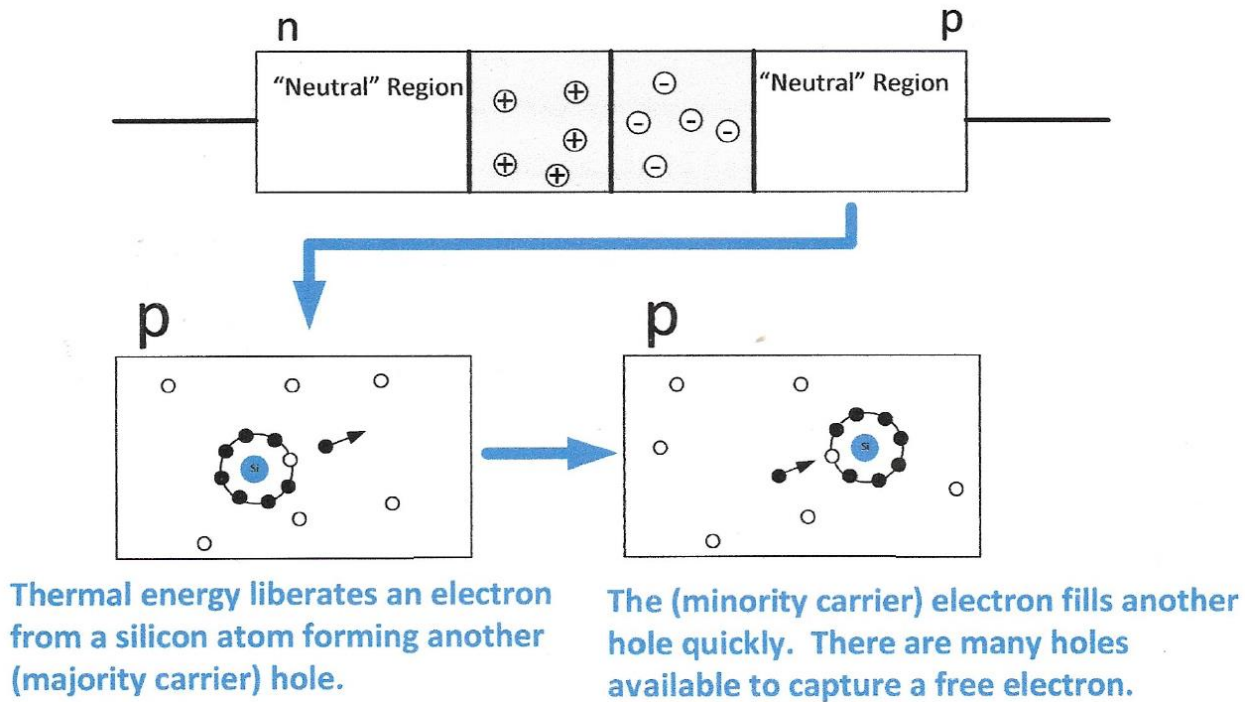


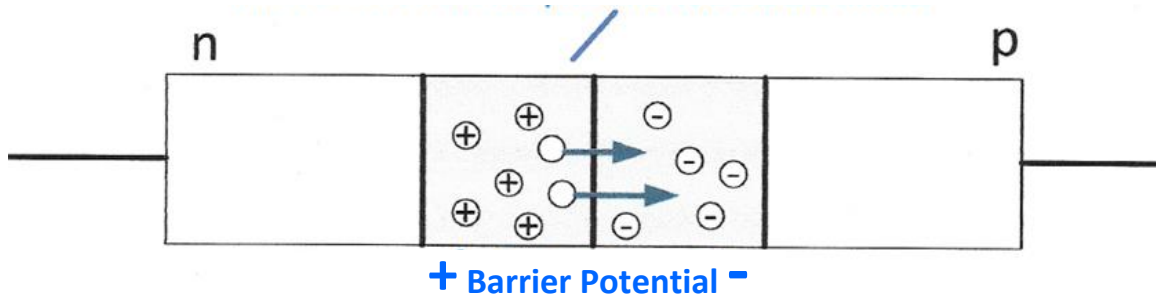
Figure 1-29

Drift and Diffusion Currents through an Unbiased P-N Junction

Before we examine the action within the depletion region, *we need to define the two key mechanisms for charge carrier movement. When charge carriers move under the influence of a voltage, the charge carrier movement is called drift current (I_{drift}).* Holes move away from the positive-most point and toward the negative-most point. Electrons move in the opposite direction. (With a little thought, we recognize that holes flow in the same direction as conventional current.) *As explained previously, diffusion is a process in which a region of heavy concentration tends to move into regions of lesser concentration.* This means a concentration of holes will tend to move away from one another as will a concentration of free electrons. This charge carrier movement is called *diffusion current ($I_{diffusion}$)*.

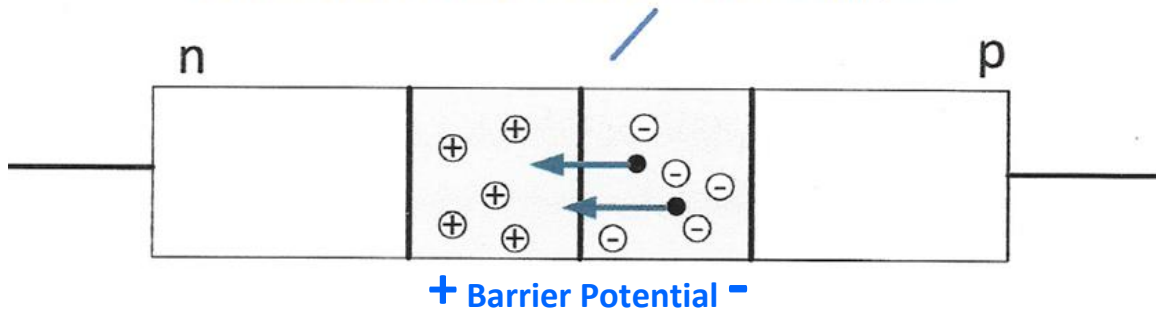
The ions locked within the depletion region produce a barrier potential. When charge carriers move under the influence of the resulting electric field, a drift current (I_{drift}) is produced. In Fig. 1-30(a) we see drift current produced by the *n*-side minority carrier holes. Fig. 1-30(b) illustrates the drift current component produced by the *p*-side minority carrier electrons.

The barrier potential electric field causes the minority carrier holes to drift away from the plus and toward the minus.



(a.)

The barrier potential electric field causes the minority carrier electrons to drift away from the minus and toward the plus.



(b.)

Figure 1-30

Figure 1-31 shows the diffusion of majority charge carriers away from charge carrier concentrations and toward the p-n junction. *Majority charge carriers produce diffusion current.*

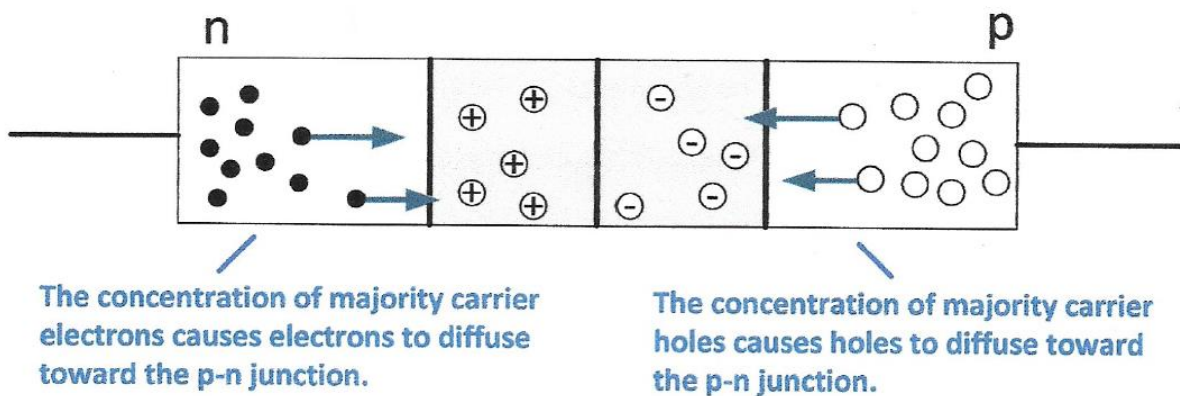


Figure 1-31

The current arrow directions for the drift current and the diffusion current are based on **conventional current** as shown in Fig. 1-32. The two current components are equal in size (since the current arrows have the same length) and opposite in direction [see Fig. 1-32(c)]. The currents cancel one another. The net result is the current through the unbiased *p-n* junction is zero. It is assumed in Fig. 1-32 that a state of thermal equilibrium exists.

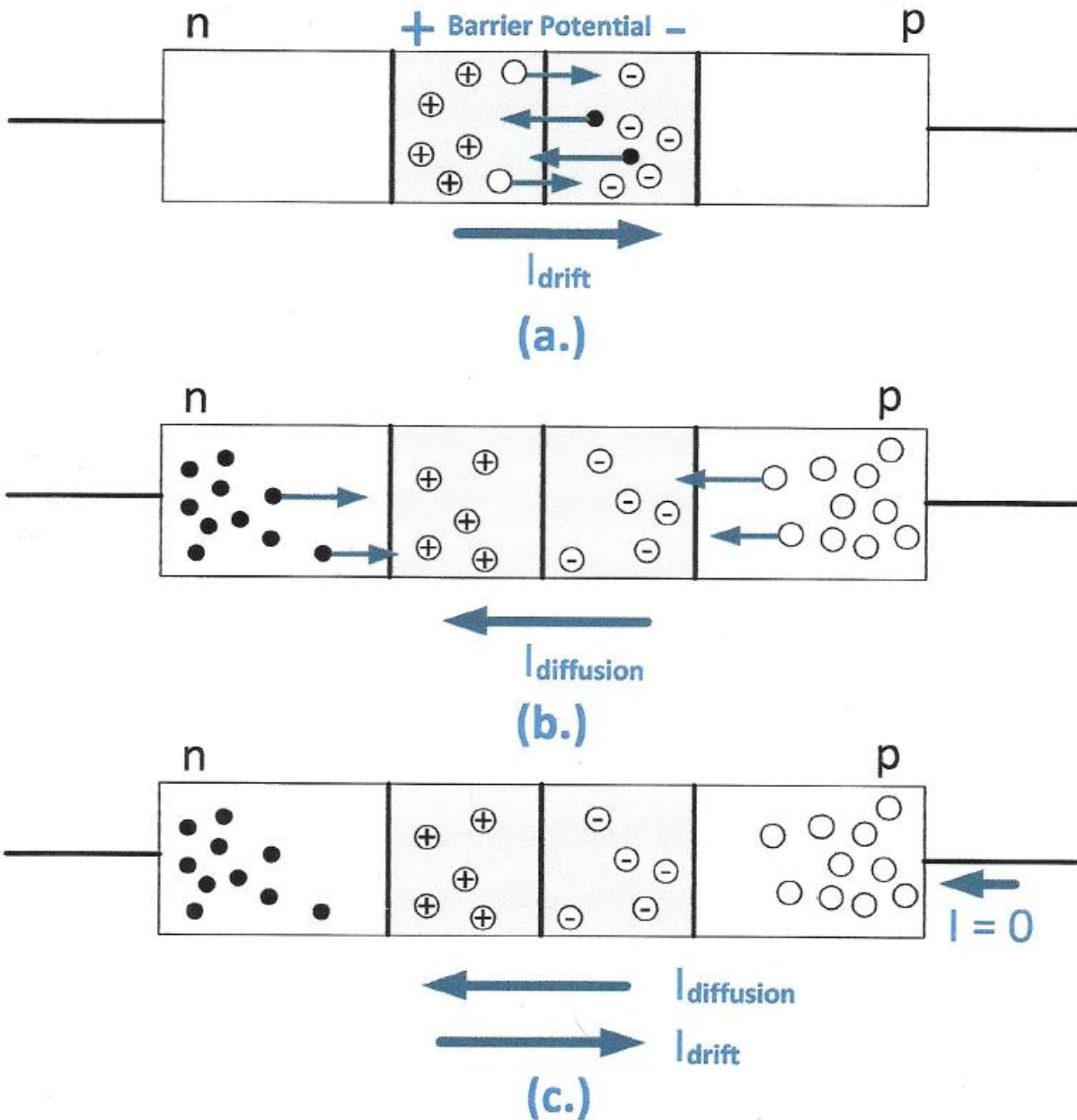


Figure 1-32

Electrons Always Seek the Lowest Energy Level

Additional insight into the characteristics of the p - n junction can be obtained by examining its associated energy diagram [see Fig. 1-33]. The band gap for the semiconductor (e.g., silicon) is the same for both the n - and p -type semiconductors. This remains true for both isolated n - and p -type materials and for n - and p -type materials that have been joined together to form a p - n junction.

Just as water always seeks the lowest level (e.g., the basement of an unwary homeowner) electrons always seek the lowest energy level. This means the high-energy conduction band electrons in the n -type material will diffuse into the p -type material and fall into holes in the valence energy band of the p -type material. This has two basic effects. Some of the upper conduction band energy levels in the n -type material will be lost and some of the lower valence energy bands of the p -type semiconductor will also be lost.

In a similar fashion some of the valence energy band electrons on the n -side of the p - n junction will diffuse into the p -side valence energy band to fall into holes. This causes some of the uppermost valence energy levels on the n -side to be lost. This also tends to remove some of the lower valence energy levels on the p -side. Because of the upward shift in the valence band energy levels on the p -side, some additional conduction energy band levels will become available.

The Energy Diagram of a P-N Junction

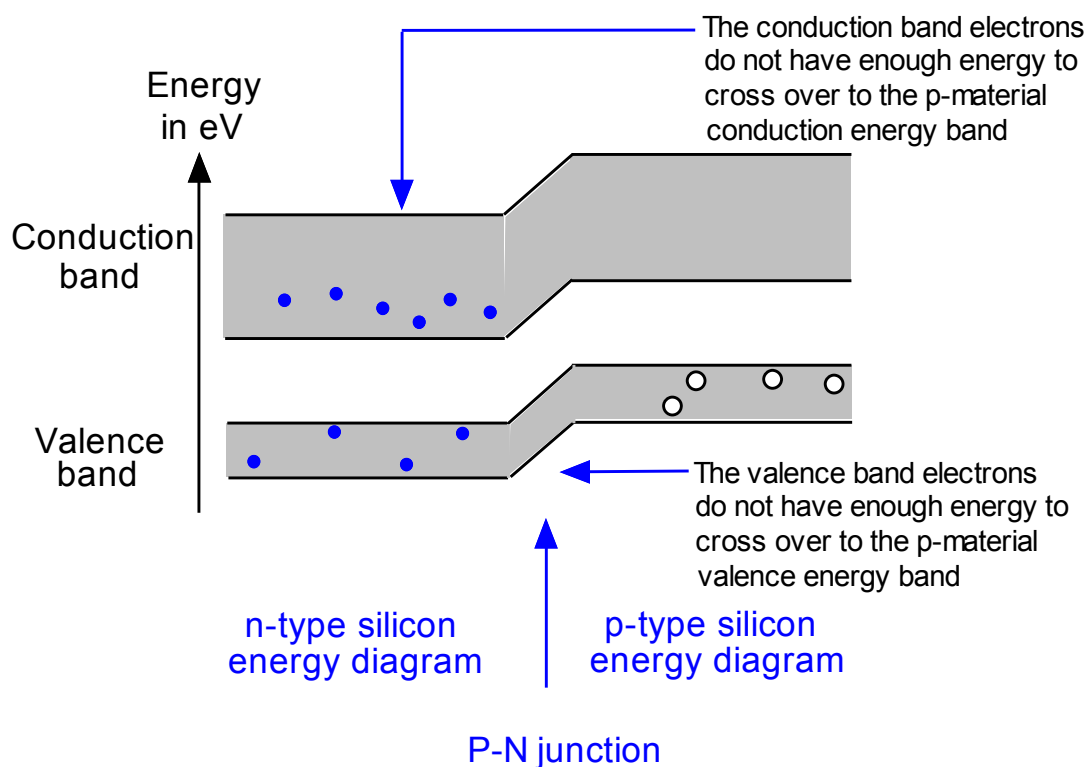


Figure 1-33

The Formation of the Barrier Potential Stops the Diffusion of the Majority Carriers Across the P-N Junction

The energy diagram of a p - n junction that has reached an equilibrium condition is given in Fig. 1-33. Note the valence and conduction energy bands for the p -type semiconductor are both higher than those for the n -type semiconductor. This means that conduction-band electrons on the n side (the majority carriers) do not have enough energy to cross the p - n junction. Further, the valence electrons on the n side also do not have enough energy to enter the p region. Consequently, the holes on the p side (the majority carriers) have too much energy to enter the n region. These conditions exist because of the formation of the barrier potential as described previously.

1-9 The Forward-Biased P-N Junction

There are two ways of applying a voltage (bias) to a p - n junction: *forward* and *reverse*. The forward bias condition is shown in Fig. 1-34. The external circuit consists of a voltage source and a current-limiting resistor in series with the p - n junction. (The p - n junction could be that in a two-terminal device called a **diode**. Diodes are introduced formally in Section 1-11.)

Our goal is to describe the charge carrier movement associated with a forward-biased p - n junction. Consequently, electron flow has been indicated in Fig. 1-34. Electrons are injected into the n -type material and extracted from the p -type material. It is important to note that forward bias occurs when the positive terminal of the voltage source connects to the p side while its negative terminal goes to the n side. **Forward bias reduces the depletion region width** [Fig. 1-34].

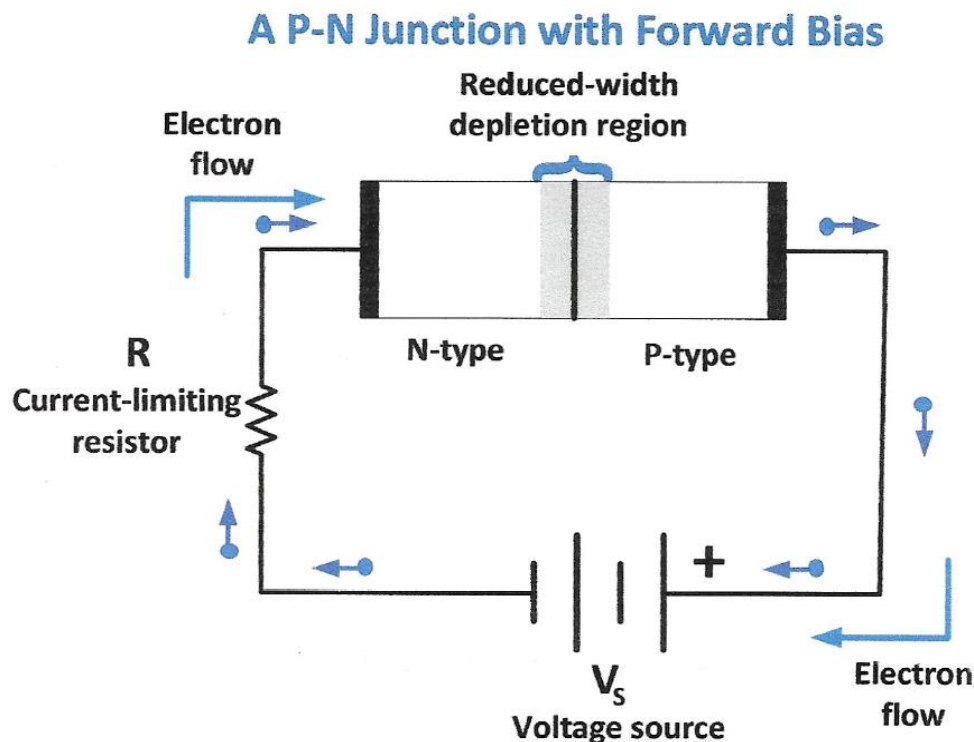


Figure 1-34

The reason why the forward bias reduces the width of the depletion region is described in Fig. 1-35. *Majority charge carrier movement into neutralizes the ions that appear at the edges of the depletion region.*

Forward Bias Reduces the Depletion Region Width

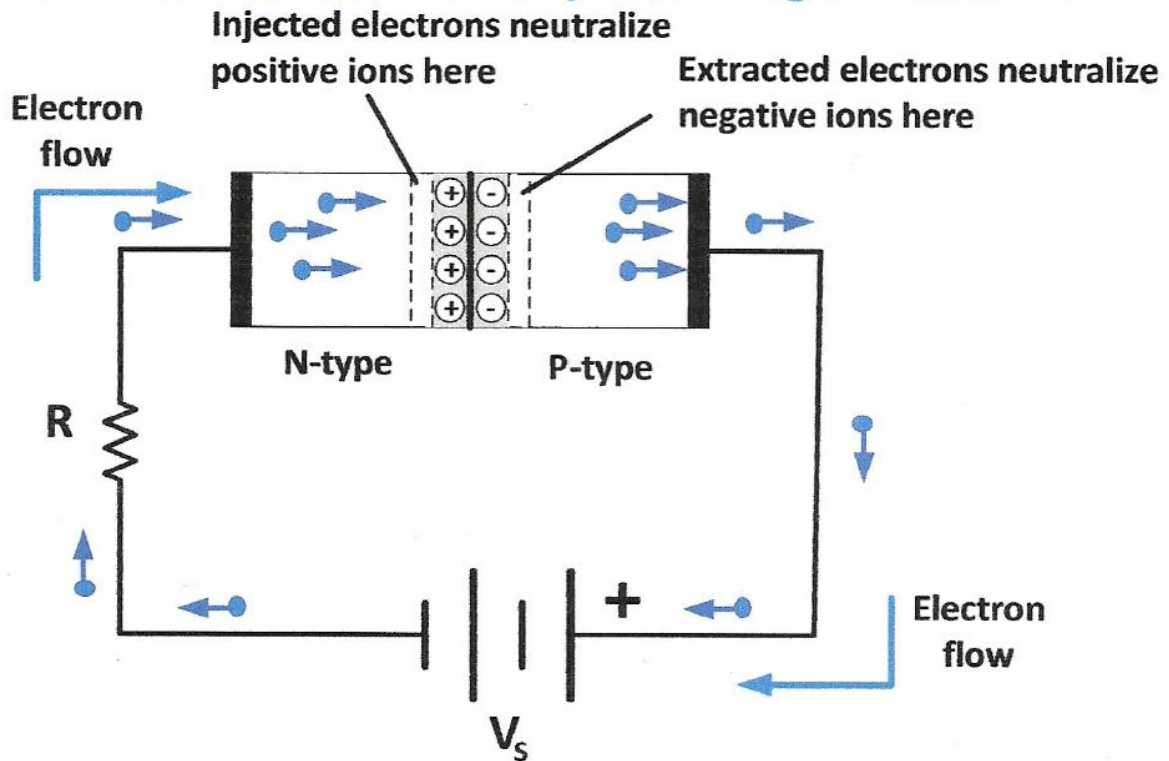


Figure 1-35

As shown in Fig. 1-36, the injected electrons in the n -type semiconductor produces a concentration of electrons that will diffuse toward the p - n junction. Similarly, extracting electrons from the p -type material will produce a concentration of holes which will also diffuse toward the p - n junction.

Majority Carriers Diffuse Toward the P-N Junction

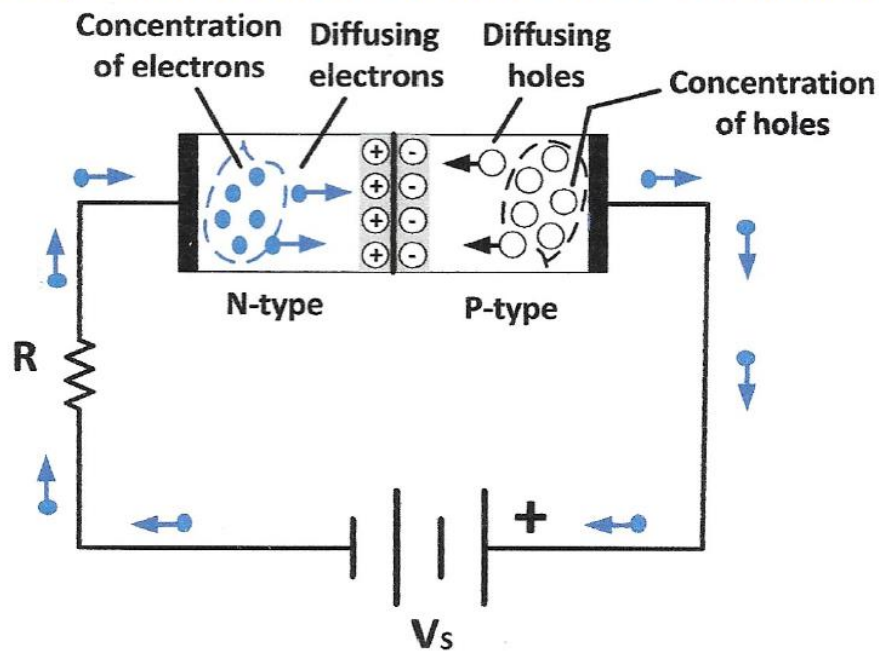


Figure 1-36

When an external DC voltage source is connected to forward bias a p-n junction, the diffusion current will increase. Forward bias reduces the depletion region width. Fewer ions means the electric field is reduced. Subsequently, *the drift current will decrease. The diffusion current will dominate. The net current through the p-n junction is due to diffusion – not drift* [see Fig. 1-37].

Diffusion is the Net Current Through the P-N Junction

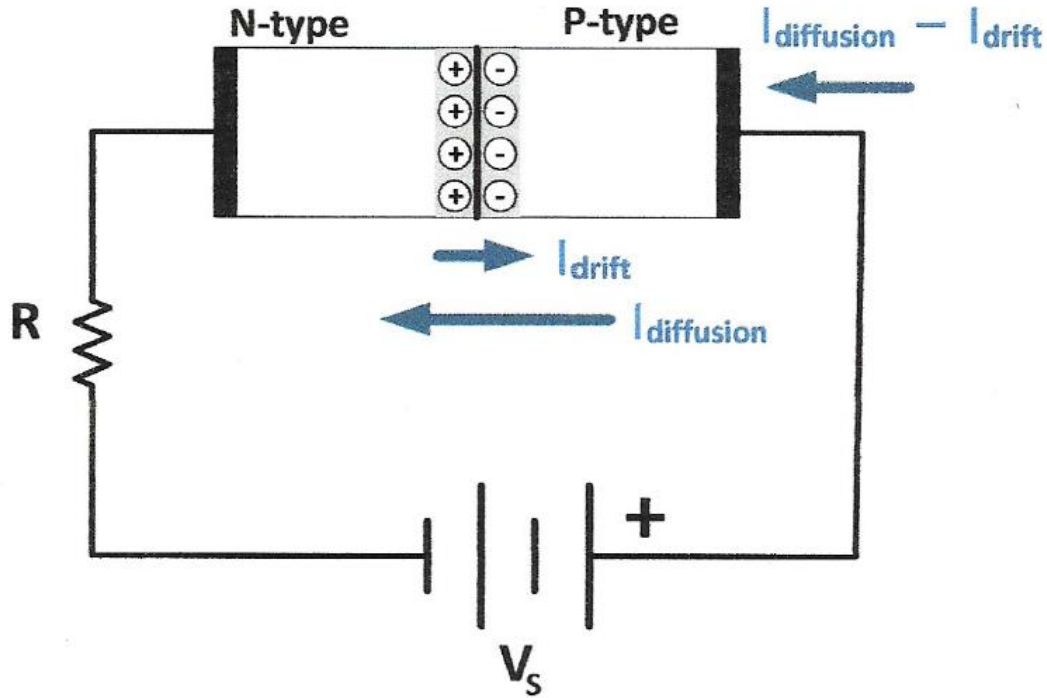


Figure 1-37

Forward-Bias Effects on the Energy Diagram

Forward bias influences the energy diagram associated with a p - n junction as shown in Fig. 1-38. Specifically, when forward bias is applied the conduction bands and the valence bands of the p - and n -type materials at the junction tend to become aligned. This means that conduction-band electrons on the n side now have enough energy to cross the p - n junction. It also means that holes can cross the p - n junction.

Careful study of the energy diagram reveals it supports our previous discussion. The conduction-band electrons are repelled by the external bias. They diffuse to the p - n junction and lose energy as they overcome the barrier potential. Their energy loss places them in the valence energy band where they recombine with holes. At the right-hand side of the energy diagram, electrons leave the valence energy band and go into the conduction energy band. This occurs because the electrons gain energy from the external applied bias.

Energy Diagram of a Forward-Biased P-N Junction

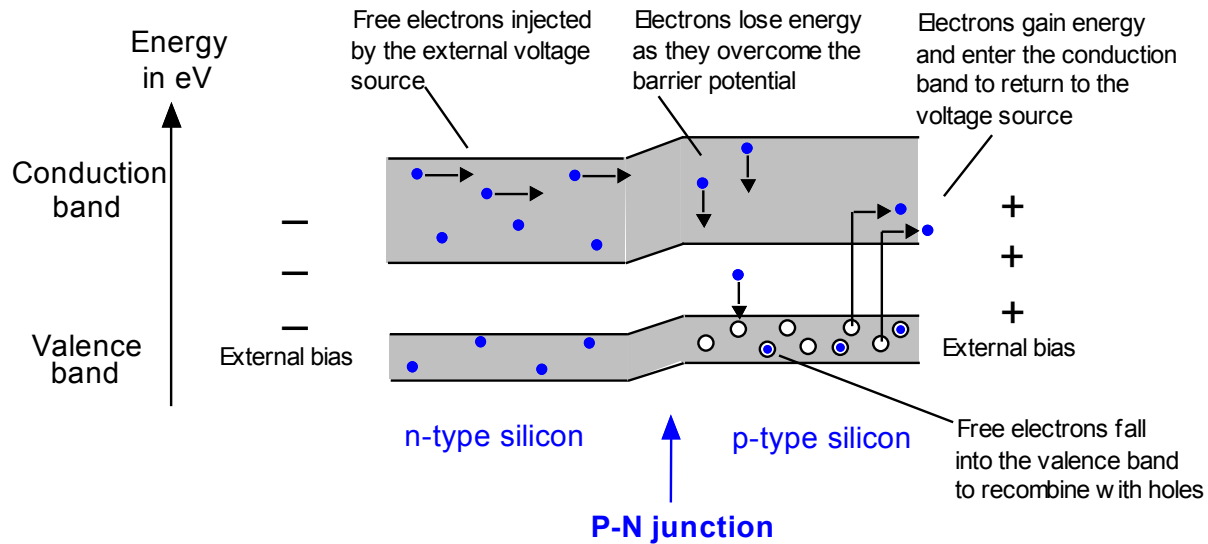


Figure 1-38

1-10 The Reverse-Biased P-N Junction

When a *p-n* junction is forward biased, the majority carriers flow through it readily. However, *when a p-n junction is reverse biased, the majority carriers will **not** flow through it.* The reverse bias condition is indicated in Fig. 1-39. Note **the n-material is now positive with respect to the p-type material.** ***The width of the depletion region is increased by the application of a reverse bias.*** Because the *n*-side is now made positive and the *p*-side is now made negative, the voltage source V_s attracts the majority carriers *away* from the *p-n* junction. Consequently, the depletion region widens. The barrier potential will increase as more and more ions are “uncovered”. The barrier potential will increase until it is equal to the magnitude of the applied reverse bias. The increase in the barrier potential means the majority carriers cannot flow through the *p-n* junction easily. Very little (ideally zero) current flows through a reverse-biased *p-n* junction. ***Because the reverse-biased p-n junction drops virtually all the applied reverse voltage and the reverse current is practically zero, the p-n junction acts like an open circuit.***

A P-N Junction with Reverse Bias

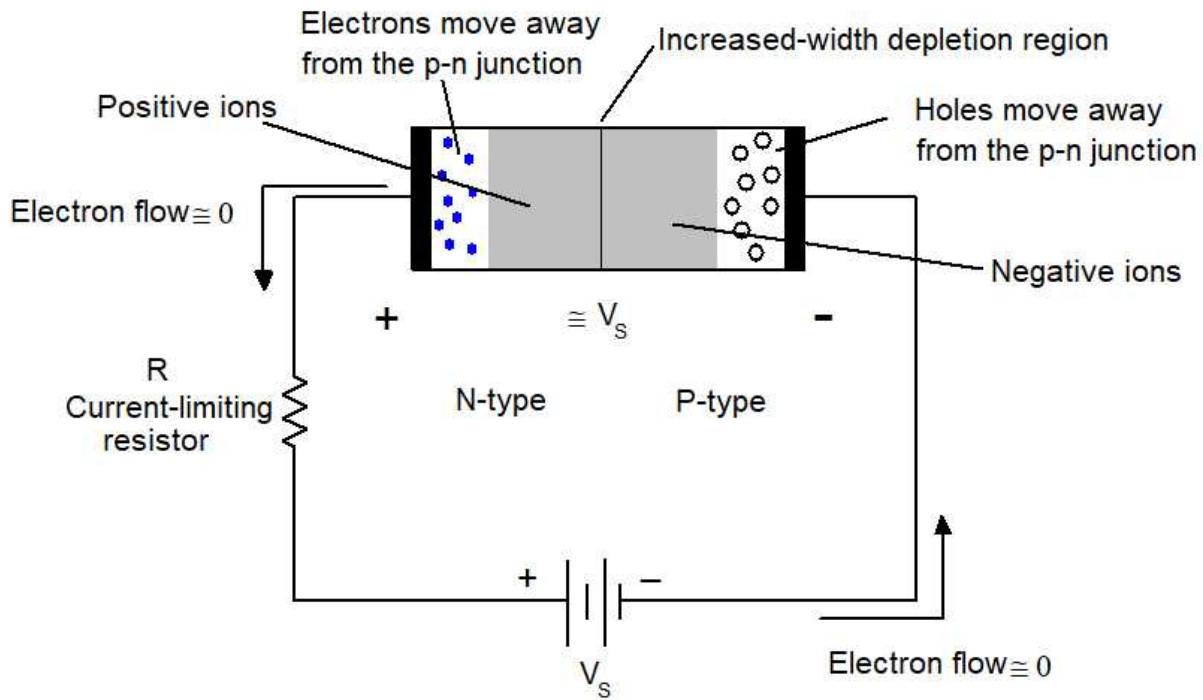


Figure 1-39

Reverse Bias Effects on the Energy Diagram

The energy diagram for the reverse-biased p - n junction is indicated in Fig. 1-40. (Contrast it with the energy diagram for forward bias in Fig. 1-38.) Reverse bias increases the barrier potential by increasing the number of ions in the depletion region. The net effect is to increase the misalignment between the conduction and valence energy bands of the n - and p -type semiconductors. The energy difference prohibits conduction-band and valence-band electrons from traveling from the n -type material to the p -type material. Recall that valence-band electrons on the n -side are required to move into the p -side to permit hole flow from the p -side into the n -side. Therefore, neither the conduction-band electrons (majority carriers) from the n -side nor holes (majority carriers) from the p -side can cross the p - n junction. The energy diagram supports the fact there will be no majority carrier movement through the p - n junction. The current will be approximately zero.

Energy Diagram of a Reverse-Biased P-N Junction

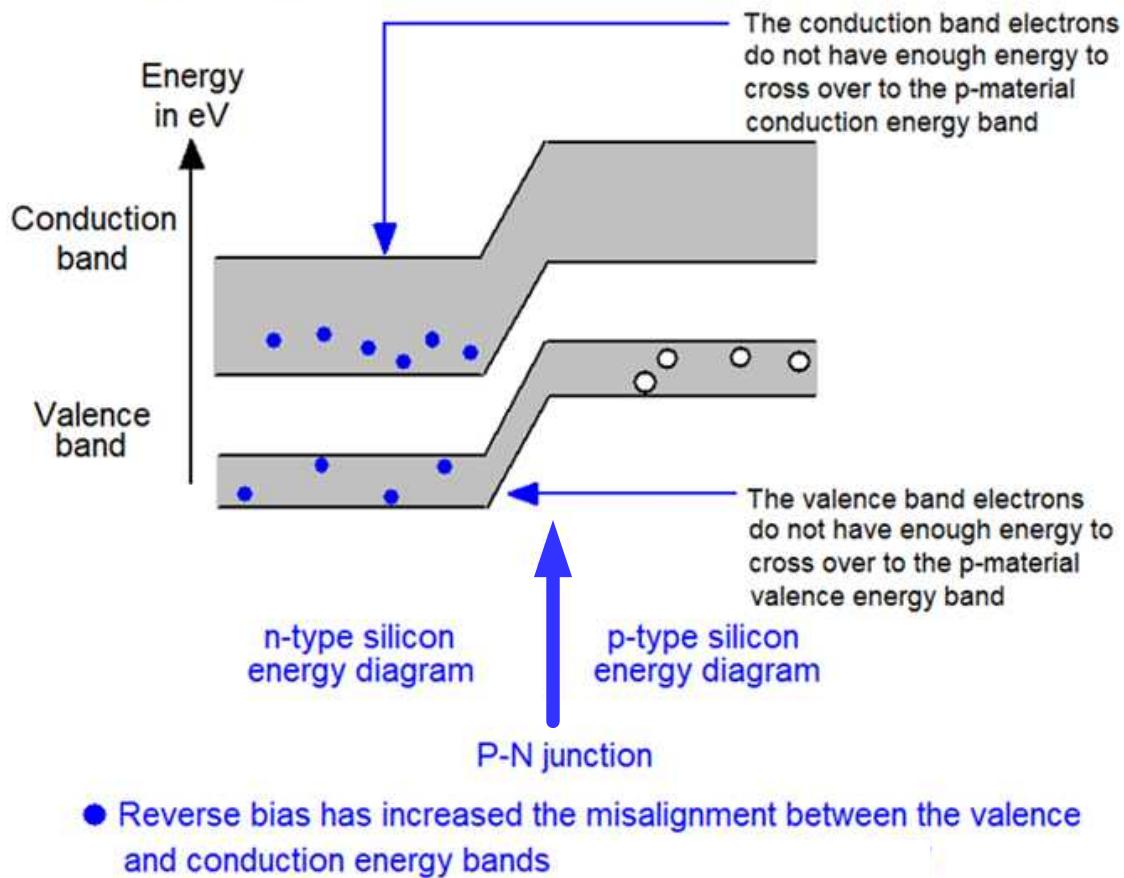


Figure 1-40

Reverse Currents

There will be a very small reverse current flow through the reverse-biased $p-n$ junction. ***This reverse current is produced by the effects of minority carriers and surface leakage.*** The minority carrier current through a reverse-biased $p-n$ junction is shown in Fig. 1-41. Recall the minority carriers in n -type semiconductors are holes and the minority carriers in p -type semiconductors are electrons. We also remind ourselves that minority carriers are produced by thermal ionization of the semiconductor atoms. Consequently, the reverse current produced by minority carriers is a strong function of temperature.

The circuit and the energy diagram are shown in Fig. 1-41. Remember: *electrons always seek the lowest energy level.* Keeping this idea in mind helps us to see the minority carriers (electrons) on the p side can easily cross the $p-n$ junction. They will lose energy, fall into the valence band on the n side, and be captured by the minority carriers (holes). At the left end of the semiconductor crystal, the valence electrons will be given enough energy by the voltage source to become free (conduction-band) electrons.

The diagram illustrates the physical structure and energy band characteristics of a P-N junction.

Top Diagram: Physical Structure and Circuit

- The junction consists of an **N-type** region (left) and a **P-type** region (right).
- A **Depletion region** is formed at the interface, containing **Positive ions** (circles with '+') and **Negative ions** (circles with '-') and free carriers.
- The built-in potential across the depletion region is denoted as V_s .
- An external circuit is connected, including a battery with voltage V_s and a resistor R .
- Electron flow** is indicated by arrows:
 - From the P-region, through the wire and resistor, to the N-region (labeled ⑥).
 - From the N-region, through the depletion region, to the P-region (labeled ①).

Bottom Diagram: Energy Band Diagram

- The vertical axis represents **Energy in eV**.
- The **Conduction band** and **Valence band** are shown for both materials.
- The **n-type silicon energy diagram** shows a higher conduction band and lower valence band compared to the **p-type silicon energy diagram**.
- A blue arrow points from the n-type conduction band to the p-type conduction band, indicating that **minority carrier conduction-band electrons have enough energy to cross over to the p-material conduction energy band**.

P-N junction

The numbers indicated in Fig. 1-41 are keyed to the points listed below.

- 42 SOLID-STATE PHYSICS AND THE
- P-N*
- JUNCTION

5. At the left side of the crystal, the electrons receive enough energy from the voltage source to be elevated to the conduction band.
6. The free electrons return to the positive terminal of the voltage source V_S .

Reverse Saturation Current

The reverse current produced by the minority carriers is essentially independent of the magnitude of the reverse voltage. This means that since the current depends solely on the number of available minority carriers, *increasing the reverse bias voltage will not cause it to increase*. Consequently, it is called the **reverse saturation current**¹¹. It is often indicated by the symbol I_S . Again, because it depends on minority carriers, it is very dependent on temperature. Specifically, *as temperature increases, the reverse saturation current will increase*.

Surface Leakage Current

Imperfections in the (otherwise orderly) crystalline structure of a semiconductor tend to promote recombinations. Recombination occurs when an electron drops into a hole. The surface of a semiconductor crystal creates imperfections since there are no atoms outside the crystal to form covalent bonds [see Fig. 1-42]. As can be seen in the figure, holes are formed on the surface of the semiconductor. Surface leakage current (denoted I_{SL}) occurs because the electrons can jump from hole to hole.

How the Surface Leakage Current is Formed

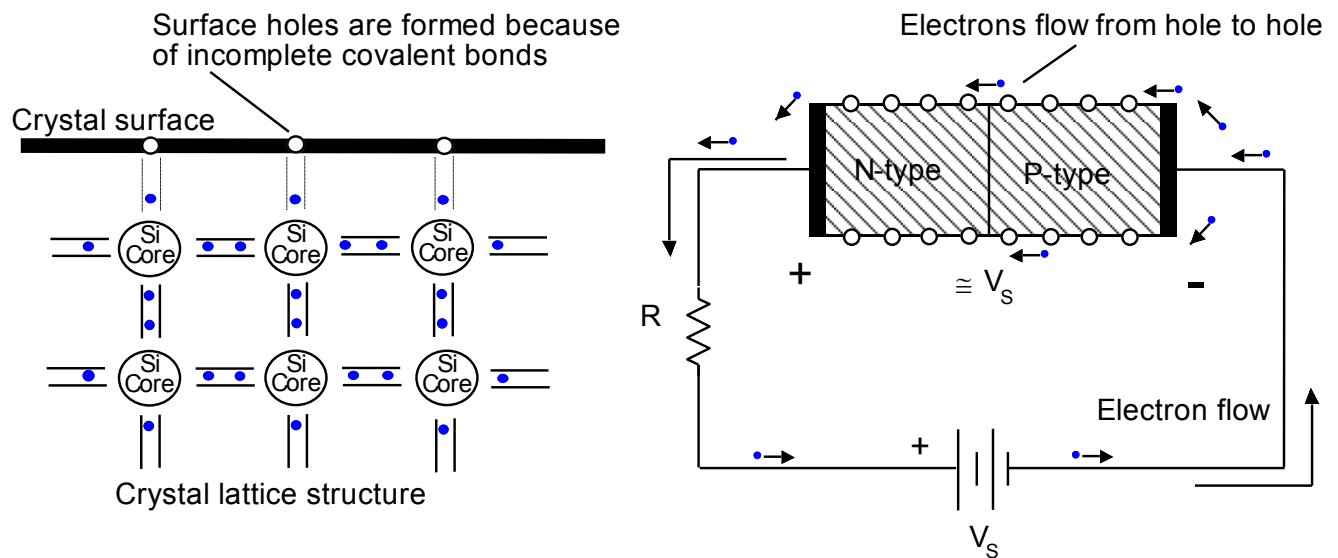


Figure 1-42

Surface leakage current is not a function of temperature. However, surface leakage current does tend to increase as the applied reverse voltage is increased.

¹¹ Saturation is the state or process that occurs when no more of something can be absorbed, combined with, or added. In this case, all the thermally produced minority carriers are used to support the reverse current.

The Total Reverse Current I_R

The total reverse current is denoted as I_R and is the sum of the reverse saturation current I_S and the surface leakage current I_{SL} .

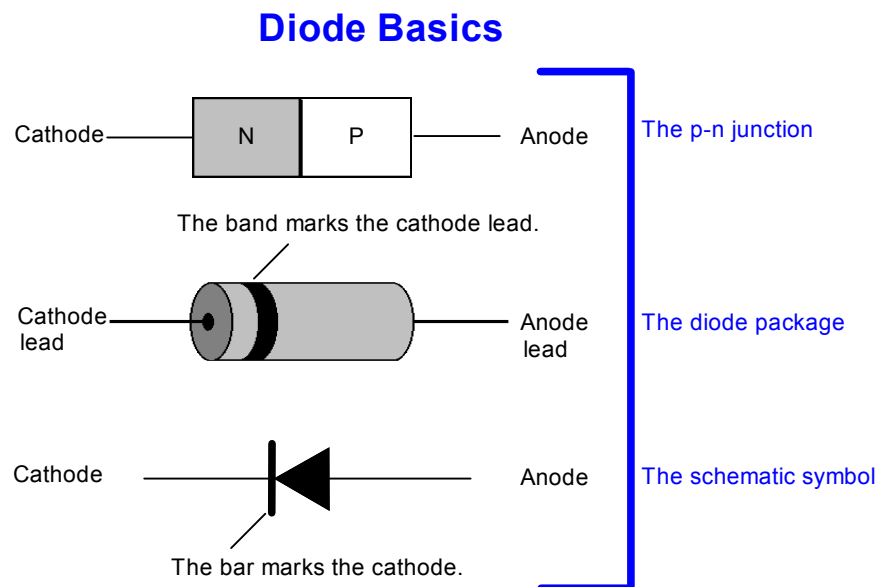
$$I_R = I_S + I_{SL} \quad (1-3)$$

The total reverse current specification is often provided by diode manufacturers on their data sheets. What are “diodes”? Read the next section!

1-11 The Diode

Perhaps the simplest solid-state device is the **diode**. It is detailed in Fig. 1-43. The diode incorporates a single *p-n* junction. Its **cathode** terminal is connected to the *n*-type material while its **anode** is connected to its *p*-type material. The diode’s schematic symbol employs a bar to indicate its cathode terminal. ***The arrow indicates the direction conventional current will pass through the diode when it is forward biased. Under this condition, the diode can be thought of as acting like a closed switch. The diode will act like an open circuit when conventional current is directed against the arrow since this means that the diode is reverse biased.*** Much more will be said about the diode’s operation as our work progresses. The band on the diode’s physical package is used to identify its cathode terminal.

Diodes are used as rectifiers in DC power supplies and as diode OR circuits in the battery-back-up systems found in digital clocks and personal computers. Small-signal diodes appear in limiting and clamping circuits. Rectifier and small-signal diodes are used extensively in electronic circuit designs. They will be explored completely in our later endeavors.



Problems for Chapter 1

Section 1-1

- 1-1. List the eight fundamental sources of energy using the COMETMAN mnemonic.
- 1-2. What is a *transducer*? Give two examples and explain them briefly.
- 1-3. Is a loudspeaker a transducer? What is its energy input? What is its primary output energy?

Section 1-2

- 1-4. A *positive ion* has more _____ (electrons, protons) than _____ (electrons, protons).
- 1-5. A *negative ion* has more _____ (electrons, protons) than _____ (electrons, protons).
- 1-6. The best electrical conductors have a valence of _____ (1,2,3,4,5).
- 1-7. Name the three (3) basic types of atomic bonding. Which type of bonding occurs in electrical conductors?
- 1-8. Orbital electrons that *gain* energy will tend to have a (an) _____ (increased, decreased) orbital radius.
- 1-9. Orbital electrons that *lose* energy will tend to have a (an) _____ (increased, decreased) orbital radius.
- 1-10. Name three typical *forms* of energy an electron emits as it falls.
- 1-11. What is a *crystal*?
- 1-12. What are *energy bands*? Why are they formed?
- 1-13. What is an *electron volt (eV)*? Explain.
- 1-14. Define the term *band gap*
- 1-15. *Electrical conductors* have a band gap of _____ (0 eV, < 5 eV, >5 eV)
- 1-16. *Electrical insulators* have a band gap of _____ (0 eV, < 5 eV, >5 eV)
- 1-17. *Semiconductors* have a band gap of _____ (0 eV, < 5 eV, >5 eV)

- 1-18. Silicon Dioxide (SiO_2) has a band gap of _____ which makes it a(n) _____ (conductor, semiconductor, insulator).

Section 1-3

- 1-19. *Semiconductors* (like silicon and germanium) are _____ (trivalent, tetravalent, pentavalent).
- 1-20. _____ semiconductors are being used to manufacture extremely high-speed electronic devices. (a) silicon, (b) gallium arsenide, (c) silicon-germanium compounds, (d) silicon carbide, (e) Both (a) and (b), (f) Both (b) and (c).
- 1-21. _____ (Germanium, Gallium arsenide, Silicon carbide) is a relatively new semiconductor material that performs well at very high temperatures.
- 1-22. Blue light-emitting diodes (LEDs) are made using a _____ (indium gallium nitride, gallium phosphide, silicon-germanium) semiconductor.

Section 1-4

- 1-23. *Pure* semiconductors are described as being _____ (extrinsic, intrinsic).
- 1-24. Explain what is meant by the term *crystal lattice*.
- 1-25. Semiconductor atoms such as silicon and germanium form _____ (covalent, ionic, metallic, both covalent and ionic) bonds when a crystal lattice structure is formed.
- 1-26. Semiconductor compounds such as gallium arsenide and gallium phosphide form _____ (covalent, ionic, metallic, both covalent and ionic) bonds when a crystal lattice structure is formed.
- 1-27. Explain why the energy band gaps associated with the gallium compounds tend to be greater than the energy band gaps associated with silicon.

Section 1-5

- 1-28. A pure semiconductor has an equal number of holes and electrons. If a semiconductor electron is to become free, the electron _____ (a) must receive enough energy to break its covalent bond, (b) must receive enough energy to jump the band gap between the valence and conduction bands, (c) must be repulsed by the nucleus, (d) both (a) and (b), (e) none of the choices.
- 1-29. In a pure semiconductor, holes _____ (a) are positive charges, (b) act like positive charges, (c) are broken covalent bonds, (d) both (b) and (c), (e) none of the choices.

- 1-30. Hole movement results from the movement of _____ (valence, free) electrons.
- 1-31. Under the influence of an applied (external) electric field valence- and conduction-band electrons tend to move in the _____ (opposite, same) direction.

Section 1-6

- 1-32. *Doped* semiconductors contain impurities and are said to be _____ (extrinsic, intrinsic).
- 1-33. *Acceptor* impurities are _____ (trivalent, tetravalent, pentavalent) and are used to make _____ (*p*-, *n*-) type semiconductors.
- 1-34. Each acceptor impurity used to replace one semiconductor atom produces _____ (one, two, three, four) hole(s).
- 1-35. *Donor* impurities are _____ (trivalent, tetravalent, pentavalent) and are used to make _____ (*p*-, *n*-) type semiconductors.
- 1-36. In a *p-type semiconductor* _____ (holes, electrons) are the *majority* carriers and _____ (holes, electrons) are the *minority* carriers.
- 1-37. In an *n-type semiconductor* _____ (holes, electrons) are the *majority* carriers and _____ (holes, electrons) are the *minority* carriers.
- 1-38. As the *temperature* of a semiconductor *increases*, the number of *minority* carriers _____ (increases, decreases).

Section 1-7

- 1-39. Why are some semiconductors called “organic”?
- 1-40. What is an “allotrope”?
- 1-41. What are the two allotropes of silicon?
- 1-42. Silicon is _____ (organic, inorganic).
- 1-43. _____ (amorphous, crystalline) silicon is used to make integrated circuits.
- 1-44. _____ (amorphous, crystalline) silicon is used to make low-cost solar cells.

- 1-45. Name the two *basic* allotropes of carbon.
- 1-46. Graphene is derived from _____ and carbon nanotubes are derived from _____.
- 1-47. Graphene is _____ (thin, thick), a _____ (excellent, poor) electrical and thermal conductor, and is rather _____ (weak, strong).
- 1-48. Name the three arrangements of single-walled carbon nanotubes. Which arrangements can be used as semiconductors?

Section 1-8

- 1-49. Explain what is meant by the term *diffusion*.
- 1-50. When a *p-n* junction is formed what stops the diffusion process?
- 1-51. What causes the *barrier potential* which forms at the *p-n* junction? List the typical barrier potential values for *p-n* junctions made from germanium, silicon, and the gallium compounds.
- 1-52. What is the *depletion region* that forms at a *p-n* junction?
- 1-53. In the depletion region _____ (positive, negative) ions exist on the p side and _____ (positive, negative) ions exist on the n side.
- 1-54. Once the barrier potential has formed, the only way majority carriers can cross the *p-n* junction is for them to _____ (lose, gain) energy.
- 1-55. Explain why the *n* and *p* regions around the *p-n* junction tend to be electrically neutral.
- 1-56. What is drift current?
- 1-57. What is diffusion current?
- 1-58. When a *p-n* junction is formed, what causes the diffusion of the charge carriers across the junction to cease?

Section 1-9

- 1-59. What is the general rule for applying a forward bias to a *p-n* junction?

- 1-60. Forward bias results in the movement of _____ (majority, minority) carriers across the p - n junction.
- 1-61. Explain what is meant by the term *recombination*.
- 1-62. Forward bias causes the majority carriers to move _____ (toward, away from) the p - n junction.
- 1-63. Forward bias _____ (increases, decreases) the depletion region width.
- 1-64. A forward-biased p - n junction demonstrates a _____ (large, small) resistance.

Section 1-10

- 1-65. Reverse bias causes the majority carriers to move _____ (toward, away from) the p - n junction.
- 1-66. Reverse bias _____ (increases, decreases) the depletion region width.
- 1-67. A reverse-biased p - n junction demonstrates a _____ (large, small) resistance.
- 1-68. The *ideal reverse current* is _____ (large, small, zero).
- 1-69. _____ (Reverse saturation, Surface leakage) current is a strong function of temperature.
- 1-70. _____ (Reverse saturation, Surface leakage) current is a strong function of the applied reverse voltage.
- 1-71. A reverse-biased p - n junction has a reverse saturation current (I_S) of 3 nA and a surface leakage current (I_{SL}) of 0.5 nA. What is its total reverse current I_R ?
- 1-72. A reverse-biased p - n junction has a reverse saturation current (I_S) of 10 nA and a surface leakage current (I_{SL}) of 1.5 nA. What is its total reverse current I_R ?

Section 1-11

- 1-73. The band on the diode package marks the _____ (anode, cathode) terminal.
- 1-74. The bar on the diode schematic symbol marks the _____ (anode, cathode) terminal.

- 1-75. The anode terminal of the diode connects to the _____ (n -, p -) type semiconductor.
- 1-76 A diode is forward biased when its _____ (anode, cathode) terminal is more positive than its _____ (anode, cathode) terminal.

2

Diodes and Circuit Analysis

Diodes are two-terminal solid-state devices. Unlike the ideal resistors, capacitors, and inductors studied in introductory circuit analysis, diodes are *non-linear* circuit elements. This is precisely the characteristic that makes the diodes so useful. However, because they are non-linear, we must develop some new circuit analysis tools. In this chapter we study the analysis techniques, and introduce the rectifier, zener, and avalanche diodes. We also see how to apply Thevenin's theorem to solve diode circuit problems. The specific topics covered include

- The Diode V - I Characteristic Curve¹²
- The Shockley Diode Equation and the DC Load Line
- The Ideal Diode Model
- The Knee-Voltage Diode Model
- The Reverse Current Source Diode Model
- Zener and Avalanche Diodes
- The Ideal Zener Diode Model
- Static and Dynamic Resistance
- The Zener Dynamic-Resistance Diode Model
- Using Thevenin's Theorem

2-0 Study Objectives

After completing this chapter, you should be able to:

- Understand reference directions and the interpretation of a diode's V - I curve.
- Know the definition of knee voltage and remember the typical values for silicon, germanium, and gallium compound diodes.
- Explain the operation of diode test circuits for forward and reverse bias.
- Describe the operation of the circuit required to generate a diode's V - I curve dynamically.
- Use Electronic Design Automation (e.g., Multisim) to generate a V - I curve.
- Use the Shockley diode equation to generate a V - I curve.

¹² The x-y plane is taught in basic mathematics courses where x is the independent (horizontal-axis) variable and y is the dependent (vertical-axis) variable. Similarly, two-dimensional graphs of the characteristics of electronic devices are placed with the independent variable voltage (V) on the horizontal axis with the resulting (dependent) variable current (I) placed on the vertical axis. The result is a **V - I characteristic curve graphed on the V - I plane**. Several industry and academic professionals prefer to use the term **I-V characteristic**. *The V - I characteristic nomenclature is used in this book.*

- Draw a DC load line for a forward-biased diode.
- Use the ideal diode model to find the Q-point.
- Employ the knee-voltage diode model to find the Q-point.
- Define the terms static and dynamic resistance.
- Use the dynamic resistance diode model to find the Q-point.
- Explain and use the reverse current source diode model.
- Describe the operation of zener and avalanche diodes.
- Use the ideal and dynamic resistance zener diode models to find the Q-point.
- Interpret a zener diode data sheet to obtain the dynamic resistance diode model parameters.
- Apply Thevenin's theorem to simplify diode circuits.
- Use Multisim to analyze a zener diode circuit using the 1N4733A zener diode.

2-1 The Diode V-I Characteristic Curve

Solid-state diodes are highly non-linear. The non-linearity is a direct result of the barrier potential that forms at the p - n junction. This non-linearity means the resistance of a diode is *not* constant. In the case of the rectifier or small-signal diodes, *their resistance will decrease as their forward bias increases*. (This will be demonstrated later.) The easiest way to describe the operation of a non-linear device is to show its ***V-I characteristic curve***. A V - I characteristic curve indicates the relationship of the voltage across a device to the corresponding current through it. Recall there are two ways to bias a diode - forward and reverse. It is customary to show forward bias in the first quadrant and reverse bias in the third quadrant. This is because of the ***reference directions*** defined in Fig. 2-1.

A Diode's Forward-Bias V-I Characteristic Curve Shows How a Diode Behaves

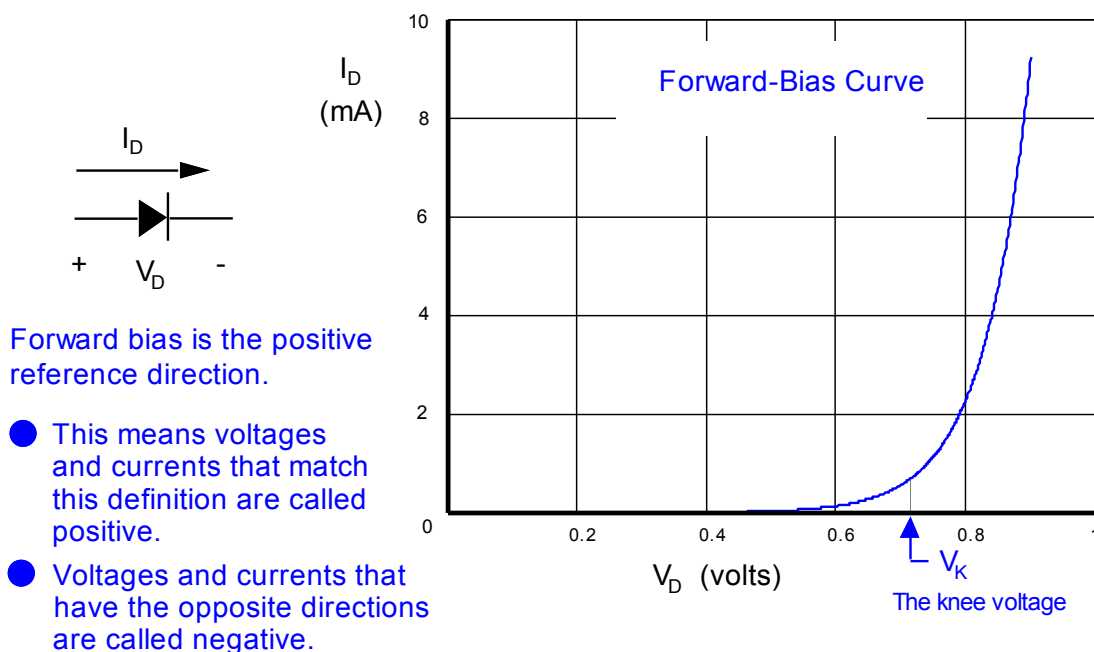


Figure 2-1.

The Knee Voltage (V_K)

When a diode is forward biased, significant current will not flow until the barrier potential is overcome. This means the available forward bias voltage must be greater than 0.7 V in the case of a silicon diode. Hence, when a significant¹³ forward current flows through the diode, the diode's voltage drop will be approximately equal to the barrier potential. This is called the **knee voltage** (V_K) and has been labeled on the forward V - I curve shown in Fig. 2-1. Observe the diode's forward current increases dramatically once V_K is exceeded. Small increases in the forward voltage drop beyond V_K can produce large increases in the diode current. The V_K for germanium diodes is taken to be 0.3 V. The V_K for the gallium compounds can range from 1.2 to 1.8 V. We shall use a nominal value of 1.6 V for gallium devices. The various knee voltages are summarized in Table 2-1.

Table 2-1. Diode Knee Voltages

Diode Material	Knee Voltage (V_K)
Germanium	0.3 V
Silicon	0.7 V
Gallium	1.6 V

¹³ Admittedly, a *significant* current is tough to define. Consequently, some engineers and technicians use 0.6 V as the knee voltage of a silicon diode.

The Reverse Current (I_R)

When a diode is forward biased its anode is more positive than its cathode. Therefore, conventional current flows in the direction of the arrow used for the diode's schematic symbol. *When a diode is reverse-biased its cathode is positive relative to its anode.* Therefore, under the condition of reverse bias, conventional current is attempting to flow *against* the diode's arrow. A small reverse current will flow from the cathode to the anode [see Fig. 2-2]. The reverse current is labeled I_R as indicated in Fig. 2-2. *Since the reverse voltage and current have directions opposite those for forward bias, they are called negative.* The reverse characteristics are plotted in the third quadrant of the V - I plane where both the vertical and horizontal axes represent negative values. Note the scales for the reverse-bias region (current in nA) are different than those for the forward-bias region (current in mA). The voltage scales are also different. This makes it easier to examine the V - I curves.

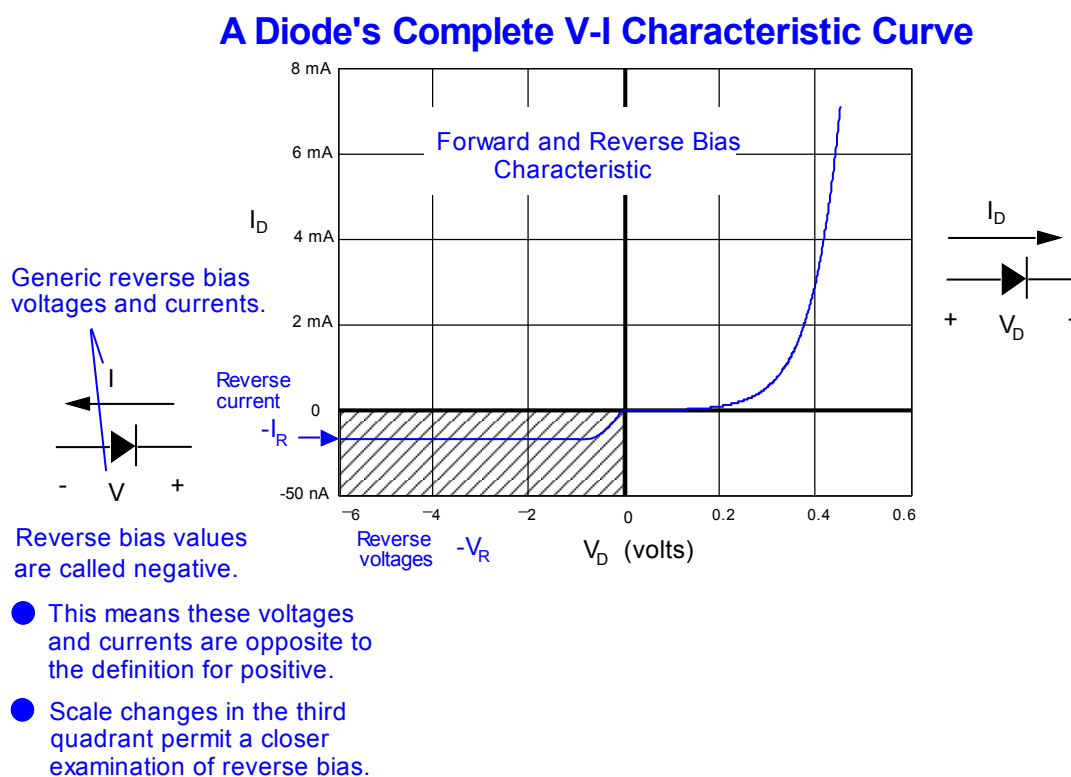


Figure 2-2.

A Forward-Bias Test Circuit

A circuit that can be used to produce the data points in a V - I curve is given in Fig. 2-3. In the forward-bias circuit, the resistor (R_I) is used to limit the maximum current through the diode. By applying Kirchhoff's Voltage Law (KVL) and Ohm's law we may obtain an equation for the diode's current I_D . A KVL equation is developed by starting at the negative terminal of V_S and working clockwise around the loop. Solving for I_D leads us to Eq. 2-1.

$$-V_S + I_D R_I + V_D = 0$$

$$I_D = \frac{V_S - V_D}{R_1} \quad (2-1)$$

Consider Example 2-1.

Example 2-1. The adjustable dc power supply (V_S) in Fig. 2-3 is set to 40 V. The voltage across the diode voltage (V_D) is 0.8 V. Find the diode's forward current I_D .

Solution: Applying Eq. 2-1 and using the value of R_1 given in Fig. 2-3, we obtain the results below.

$$I_D = \frac{V_S - V_D}{R_1} = \frac{40 \text{ V} - 0.8 \text{ V}}{1 \text{ k}\Omega} = 39.2 \text{ mA}$$

A Diode Test Circuit - Forward Bias

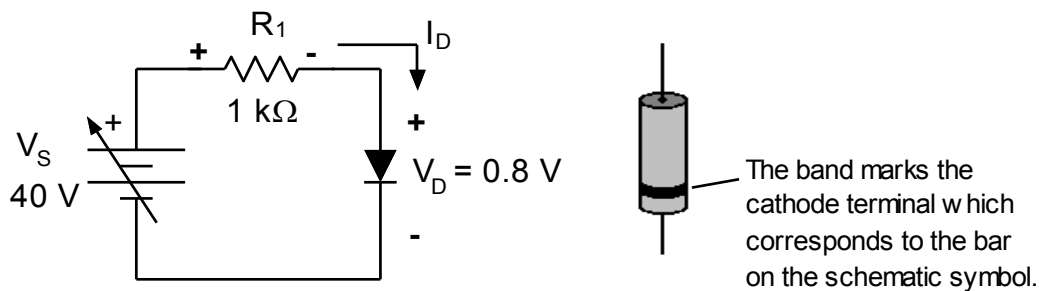


Figure 2-3.

It should be clear that if the adjustable power supply voltage is lowered to 35 volts, the diode's current will be reduced. This will result in a reduced voltage across the diode. (As an example, the reader should verify that if V_S is 35 V, and V_D is 0.78 V, then I_D becomes 34.2 mA.) By taking several data points, it is possible to graph the diode's forward V - I characteristic curve.

If we were to construct the test circuit shown in Fig. 2-3, the resistance of R_1 should be measured. Alternatively, a precision resistor (e.g., a 1%-tolerance unit) should be used. This will permit us to *sense* the current through the diode by measuring the voltage drop across R_1 and applying Ohm's law.

A Reverse-Bias Test Circuit

The test circuit shown in Fig. 2-4 can be used to obtain the V - I curve data for a reverse-biased diode. Since a reverse-biased diode passes an extremely small current, a current-limiting resistance may not be necessary. However, a large (precision or measured) resistor can be used to sense the current through the diode. (Again, we measure the voltage drop across it and apply Ohm's law.) The diode has been reversed such that its cathode is now positive relative to its anode. Also, note **the reverse voltage is called V_R and the reverse current I_R** . This notation is consistent with that used by diode manufacturers on their data sheets. (Do **not** confuse V_R with the notation for the voltage drop across the resistor V_{R1} .)

The diode's reverse current can be found by applying Kirchhoff's voltage law and Ohm's law. Except for a minor change in notation, the resulting equation is identical to Eq. 2-1.

$$-V_S + I_R R_1 + V_R = 0$$

$$I_R = \frac{V_S - V_R}{R_1} \quad (2-2)$$

Now consider Example 2-2.

A Diode Test Circuit - Reverse Bias

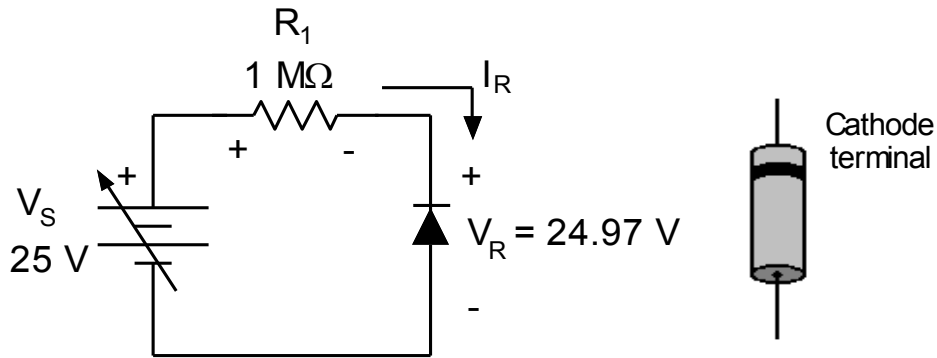


Figure 2-4.

Example 2-2. The adjustable DC power supply (V_S) in Fig. 2-4 is set to 25 V. The diode reverse voltage (V_R) is 24.97 V. Find the diode's reverse current I_R .

Solution: Applying Eq. 2-2 and using the value of R_1 given in Fig. 2-3, we obtain the results below.

$$I_R = \frac{V_S - V_R}{R_1} = \frac{25 \text{ V} - 24.97 \text{ V}}{1 \text{ M}\Omega} = 30 \text{ nA}$$

If we adjust the reverse voltage (V_R) to different values (e.g., 5, 10, 15, 20, and 25 volts) we can then measure the corresponding reverse current (I_R) values. Once this is done, we can again plot the diode's V - I characteristic curve. V_R and I_R are *positive* quantities as indicated in Fig. 2-4. However, they are *negative* when I_D and V_D are taken as the reference [see Fig. 2-2].

Using EDA to Produce the V-I Curve

Electronic Design Automation (EDA) refers to the extensive use of computer software tools to draw electronic schematic diagrams (perform schematic capture), simulate the resulting circuits, optimize the design, create a printed circuit board layout, generate a Bill of Materials (BOM) and document the entire process. **Multisim** is produced by a company called **National Instruments (NI)** and is one of the many software tools available in the EDA arena. NI offers a reasonably sophisticated software package at a very competitive price. Many high-end EDA systems are also available but may cost thousands of dollars.

Let's see how to use Multisim. We begin by running the program. If an icon (Fig. 2-5) is on your desktop, **double click on it and the program will run**. (If you have Windows 10, you can use Cortana to search and find the Multisim Application.)

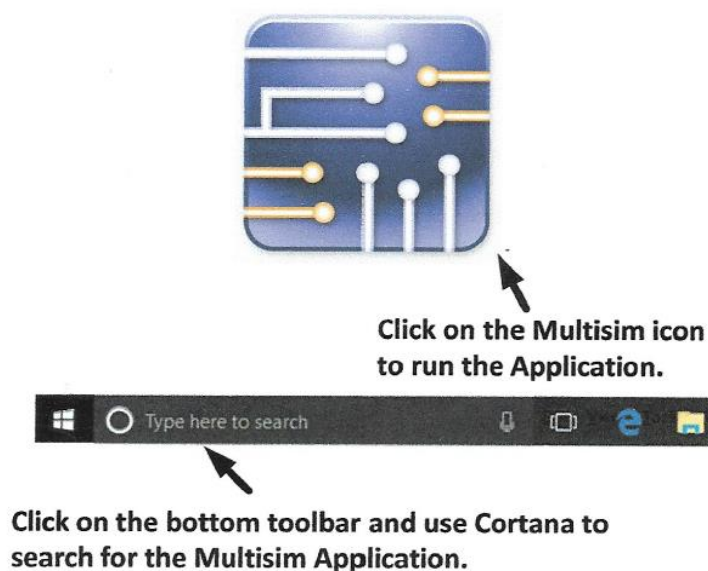


Figure 2-5.

Once Multisim has started, it will take you to a blank page as illustrated in Fig. 2-6.

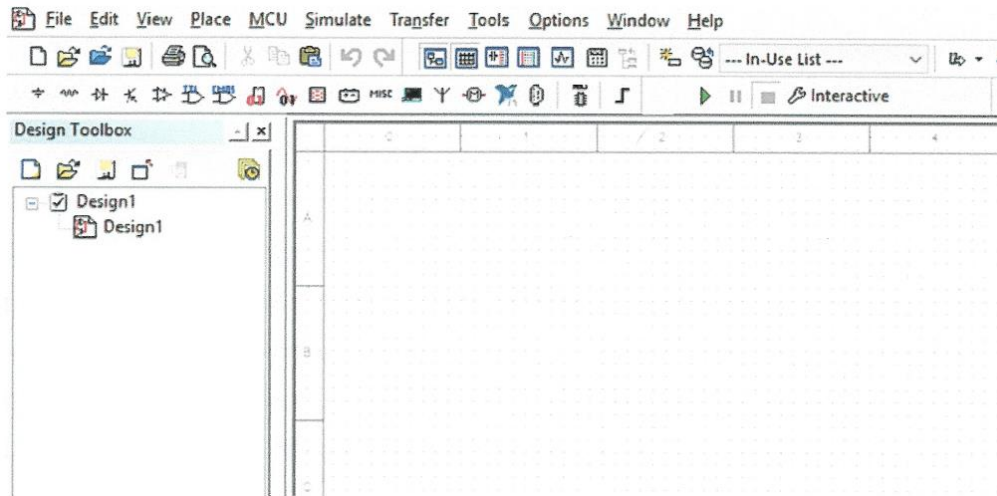


Figure 2-6.

We need to add components. We click on **Place** and then select **Component** in the drop-down menu shown in Fig. 2-7.

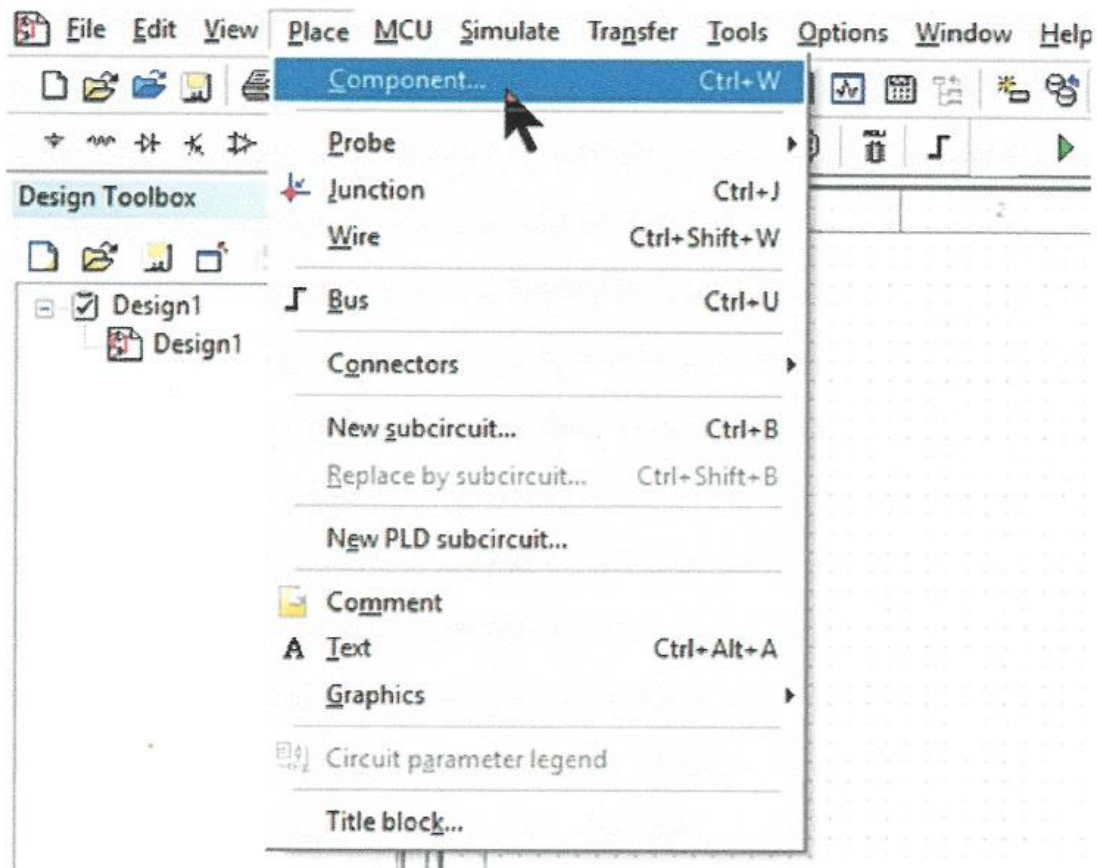


Figure 2-7.

Use the drop-down menu in **Group** and select **Sources**. Next select **Power Sources**. Add a **DC power (voltage) source** as indicated in Fig. 2-8.

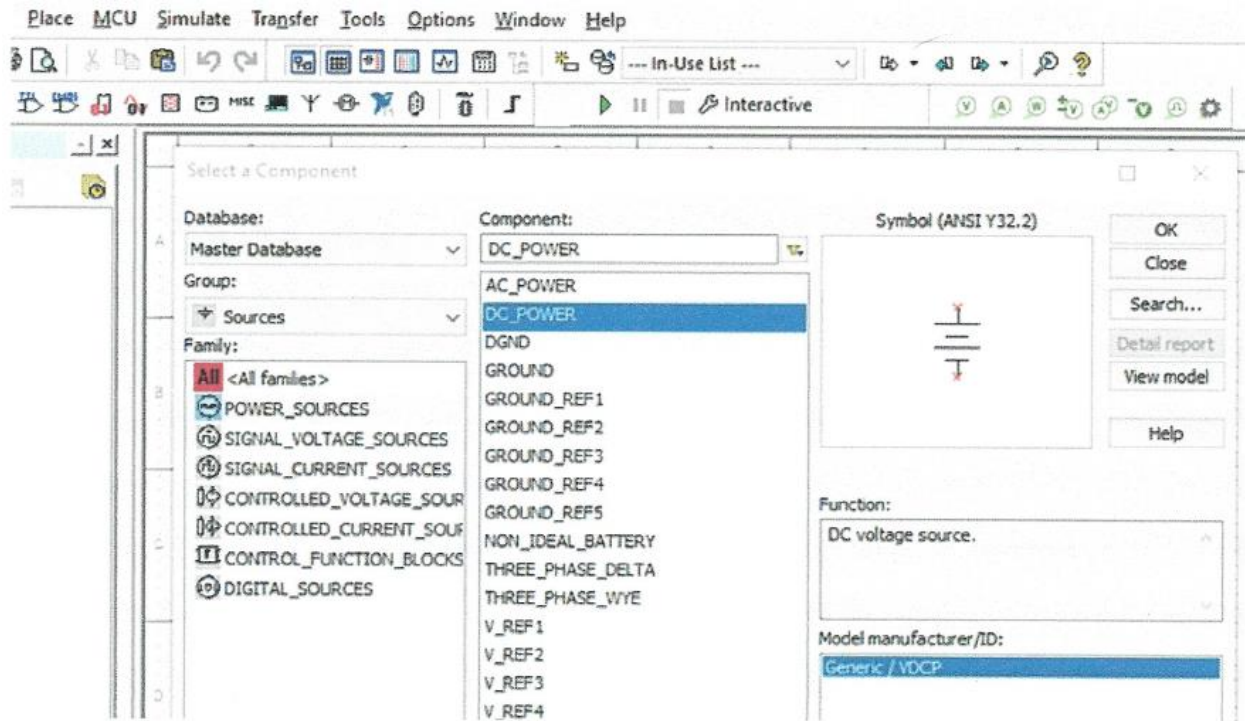


Figure 2-8.

(Note in Fig. 2-8 that Multisim provides the schematic symbol it uses for the selected device.) Once we select the desired component, we click on OK, drag the component to the desired location and place the component (with a left mouse button click) on the schematic sheet (Fig. 2-9).

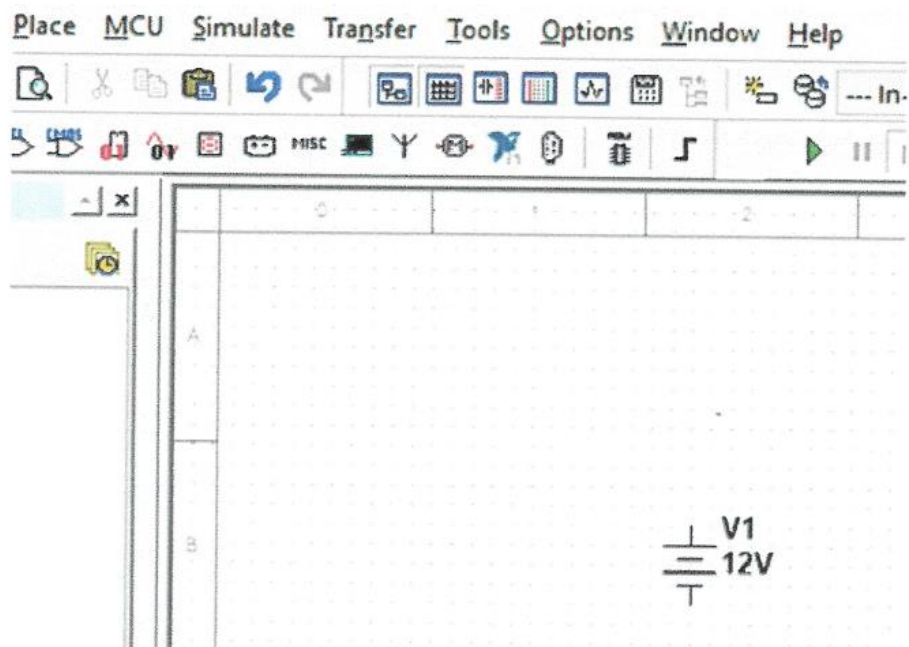


Figure 2-9.

In this same Group we also add a Ground (Fig. 2-10). (Select Ground, click on OK, and place it on the schematic sheet.)

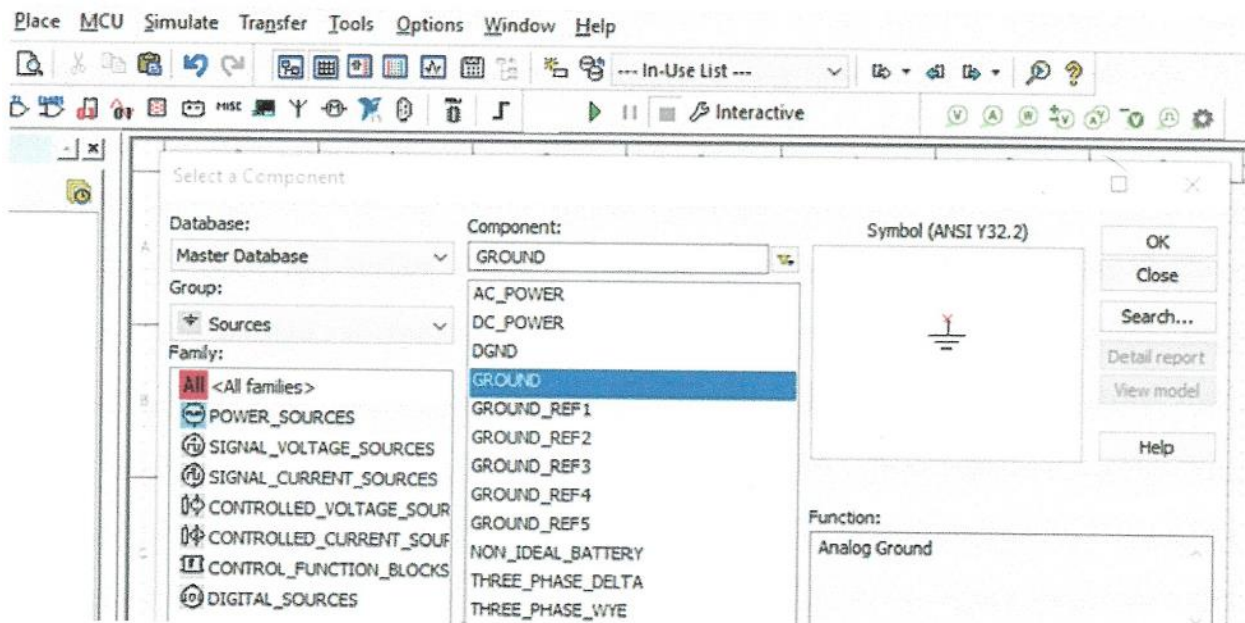


Figure 2-10.

The last component to add is a 1N914 solid-state diode. Use the drop-down menu in Group and select Diodes. A long list of diodes will appear. Rather than scrolling through the desired 1N914, click in the Component box and type “1n914” or “1N914”. The 1N914 diode will appear (Fig. 2-11).

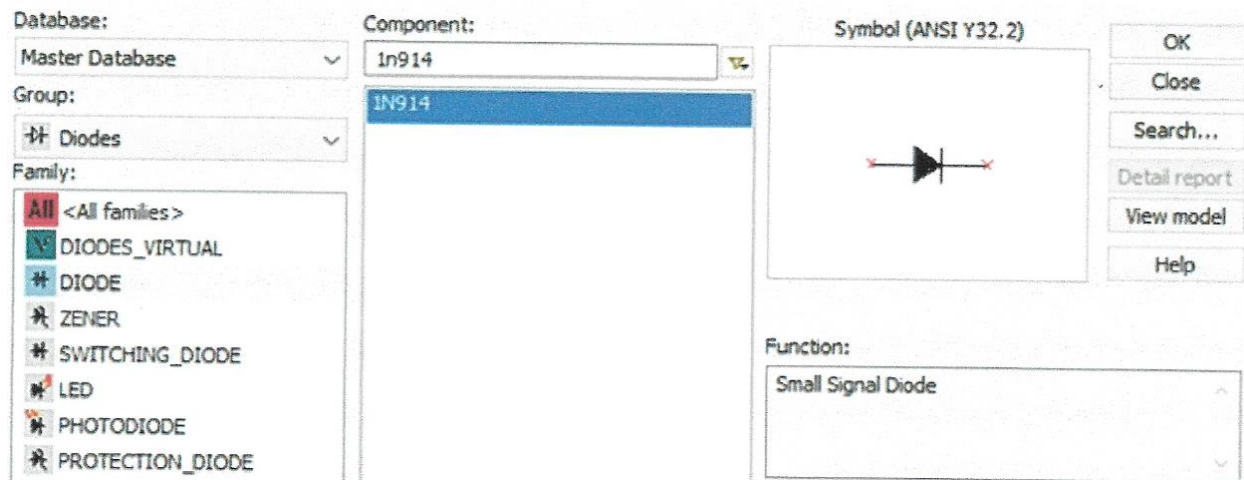


Figure 2-11.

Click OK and place the diode on the schematic sheet (Fig. 2-12). The diode will appear with a horizontal orientation on the schematic sheet. It can be rotated by clicking on it and depressing CTRL and R simultaneously. (This operation is usually indicated as CTRL-R.) By clicking and dragging each of the components, the arrangement depicted in Fig. 2-12. To wire the components together, click on Place, Component and Wire, which is also shown in Fig. 2-12.

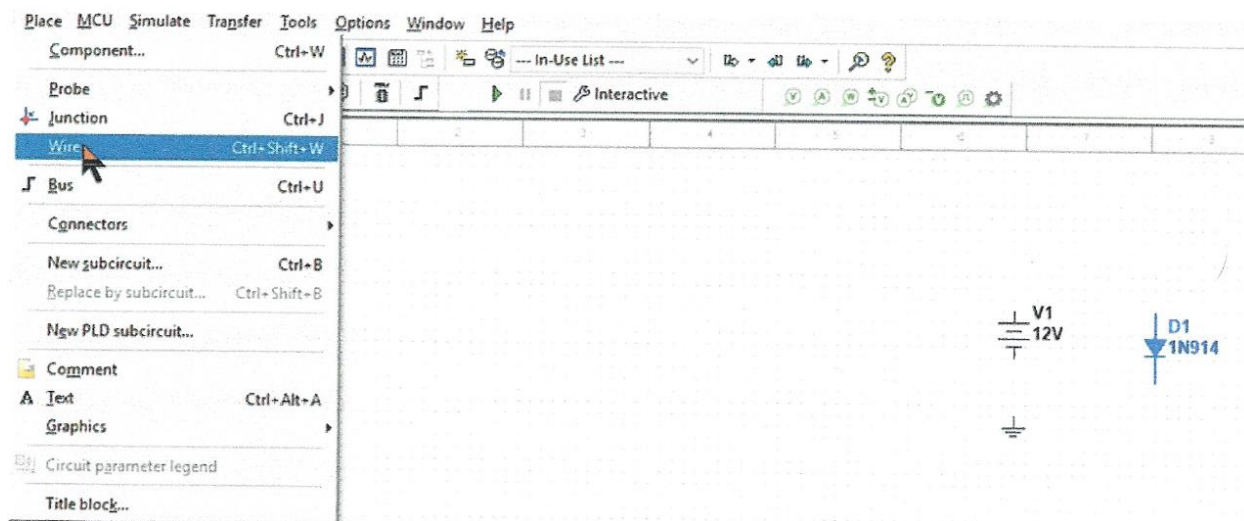


Figure 2-12.

The components are wired together as indicated in Fig. 2-13(d). We click on **Simulate** [Fig. 2-13(a)], **Analysis and simulation** [Fig. 2-13(b)], **DC Sweep** [Fig. 2-13(c)] to generate the V - I curve.

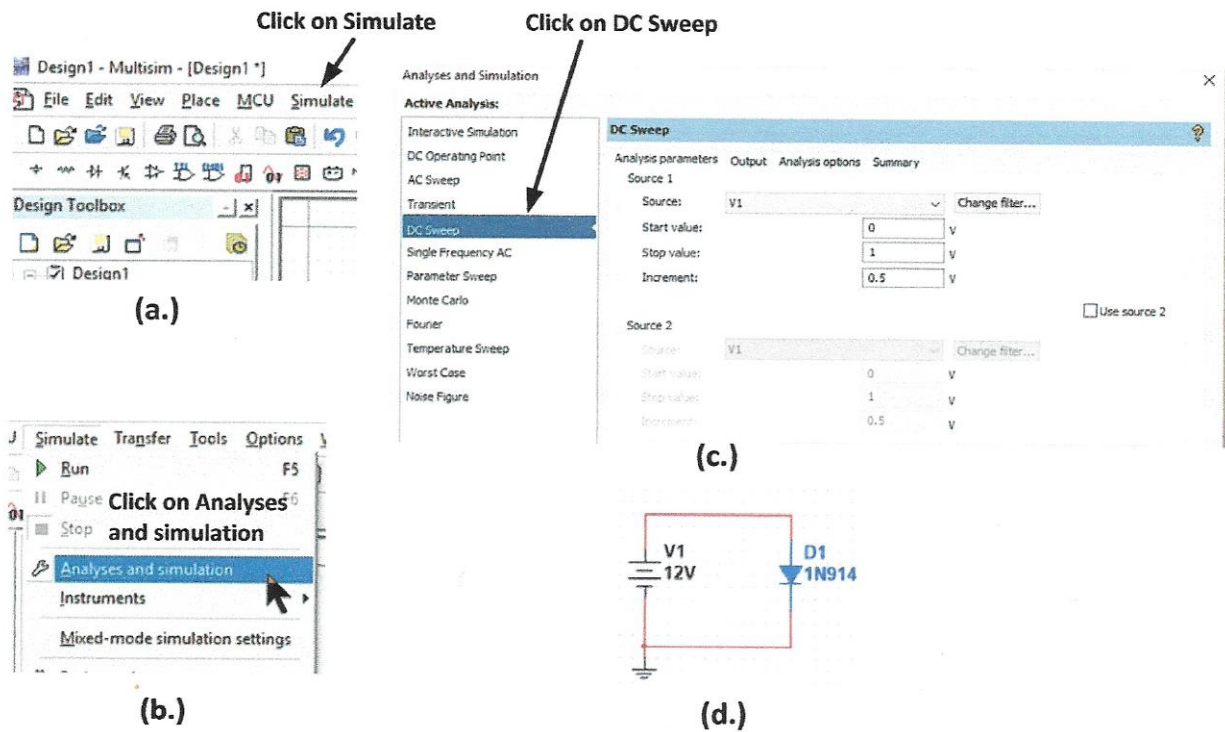


Figure 2-13.

We edit the analysis to produce a DC sweep (of the voltage source $V1$) that starts at 0 and increases to 1 V in steps of 0.01 V. This is shown in Fig. 2-14. (We are not concerned about source 2. Later it will be shown how to use that option to produce *nested* DC sweeps.)

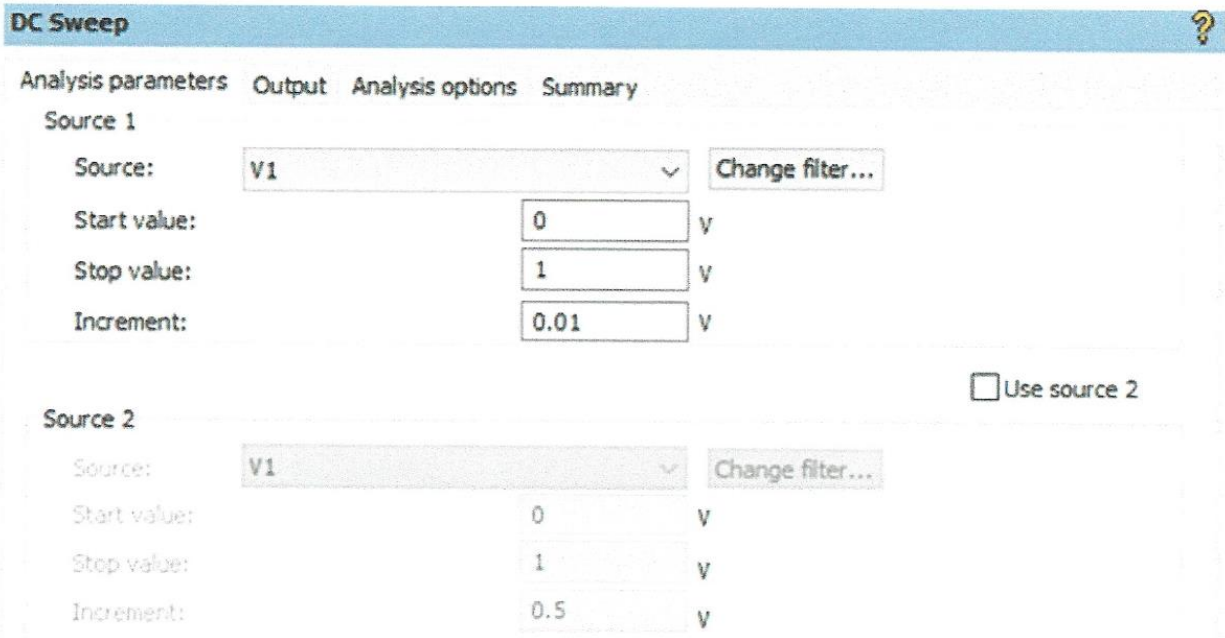


Figure 2-14.

Next, we click on the **Output** tab (Fig. 2-14). This will take us to output options selection shown in Fig. 2-15. We want the diode (D1) current to appear on the vertical axis. Click on **I(D1[ID])**¹⁴ at the top of the list on the left-hand side and then **Add**. This will cause it to appear in the table on the right. Click on the **Run** button at the bottom.

¹⁴ Do *not* worry about the format I(D1[ID]). Hey, it has a “D1” in it, which is the reference designator for the diode. That is all we care about.

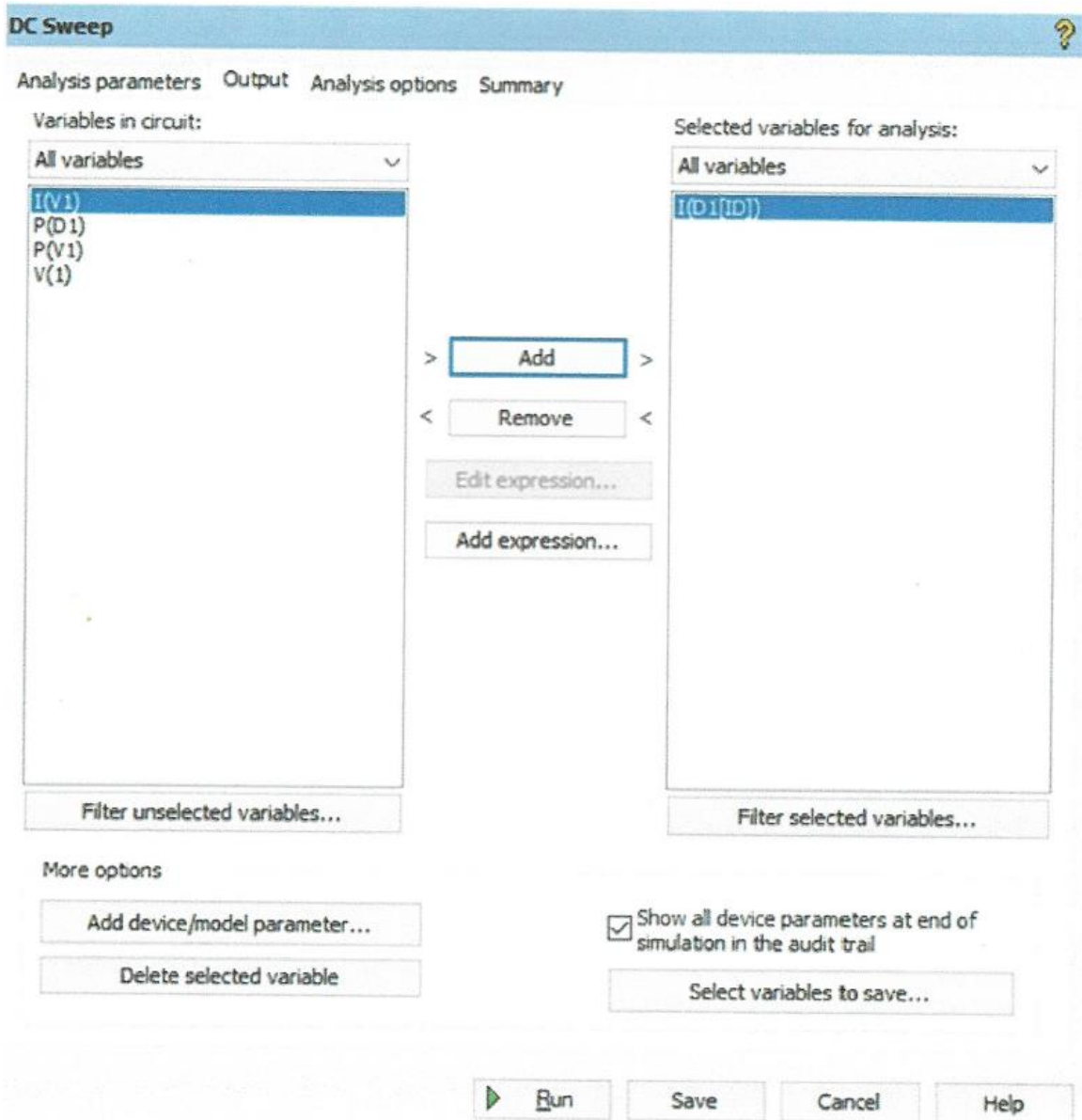


Figure 2-15.

The V - I curve will be generated (Fig. 2-17). Click on the **Graph** tab and then select **Black and White Colors** (Fig. 2-17). This replaces the black background with a white background. This is only necessary if a hard copy is desired. It will preserve printer supplies (e.g., toner and/or ink).

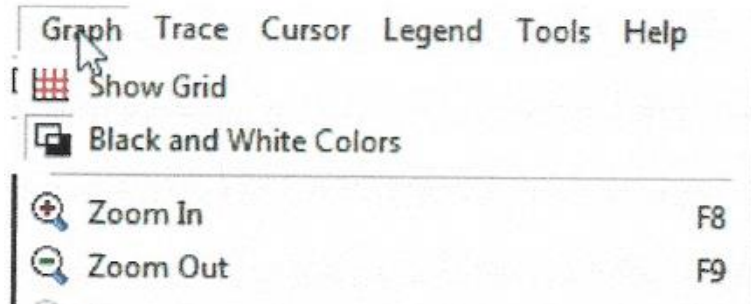


Figure 2-16.

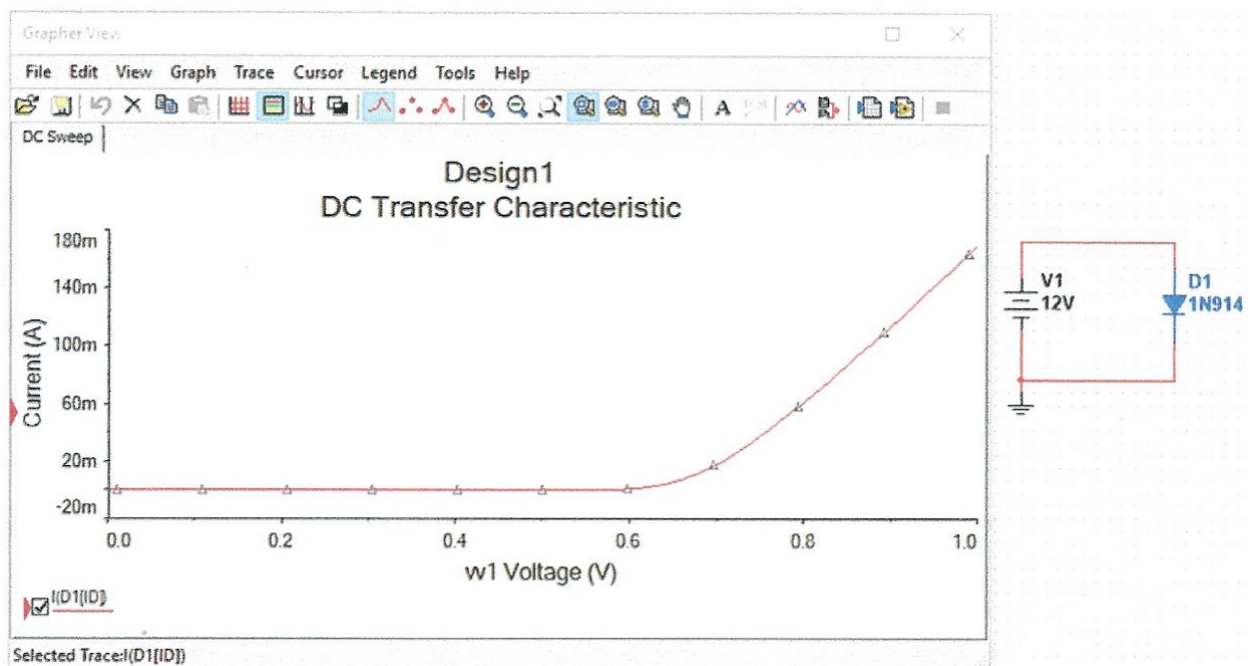


Figure 2-17.

Note that no current-limiting resistor is used in the circuit (Fig. 2-17). This is permitted because we are dealing with a computer *simulation*. Computer models do not burn up.¹⁵

There are three other points that should be mentioned. First, the primary purpose of this exercise is to introduce the use of Multisim, which includes how to draw a schematic and perform a simulation. Second, to see how a DC sweep is done – DC sweeps are used very often. Third, Multisim uses non-linear models to provide simulation results that are realistic – they reflect the expectations from the actual circuit.

¹⁵ Some simulation products include a “smoke option”. If the power rating of a device is exceeded, a smoke graphic appears on the schematic diagram. It is often difficult to convince engineering managers this novelty is worth the extra expense – particularly when the departmental budget is very restricted.

2-2 The Shockley Diode Equation and the DC Load Line

The non-linear nature of the diode is obvious when we glance at its V - I curve. Computer simulation programs (such as Multisim) use very complex non-linear mathematical models of the solid-state devices. *The Shockley diode equation (Eq. 2-3) is a simple example of a non-linear mathematical description of the ideal p - n junction.*

$$I_D = I_S(e^{KV_D} - 1) \quad (2-3)$$

where I_D = diode current (amperes)
 I_S = reverse saturation current (amperes)
 e = the natural number, 2.71828...
 K = a temperature-dependent constant (volts⁻¹)
 V_D = the bias voltage across the p - n junction (volts)

We will *not* use the Shockley diode equation to any great extent. It gives us some insight into the complexity of the computer simulation models, and it serves as the basis for some of our later work with diodes and transistors.

At room temperature (25°C or 77°F) the constant K is equal to 38.46 for an *idealized* p - n junction and the Shockley diode equation can be written as Eq. 2-4.

$$I_D = I_S(e^{38.46V_D} - 1) \quad (2-4)$$

A graph of Eq. 2-4 is given in Fig. 2-18. (An I_S of 0.1 pA is used.) Positive values of V_D provide forward bias and positive values of I_D . (Although not shown, negative values of V_D correspond to a reverse bias and results in negative values of I_D .) A table of I_D values for various values of V_D is also provided in Fig. 2-18. Students needing calculator practice may wish to verify them.¹⁶

¹⁶At the very least, make sure your calculator *has* an e^x (or an $\ln x$) button and you know how to use it. No button? You need to obtain a *scientific* calculator.

The V-I Curve of a P-N Junction Using the Shockley Diode Equation

V_D	I_D
0 V	≈ 0 mA
0.10 V	≈ 0 mA
0.20 V	≈ 0 mA
0.30 V	≈ 0 mA
0.40 V	≈ 0 mA
0.45 V	0.00328 mA
0.50 V	0.0225 mA
0.55 V	0.154 mA
0.60 V	1.051 mA
0.65 V	7.193 mA
0.70 V	49.21 mA

Note: $I_S = 0.1$ pA

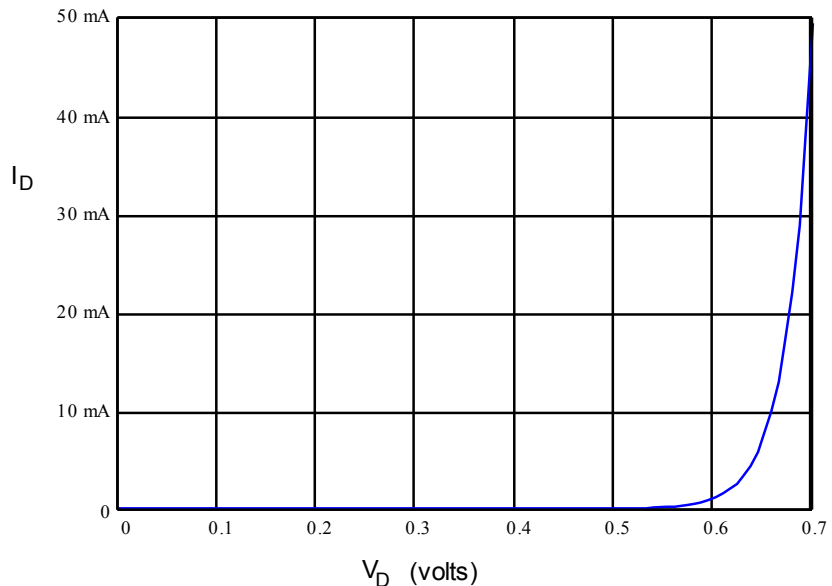


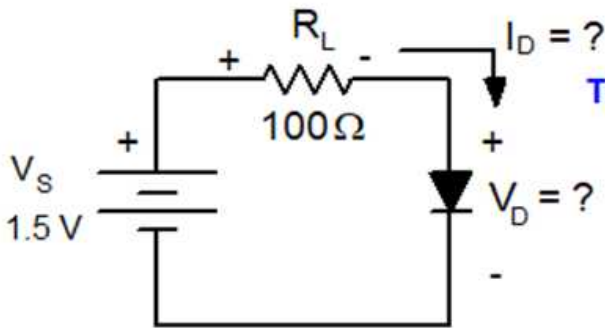
Figure 2-18.

The Shockley diode equation describes an idealized p-n junction. There are several aspects about a real diode the Shockley diode equation does not address. However, we will not concern ourselves with those considerations at this point.

The DC Load Line

We have seen how to analyze diode circuits where we are given some information about the diode. Specifically, if you refer to Examples 2-1 and 2-2, you will see that in both cases we are given the diode voltage drop. While this made the analysis examples straightforward, we seldom have this much information. When we analyze diode circuits, we are trying to *predict* what will happen in the actual circuit. This means we typically have two unknowns: I_D and V_D . To compound our problems further, we are dealing with a *non-linear circuit analysis problem*. To solve non-linear problems easily, special analysis techniques must be used. The first approach we consider is a *graphical* method called *the DC load line*. A circuit and the analysis approach are provided in Fig. 2-19.

DC Load Line Analysis



The load line equation is based on KVL.

$$V_S = I_D R_L + V_D$$

- ◆ We plot its two end points by first setting I_D to zero and finding the corresponding V_D .
- ◆ Then we set V_D to zero and find the corresponding I_D .
- ◆ This strategy is reflected in the given procedure.

Figure 2-19.

There is a simple, **five-step procedure** that can be followed to generate the DC load line analysis. Each step number is labeled in Fig. 2-20.

1. **Obtain the diode's V - I characteristic curve.** (The first quadrant is used here since the diode is forward biased. The third quadrant is used for reverse-biased diodes.)
2. **Find the open-circuit voltage (V_{oc}) and locate it on the V - I characteristic.** (This is the voltage that would appear across the diode if it were to act like an open circuit.)

$$V_{oc} = V_S$$

3. **Find the short-circuit current (I_{sc}) and locate it on the V - I characteristic.** (This is the current that would flow through the diode if it were to act like a short circuit.)

$$I_{sc} = \frac{V_S}{R_L}$$

4. **Connect the two points (V_{oc} and I_{sc}) with a straight line.** (The straight line is called the DC load line.)
5. **The intersection between the load line and the diode's characteristic curve gives the DC operating point.** The DC operating point is also called the "Q point".

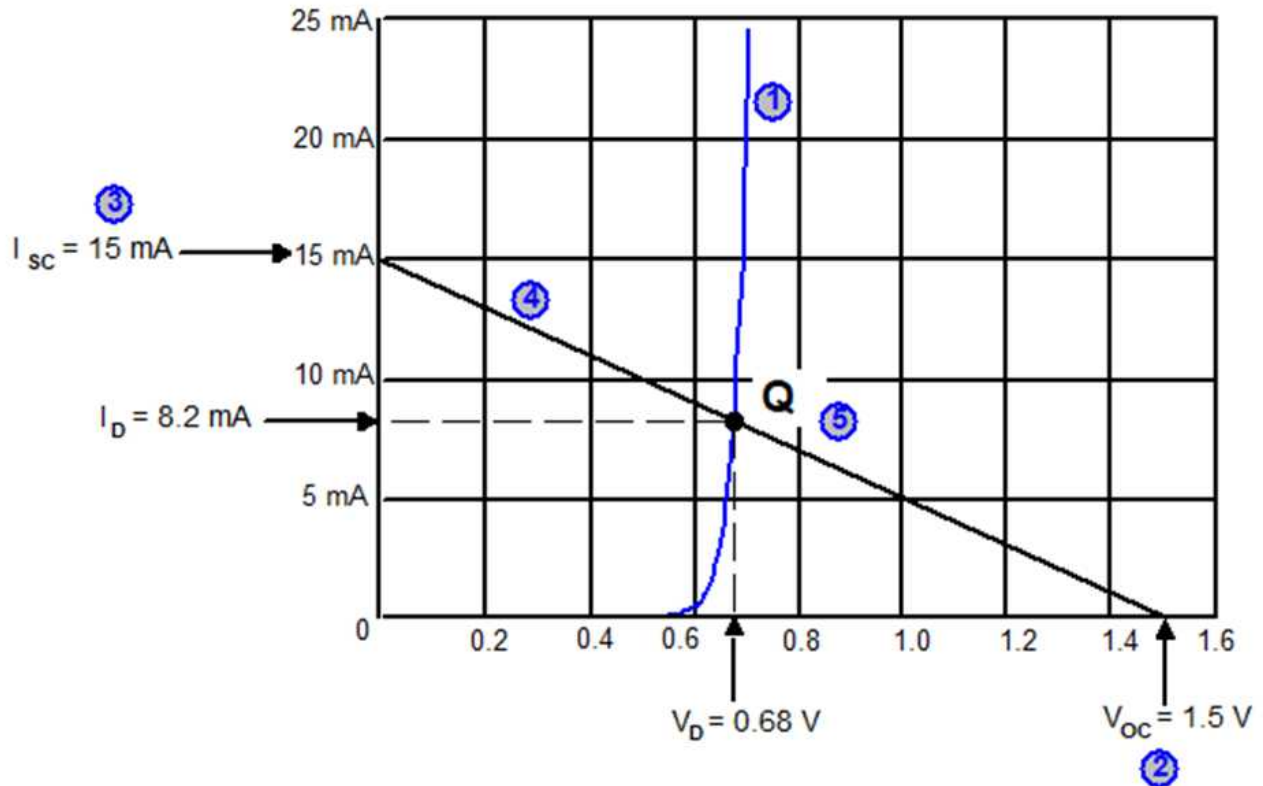


Figure 2-20.

Let's summarize. We have a series circuit that includes a forward-biased diode such as that shown in Fig. 2-19. The problem is to determine the current through the diode (I_D) and the voltage across it (V_D). The first step is to obtain the diode's V - I characteristic curve using one of the methods described in Section 2-1. Since the diode is forward biased, the analysis is conducted in the first quadrant. (If the diode is reverse-biased, we would work in the third quadrant.)

Next, we determine the endpoints of the DC load line. These can be found by obtaining the open-circuit voltage (V_{oc}) that would be present if the diode were removed and the short-circuit current (I_{sc}) that would flow if the diode were replaced by a short circuit. These are illustrated in Fig. 2-21.

Finding the Open-Circuit Voltage and the Short-Circuit Current

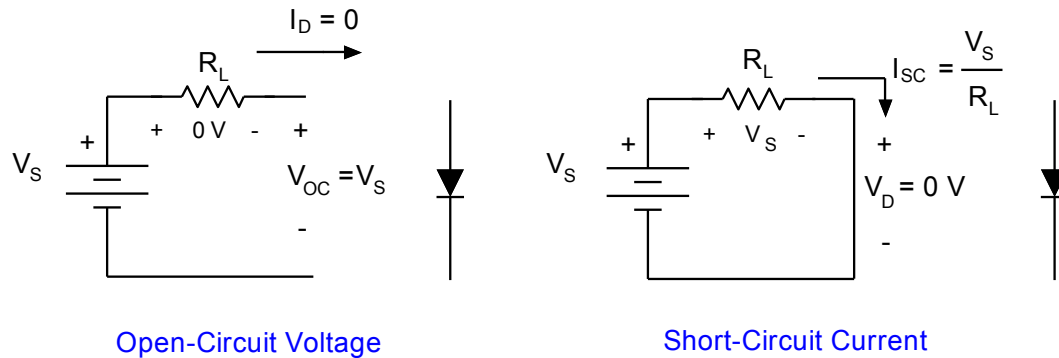


Figure 2-21.

Determining the Q point

The open-circuit voltage and the short-circuit points are located on the diode's V - I characteristic. A straight line (called **the DC load line**) is drawn between the two points. The intersection between the diode's V - I characteristic curve and the DC load line is the graphical solution to the problem. (The diode's non-linear characteristic and the circuit constraints are satisfied simultaneously.) By careful inspection of the graph we read the diode's current and voltage drop. The intersection point (and the corresponding I_D and V_D values) are described as being the diode's bias point. ***Since many electronic circuits process AC signals, the DC bias point is called the Q point. The "Q" stands for quiet, or quiescent, circuit conditions when no AC signal is applied.***

The DC load line certainly avoids the headaches associated with solving non-linear equations analytically. It can also help us visualize the voltage and current relationships in a diode circuit. However, its fundamental drawbacks are that it requires the V - I curve for the diode of interest and graphs must be drawn carefully if a reasonable accuracy is required. Because of these requirements, *the DC load line approach is seldom used*. Instead, diode models (equivalent circuits) are preferred. As we shall see, the use of diode models permits us to analyze diode circuits using "regular" circuit analysis approaches.

2-3 The Ideal Diode Model

When a diode is forward biased it passes current easily. Its resistance is low. When a diode is reverse biased the current through it is extremely small. Its resistance is large. Given these two conditions, we state the following approximation:

A forward-biased diode acts like a closed switch (a short circuit), and a reverse-biased diode acts like an open switch (an open circuit).

This approximation forms the basis of the **ideal diode model**. Very simply, if the diode is forward biased, we consider it to be a closed switch. If the diode is reverse biased, it is replaced by an open switch. These concepts are depicted in Fig. 2-22. To see how the ideal diode model is applied, consider Examples 2-3 and 2-4.

The Ideal Diode Model

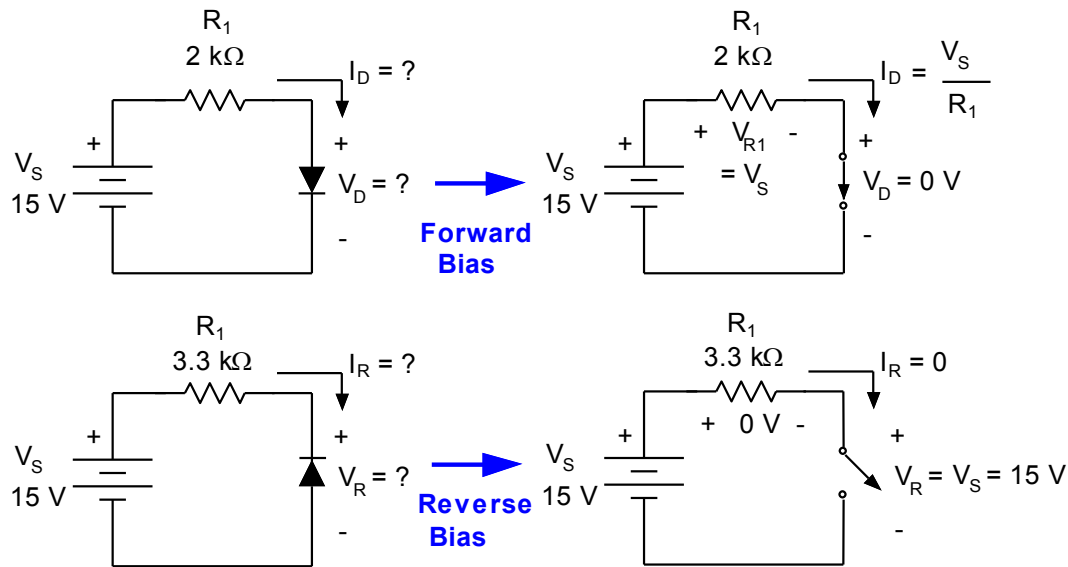


Figure 2-22.

Example 2-3. Determine the current (I_D) through the forward-biased diode shown in Fig. 2-22. Also, determine its voltage drop (V_D).

Solution: Since the diode is forward biased, we approximate it as a closed switch as shown in the equivalent circuit. By using this model, we are assuming the diode's forward voltage drop is negligibly small and set it equal to zero. Hence, we state

$$V_D = 0$$

By Kirchhoff's voltage law, the voltage drop across resistor R_1 must be equal to V_S . Ohm's law permits us to determine the current through R_1 , which is equal to I_D .

$$I_D = \frac{V_S}{R_1} = \frac{15 \text{ V}}{2 \text{ k}\Omega} = 7.5 \text{ mA}$$

Example 2-4. Determine the voltage drop (V_R) across reverse-biased diode shown in Fig. 2-22. Also, determine the current (I_R) through the diode.

Solution: Since the diode is reverse biased, we approximate it as an open switch as shown in the equivalent circuit. By using this model, we are assuming the diode's reverse current is negligibly small. Therefore, we set it equal to zero. Hence, we state

$$I_R = 0$$

By Ohm's law, the voltage drop across resistor R_1 must also be equal to zero. By applying Kirchhoff's voltage law, we find the reverse voltage across the diode to be equal to V_S .

$$V_R = V_S = 15 \text{ V}$$

From Fig. 2-22 and Examples 2-3 and 2-4, it is clear the ideal diode model is extremely easy to apply. It is also reasonably accurate provided the diode's forward voltage drop (and/or its reverse current) is negligibly small. To contrast the ideal diode model with the real diode (like the 1N4004 rectifier), we compare their respective V - I characteristic curves in Fig. 2-23.

A Comparison Between an Actual and Ideal Diode V - I Characteristic

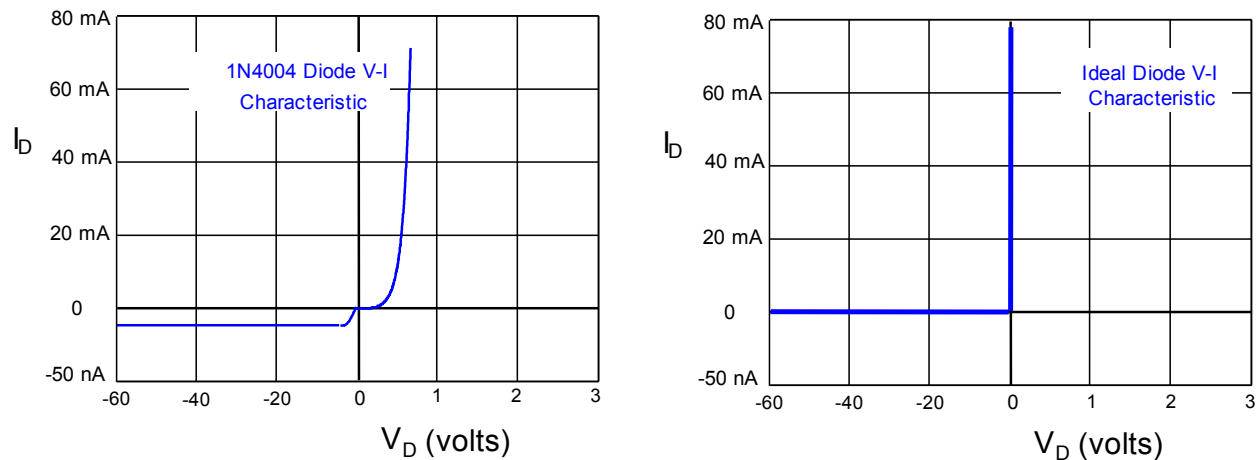


Figure 2-23.

By inspection we see the ideal diode forward voltage drop is zero volts, regardless of the forward current. We also see the ideal diode's reverse current is zero for all values of reverse voltage. Again, the accuracy of these approximations depends on the problem under consideration. This will become clear when we investigate the more accurate knee-voltage and the reverse-current-source diode models.

2-4 The Knee-Voltage Diode Model

The knee-voltage model of a diode is a far more accurate representation of a diode's forward-biased nature than the ideal diode model. Subsequently, it is the model of choice for much of our work.

A (sufficiently) forward-biased diode acts like a voltage source in that it drops a reasonably constant voltage independent of its forward current. Its voltage drop is approximately equal to its knee voltage. A reverse-biased diode acts like an open switch.

This model only modifies how we look at a forward-biased diode. (The “sufficiently” qualification will be explained later in this section.) It does not change our view of a reverse-biased diode. The features of the knee-voltage diode model have been summarized in Fig. 2-24.

The Knee-Voltage Diode Model

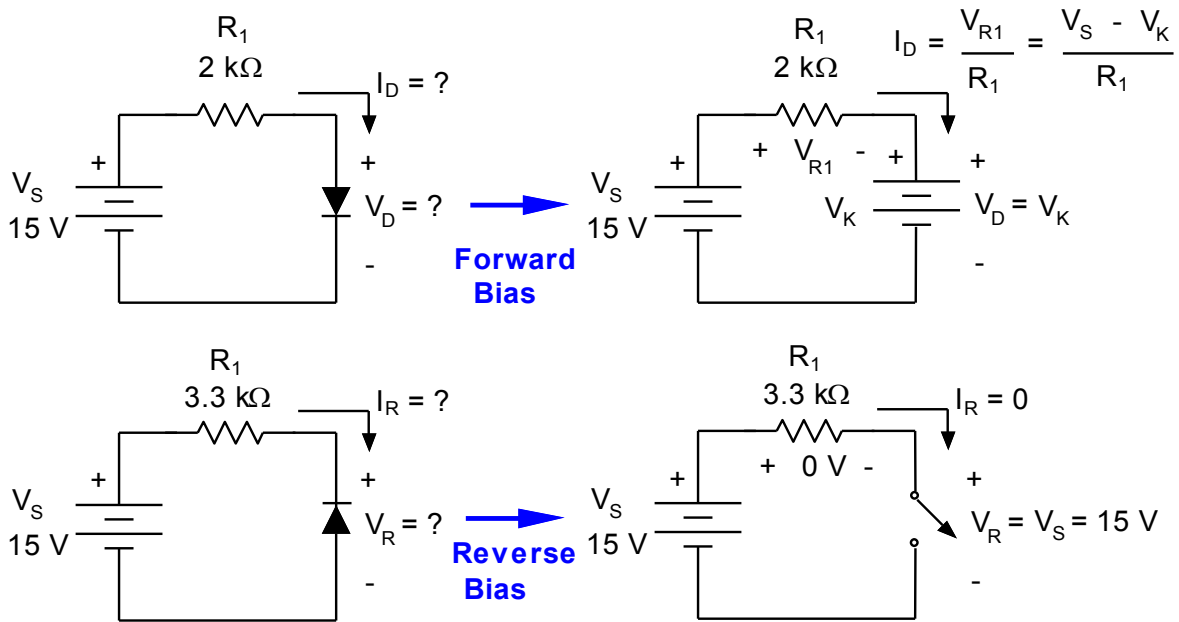


Figure 2-24.

The strategy behind the knee-voltage model is simple. We have two unknowns: I_D and V_D . To simplify our problem, we approximate V_D to eliminate it as an unknown. **Recall (from Table 2-1) the knee voltages (V_K) for silicon and germanium diodes are taken to be 0.7 V and 0.3 V, respectively.** Since we “know” the forward voltage across the diode is equal to V_K , we use Kirchhoff’s voltage law to determine the voltage across resistor R_1 . Ohm’s law permits us to find the forward current through it. Hence, from Fig. 2-24 we arrive at Eq. 2-5.

$$V_{R1} + V_K = V_S$$

$$I_D R_1 + V_K = V_S$$

$$I_D = \frac{V_S - V_K}{R_1}$$

(2-5)

Consider Examples 2-5 and 2-6.

Example 2-5. A *silicon* diode is used in the forward-bias circuit given in Fig. 2-24. Find the diode's forward current I_D .

Solution: Since the diode is silicon, we use the knee-voltage diode model shown in Fig. 2-24 and set

$$V_D = V_K = 0.7 \text{ V}$$

From Eq. 2-5 we find I_D .

$$I_D = \frac{V_S - V_K}{R_1} = \frac{15 \text{ V} - 0.7 \text{ V}}{2 \text{ k}\Omega} = 7.15 \text{ mA}$$

Example 2-6. A *germanium* diode is used in the forward-bias circuit given in Fig. 2-24. Find the diode's forward current I_D .

Solution: Since the diode is germanium, we use the knee-voltage diode model shown in Fig. 2-24 and set

$$V_D = V_K = 0.3 \text{ V}$$

From Eq. 2-5 we find I_D .

$$I_D = \frac{V_S - V_K}{R_1} = \frac{15 \text{ V} - 0.3 \text{ V}}{2 \text{ k}\Omega} = 7.35 \text{ mA}$$

Since the forward-bias voltage source (V_S) is so large compared to the diode voltage drops, the diode current is approximately the same in both cases. However, if V_S is reduced (e.g., to 1.5 V) the silicon and germanium diode currents will be affected significantly (e.g., 0.4 mA and 0.6 mA, respectively.) You are encouraged to verify this.

The V - I curve for the knee-voltage diode model is illustrated in Fig. 2-25. The diode's non-linear V - I characteristic is being approximated using straight-line segments. Consequently, the knee-voltage model is also described as a ***piecewise linear approximation***. The vertical portion of the characteristic means the voltage drop across the diode is constant regardless of the forward current through it. Observe that ***no diode current is assumed to flow for diode voltage drops that are less than the knee voltage***. Alternatively, we may state the diode will pass zero current until its barrier potential is overcome. Consider Example 2-7.

A Comparison Between an Actual and the Knee-Voltage Model Diode V-I Characteristic

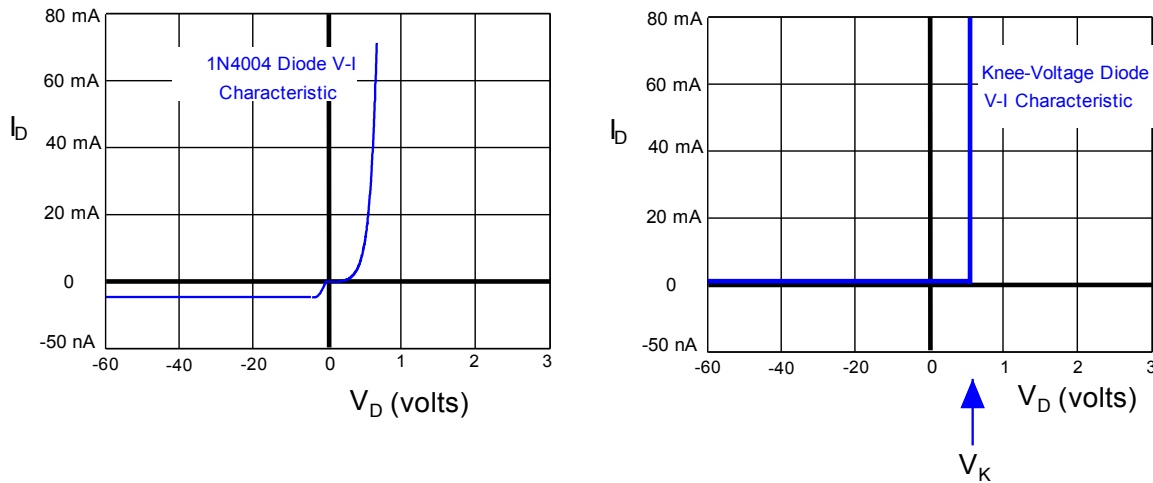


Figure 2-25.

Example 2-7. All three of the diodes shown in Fig. 2-26(a) are silicon units. Apply the knee-voltage model to determine the currents through each of the diodes.

Solution: First, we observe that all three diodes are forward biased. However, since the circuit branch containing diode D_1 only requires 0.7 V to go into conduction, it will conduct first. This means the voltage across the series combination of diodes D_2 and D_3 will be limited to 0.7 V. The series combination of two silicon diodes means a total of 1.4 V is required to place them into conduction. Since diode D_1 limits the voltage to 0.7 V, diodes D_2 and D_3 will both be *off* (or non-conducting). The equivalent circuit is shown in Fig. 2-26 (b).

$$V_{D1} = V_K = 0.7 \text{ V}$$

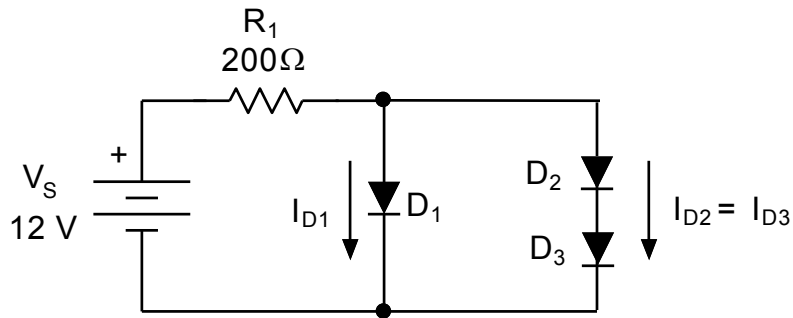
Applying Eq. 2-5 allows us to find I_{D1} .

$$I_{D1} = \frac{V_S - V_K}{R_1} = \frac{12 \text{ V} - 0.7 \text{ V}}{200 \Omega} = 56.5 \text{ mA}$$

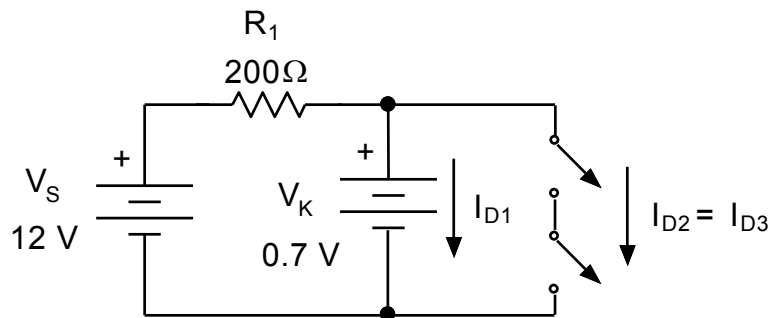
Since diodes D_2 and D_3 are both non-conducting, their currents are zero.

$$I_{D2} = I_{D3} = 0$$

Using the Knee-Voltage Diode Model



(a) The circuit to be analyzed.



(b) The equivalent circuit.

Figure 2-26.

The circuit design given in Fig. 2-26 is not likely to be seen in practice¹⁷. However, its purpose is to illustrate that we must always be mindful of the amount of forward bias placed across a p - n junction. If it is too small, the p - n junction will not conduct. This principle is used in the short-circuit protection circuits found in power supplies and power amplifiers that we shall investigate in our later work.

¹⁷ On its encounter, we could assume it was concocted on a Monday morning by a circuit designer who was suffering from a weekend of excesses.

2-5 The Reverse Current Source Diode Model

Ideally, a reverse-biased p - n junction acts like an open switch. However, the reverse current through a diode is only *approximately* zero. Occasionally, greater precision is required when a circuit is being analyzed. (This could be during the circuit design phase or when troubleshooting a “sick” circuit.) The result is we must take the reverse current into account. Since the reverse current (I_R) is approximately constant, we can represent a reverse-biased diode by using a current source. (Remember: *A current source maintains a constant terminal current independent of the voltage across it.*) This concept is illustrated in Fig. 2-27.

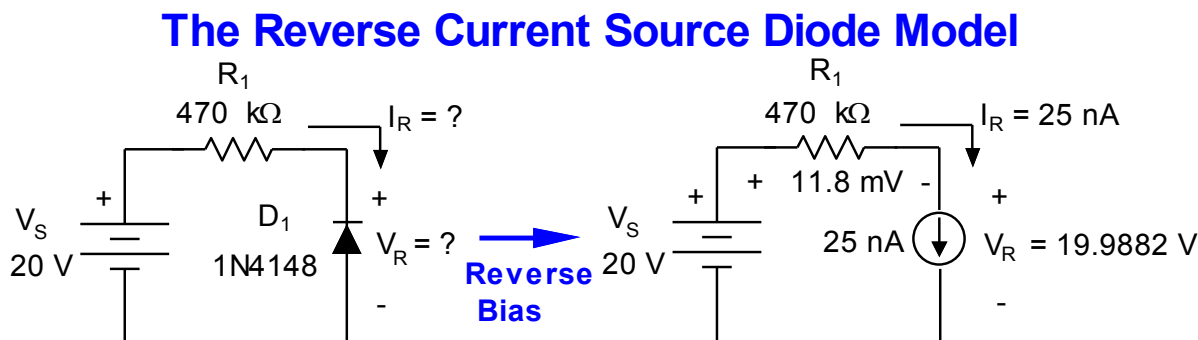


Figure 2-27.

Example 2-8. A 1N4148 silicon diode is reverse biased as shown in Fig. 2-27. Find the reverse current I_R and the reverse voltage drop V_R .

Solution: The manufacturer gives the maximum current I_R (at 25°C) of 25 nA with a reverse bias of 20 V. Using this value for I_R permits us to ascertain the voltage drop across the diode. By using Kirchhoff’s voltage law and Ohm’s law, we arrive at the result below.

$$V_R = V_S - I_R R_1 = 20 \text{ V} - (25 \times 10^{-9} \text{ A})(470 \times 10^3 \Omega) = 19.988 \text{ V} \cong 19.99 \text{ V}$$

With a little reflection, it is clear the increased precision offered by this model has reduced our usual guess (of 20 V since the diode is assumed to act like an open) by about 10 mV. However, do *not* dismiss the model as useless. The only time we really need to apply it is when the *ideal model does not work* to explain a given problem.

2-6 Zener and Avalanche Diodes

When a p - n junction is reverse biased excessively, it will experience a phenomenon known as **voltage breakdown**. Figure 2-28 illustrates the effect of reverse voltage breakdown on the V - I characteristic curve. When a p - n junction is in breakdown, its reverse current can rise to large values. The current is limited solely by the resistance in series with the p - n junction. Breakdown is not inherently damaging to a p - n junction. However, if the reverse current is *not* limited to a safe value, the resulting excessive power dissipation (VI) can damage the p - n junction.

Generally, *rectifier and small-signal diodes* are *not* expected to be subjected to reverse breakdown conditions. However, ***zener and avalanche diodes are designed to be operated in the reverse-breakdown mode***. As their respective names suggest, zener diodes enter breakdown due to the Zener effect while avalanche diodes experience breakdown because of the avalanche mechanism.

Zener and avalanche diodes are used as *voltage limiters*, *simple voltage regulators*, and as *voltage references* in some electronic circuits. Zener and avalanche diodes respond differently to the effects of temperature. This will be explained shortly. Consequently, we need to distinguish between the two types of voltage breakdown diodes. This is made difficult because ***both are referred to as zener diodes***. Further, the *same* schematic symbol is used. The (most popular) symbol is also indicated in Fig. 2-28. Note the cathode bar forms a “Z”.

Reverse Breakdown on the V-I Characteristic Curve

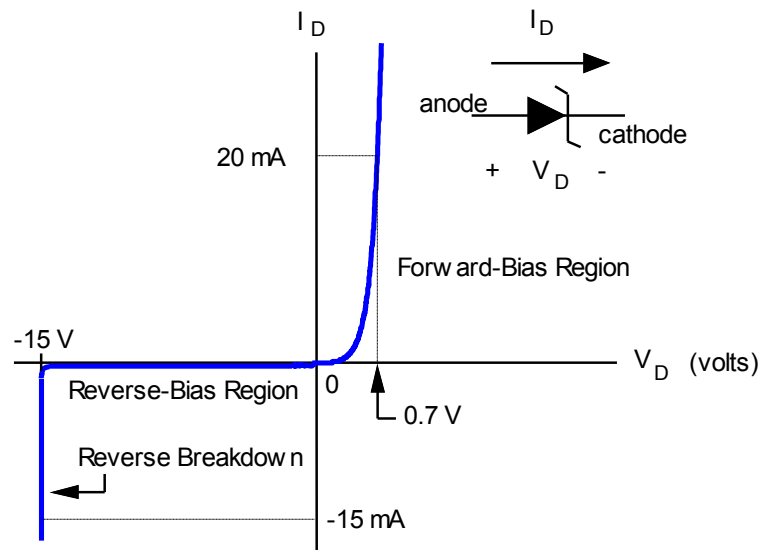


Figure 2-28.

Zener Breakdown Requires a Narrow Depletion Region

When any *p-n* junction is reverse biased, its depletion region widens. The depletion region width extends into a semiconductor as a function of its doping level. Therefore, the depletion penetrates slightly into the heavily doped (n^+) side and further into the moderately-doped *p* side [see Fig. 2-29]. The doping levels are intended to keep the depletion region narrow. A corresponding electric field will develop within the depletion region. If the electric field intensity (ϵ) becomes 3×10^8 V/m or greater, Zener breakdown can result. When Zener breakdown occurs, the electric field intensity is so great that electrons are ripped away from their parent semiconductor (e.g., silicon) atoms. The requirement for the Zener effect is given by Eq. 2-9. ***Note the typical breakdown voltage range for zener diodes is 2.4 to 5 volts.***

$$\epsilon = \frac{V}{d} = \frac{\text{Reverse Bias}}{\text{Depletion Region Width}} \geq 3 \times 10^8 \frac{\text{V}}{\text{m}} \quad (2-9)$$

2.4 to 5 volts
 Small to produce the required electric field intensity

A Reverse-Biased Zener Diode P-N Junction in Breakdown

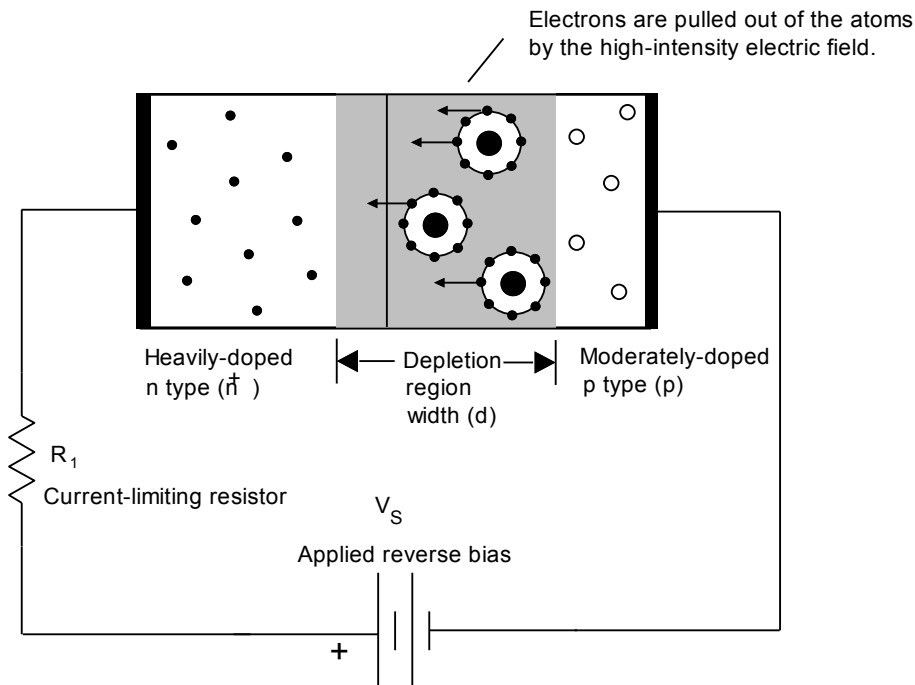


Figure 2-29.

Avalanche Breakdown Occurs at Greater than 5 Volts

When the p -side doping levels are reduced to lightly doped (p^-), the depletion region will be wider [see Fig. 2-30]. As the reverse voltage is increased, the electric field intensity will also increase. However, because depletion region is wider, the reverse voltages are larger. Another result will be observed before the electric field intensity reaches the level necessary for the Zener effect to occur.

The (minority carrier) electrons that form on the p side of the depletion region will be accelerated by the applied reverse voltage. As the velocity of an electron is increased, its kinetic energy also increases. (This is given by Eq. 1-1.) The electrons are quite likely to collide with semiconductor (e.g., silicon) atoms within the depletion region. Because the kinetic energy of the electrons is so large, they will dislodge additional electrons when they collide with the semiconductor atoms. This will result in an avalanche of charge carriers and a rapid increase in the reverse current. ***Avalanche breakdown occurs when the reverse voltage exceeds 5 volts.***

A Reverse-Biased Avalanche Diode P-N Junction in Breakdown

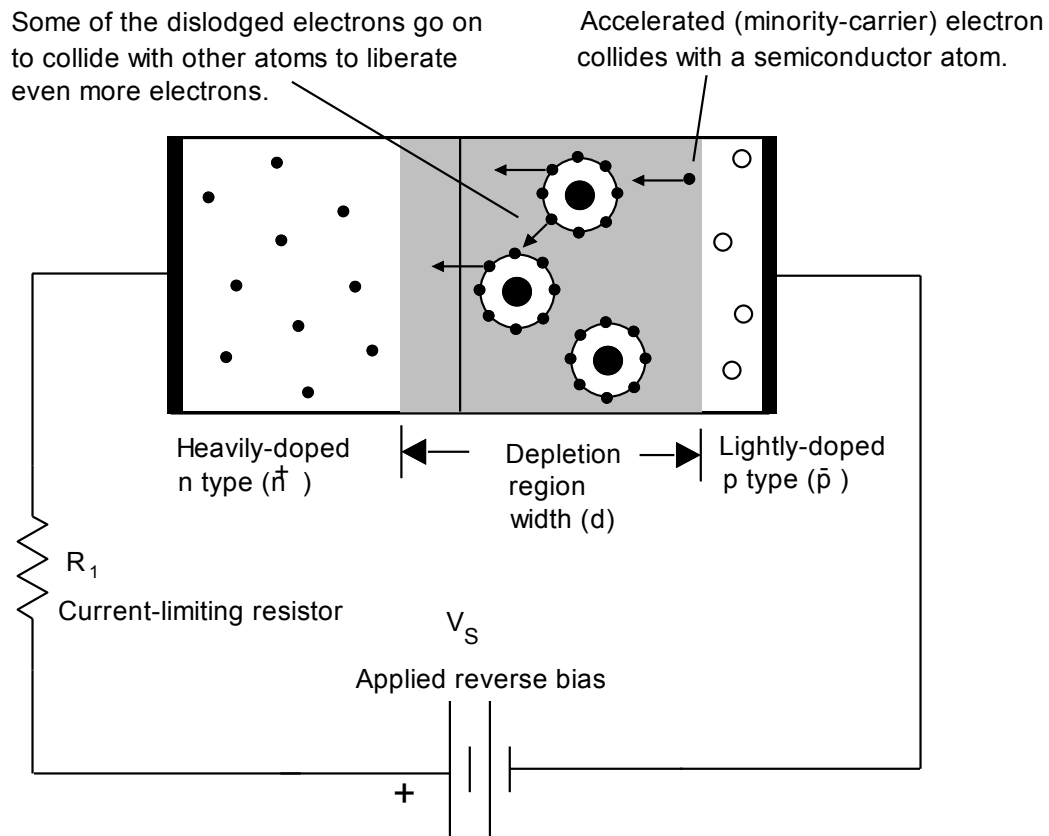


Figure 2-30.

Significance?

Now that we have worked through the fundamental differences between zener and avalanche diodes, it is natural to wonder why this is important. There are two reasons. First, the Zener effect exhibits a negative temperature coefficient while the avalanche mechanism demonstrates a positive temperature coefficient. This means a zener diode's breakdown voltage will tend to *decrease* as its temperature is *raised*. In contrast, an avalanche diode's breakdown voltage will tend to *increase* as its temperature is *raised*. The effects on the V - I curves are shown in Fig. 2-31.

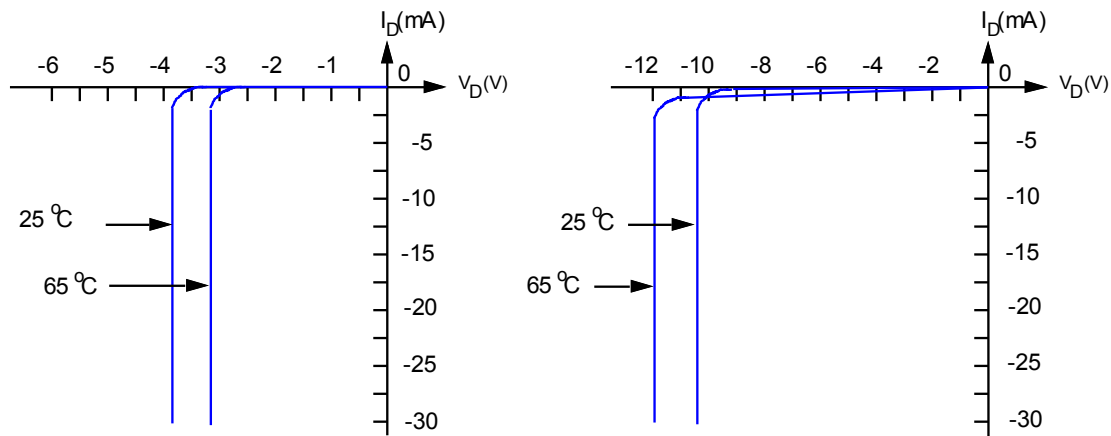
Since technicians, engineers, and even the manufacturers of zener and avalanche diodes refer to them both as “zener” diodes, the only way we can know which one we are dealing with is by remembering the following:

- **Zener diodes have breakdown voltages of less than 5 volts and have a negative temperature coefficient (negative tempco).**
- **Avalanche diodes have breakdown voltages that are greater than 5 volts and have a positive temperature coefficient (positive tempco).**
- **Diodes that break down around 5 volts experience the Zener effect and the avalanche mechanism simultaneously. Consequently, these diodes have breakdown**

voltages that do *not* change with temperature. These diodes are said to have a zero-temperature coefficient.

The second reason for understanding these breakdown mechanisms is because they also limit the maximum reverse voltages that transistors and integrated circuits can withstand.

Temperature Effects on Zener and Avalanche Breakdown Diodes



(a) Zener diodes have a negative tempco.(b) Avalanche diodes have a positive tempco

Figure 2-31.

2-7 The Ideal Zener Diode Model

The ideal model for a zener diode in breakdown is a voltage source as shown in Fig. 2-32. The model is like the knee-voltage diode model used to describe forward-biased diodes. The assumption here is the reverse breakdown portion of the V - I characteristic (Fig. 2-31) is essentially vertical. ***This means the breakdown voltage is virtually constant regardless of the size of the current.*** (Both V_Z and I_Z are *positive* quantities since they are defined as indicated in Fig. 2-32.)

The Ideal Zener Diode Model

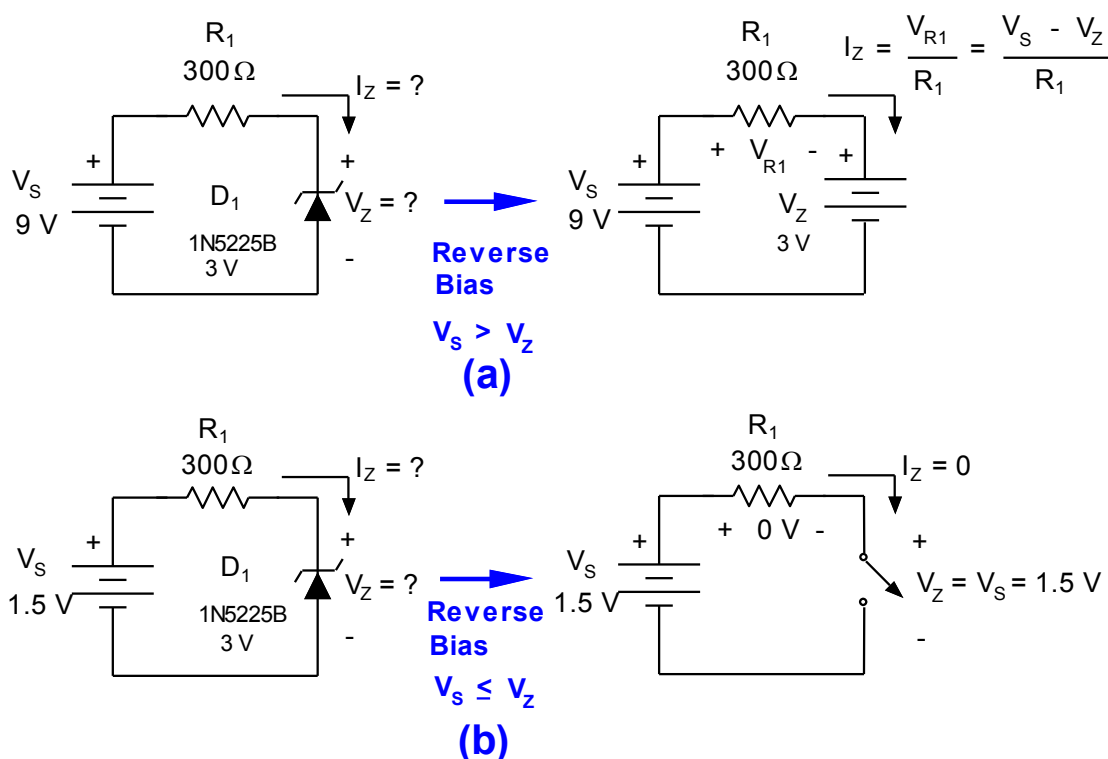


Figure 2-32.

We also note in Fig. 2-32(b) that if the applied reverse voltage is not large enough, the zener diode will not enter breakdown and behaves like an open switch.

Example 2-9. A 1N5225B zener diode is reverse biased with a V_S of 9 V as shown in Fig. 2-32(a). Find the zener diode's current I_Z and its voltage drop V_Z .

Solution: A manufacturer's data sheet indicates the 1N5225B has a nominal breakdown voltage of 3 V. Since the source voltage is more than adequate to cause breakdown, we model the zener diode as a 3-V source. Therefore, we assume

$$V_Z = 3 \text{ V}$$

Kirchhoff's voltage law gives us the voltage across resistor R_1 , and Ohm's law permits us to find the current.

$$I_Z = \frac{V_S - V_Z}{R_1} = \frac{9 \text{ V} - 3 \text{ V}}{300 \Omega} = 20 \text{ mA}$$

Example 2-10. The 1N5225B zener diode given in Example 2-9 is now reverse biased with a V_S of 1.5 V as shown in Fig. 2-32(b). Find the zener diode's current I_Z and its voltage drop V_Z .

Solution: Since the applied reverse bias is not large enough to cause breakdown, the zener diode is modeled as an open switch. Consequently, it drops all the applied voltage and the current is zero. These observations are indicated in Fig. 2-32(b).

$$V_Z = V_S = 1.5 \text{ V and } I_Z = 0$$

Both zener and avalanche diodes are made from silicon. This is because the reverse leakage current associated with reverse-biased silicon diodes tends to be small. Subsequently, a forward-biased “zener” diode acts like any forward-biased silicon diode. This means the knee-voltage model for forward bias shown in Fig. 2-24 applies and V_K is 0.7 V.

2-8 Static and Dynamic Resistance

The ideal zener diode model represents the zener diode as a voltage source when it is in breakdown. This means the voltage across the zener diode is constant when in breakdown. The size of the zener current (I_Z) does not matter. In actuality, the magnitude of the zener voltage (V_Z) increases as the zener current (I_Z) increases. The variation in the zener voltage with current is produced by the effects of resistance.

The semiconductor material has some inherent resistance called its **bulk resistance**. (The bulk resistance of a semiconductor such as silicon is produced by the collisions that occur between the electrons and the semiconductor atoms.) The **diode leads** have some small resistance. The third cause is the resistance that exists between the diode lead connections and the semiconductor material. This is called **contact resistance**.

The increase in V_Z with increases in I_Z can be incorporated in the model of the zener diode by using a **dynamic resistance** in series with an equivalent voltage source. Before we proceed further, we must understand the differences between static and dynamic resistance.

Static Resistance is DC Resistance

Static resistance can be determined by using Ohm's law. It is given by the ratio of the DC voltage across the device (or circuit) of interest to the corresponding current through it. Consider Fig. 2-33. A resistor has a straight-line V - I characteristic that passes through zero. Because the resistor has a straight-line V - I characteristic *and* because it passes through zero, it is described as a *linear* circuit element. At every point along its V - I characteristic, the ratio of the voltage across it to the corresponding current through it gives its resistance.

The Static (DC) Resistance of a Linear Resistor is Constant

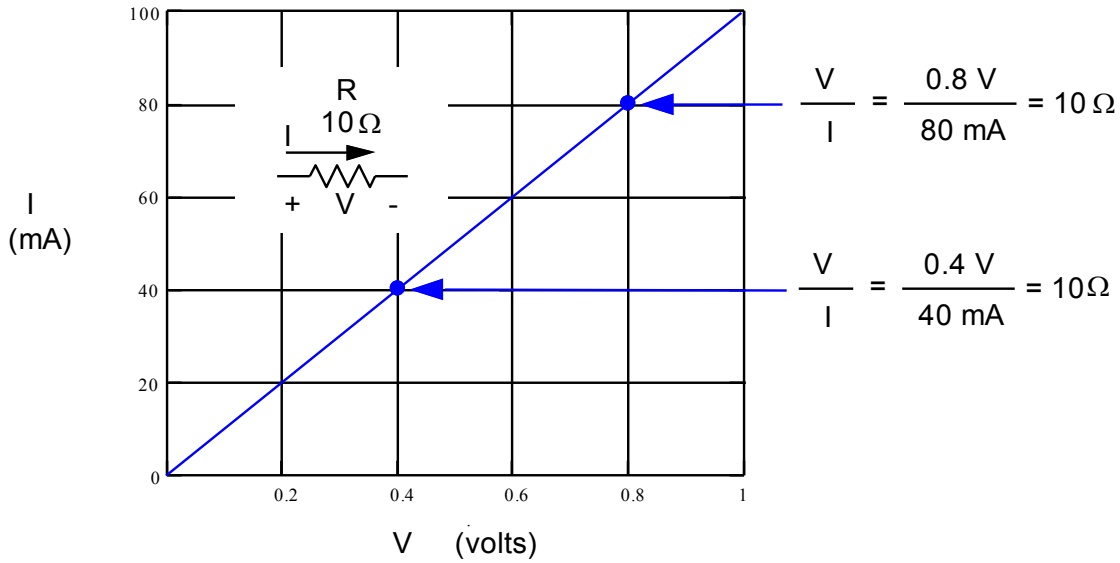


Figure 2-33.

The concepts depicted in Fig. 2-33 should be familiar. We are just reminding ourselves of the characteristics of a linear resistor. Now suppose we examine the V - I characteristics of a $10\text{-}\Omega$ resistor in series with a 3-V voltage source (V_{Z0}) as indicated in Fig. 2-34. The reason why a lowercase letter (r_Z) has been used for the resistor will be explained shortly.

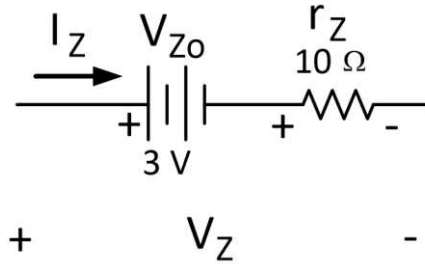


Figure 2-34.

Now by applying Kirchhoff's voltage law to the series circuit shown in Fig. 2-34, we obtain the result below.

$$V_Z = V_{Z0} + I_Z r_Z$$

The total voltage V_Z across the *series combination* is given by the sum of the voltage source V_{Z0} and the voltage drop $I_Z r_Z$ across the series resistance. By inspection, when the current I is zero, the total voltage V_Z will be equal to 3 V . If the current becomes 20 mA the total voltage V_Z becomes 3.2 V .

$$V_Z = V_{Z0} + I_Z r_Z = 3 \text{ V} + (20 \text{ mA})(10 \Omega) = 3.2 \text{ V}$$

These observations are reflected in Fig. 2-35. ***If the applied voltage is less than V_{Z0} , we assume the combination acts like an open circuit. Consequently, that portion of the V - I characteristic is represented by a horizontal line until the voltage reaches V_{Z0} .***

The Static (DC) Resistance of a Non-Linear Resistor is NOT Constant

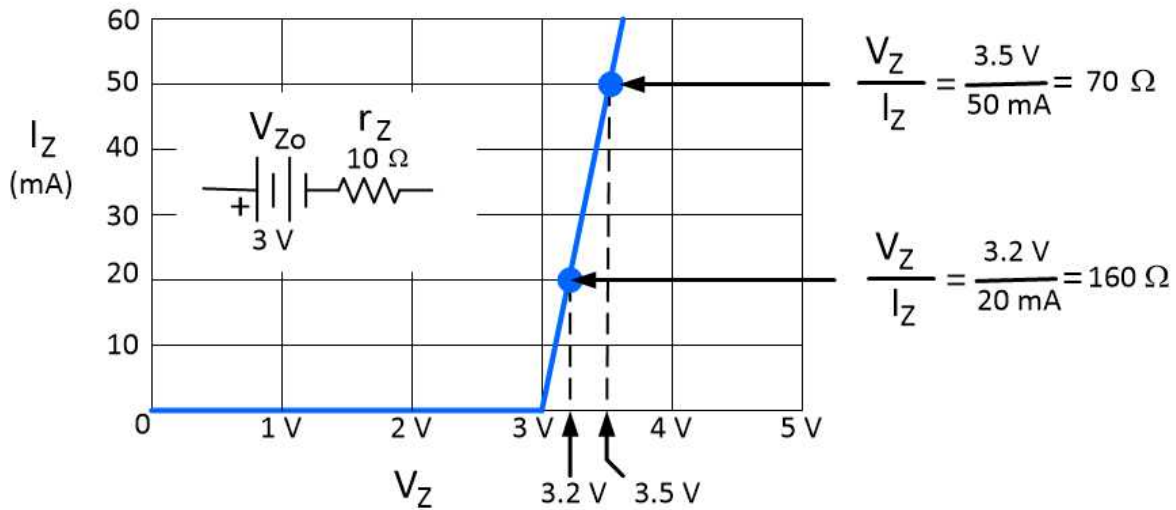


Figure 2-35.

The composite V - I characteristic forms a straight line. However, because it does not pass through zero, it is classified as being *non-linear*. This means its static resistance is *not* constant. At a current of 20 mA, the resistance is 160 Ω and at a current of 50 mA the resistance becomes 70 Ω . ***The static resistance decreases as the current increases.*** (This also occurs in the case of rectifier and small-signal diodes because of their non-linear V - I characteristic.)

Dynamic resistance is the ratio of the change in voltage to the corresponding change in current. The Greek letter (capital) delta Δ is read “change in”. Equation 2-10 shows the change in a given quantity is determined by taking differences. This is defined in Fig. 2-36. Dynamic (and AC) resistance is typically indicated by using a lowercase R (r).

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{V_{Z2} - V_{Z1}}{I_{Z2} - I_{Z1}} \quad (2-10)$$

The Dynamic Resistance

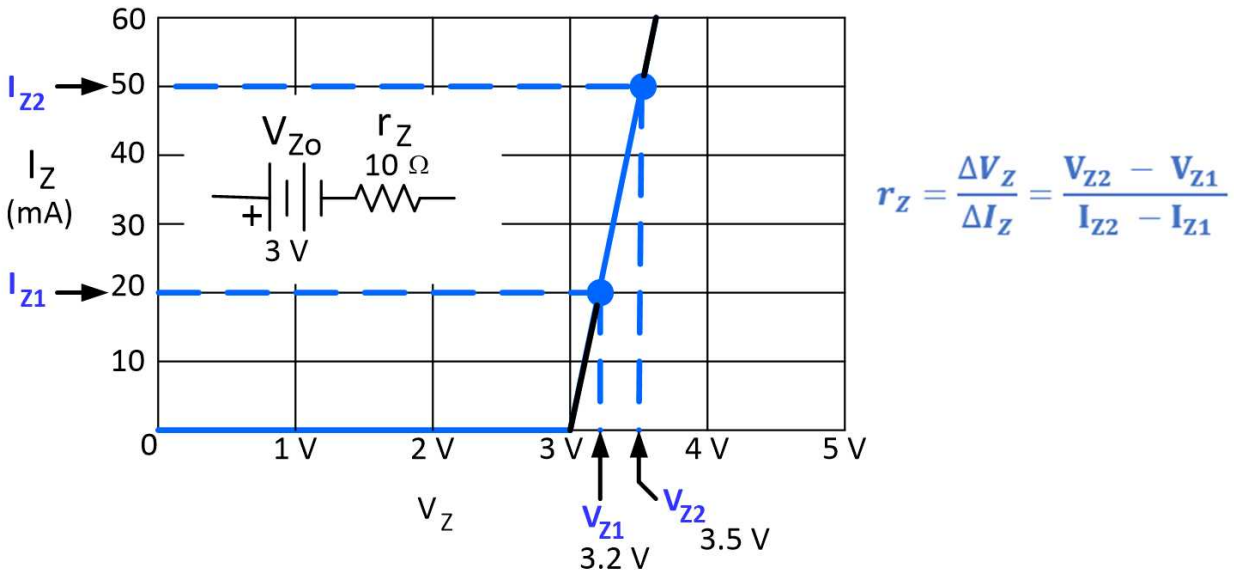


Figure 2-36.

Substituting in the values indicated in Fig. 2-36 into Eq. 2-10 gives us the dynamic resistance.

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{V_{Z2} - V_{Z1}}{I_{Z2} - I_{Z1}} = \frac{3.5 \text{ V} - 3.2 \text{ V}}{50 \text{ mA} - 20 \text{ mA}} = 10 \Omega$$

2-9 The Zener Dynamic-Resistance Diode Model

The zener dynamic resistance¹⁸ diode model improves our approximation of a zener diode in breakdown. Specifically, it includes the variations in the reverse breakdown voltage as the reverse current varies. Figure 2-37 shows the reverse voltage V_Z , and the reverse current I_Z in the first quadrant of the V - I characteristic. This is valid because we are taking V_Z and I_Z as our (positive) reference for zener diodes. (This is consistent with manufacturers' data sheets.)

As can be seen in Fig. 2-37, ***the dynamic resistance zener diode model is a piecewise linear approximation of the actual zener diode characteristic.*** In this case two straight lines are used to represent the actual characteristic.

¹⁸ While we are using a *dynamic resistance* model for the zener diode, many manufacturers use the term *impedance*. Impedance is a general term used to describe the ratio $\Delta V / \Delta I$ in AC applications. In the case of the zener diode, the impedance is purely resistive.

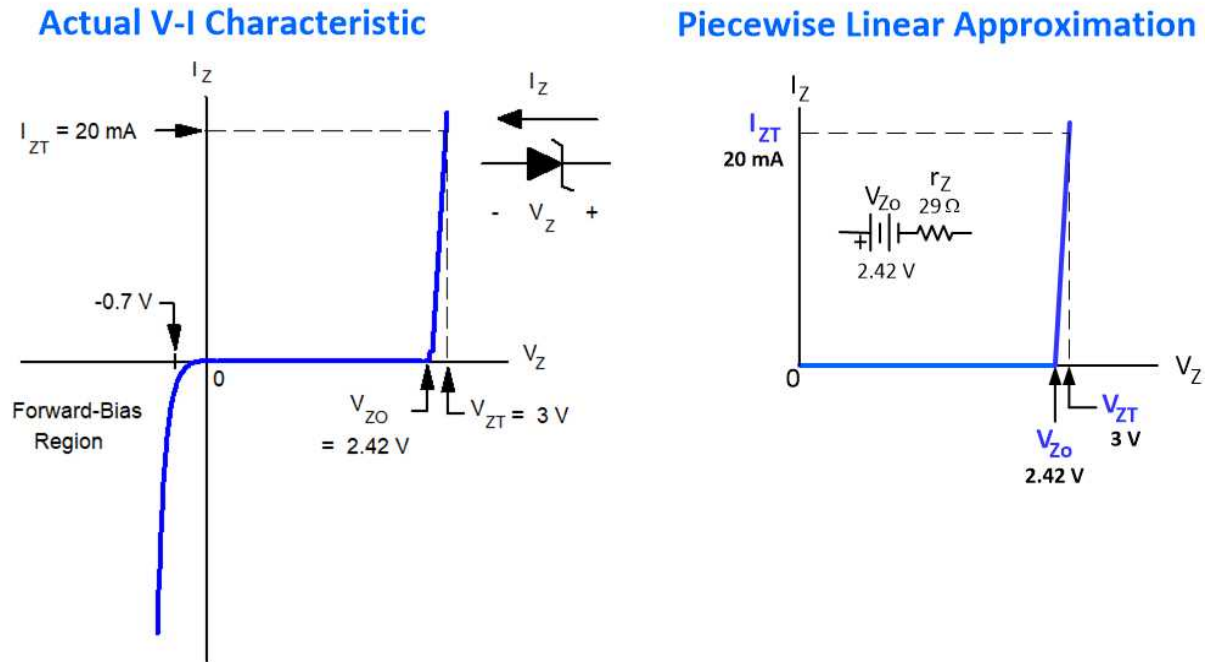


Figure 2-37.

Using the Zener Diode Data Sheet

To obtain the information required to find r_Z and V_{Z0} , we must use the manufacturer's data sheet. A typical, but *partial* data sheet has been provided in Fig. 2-38. The **nominal zener test voltage** is designated as V_Z on the data sheet. However, this quantity is denoted as V_{ZT} on the graph provided in Fig. 2-37. V_{ZT} is the voltage across the zener diode when the zener test current (I_{ZT}) flows.

1N5221 to 1N5267				
Small Signal Zener Diodes				
ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ\text{C}$, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Power dissipation	$T_L \leq 25^\circ\text{C}$	P_{tot}	500	mW
Zener current		I_Z	P_{tot}/V_Z	mA
Thermal resistance junction to ambient air	$l = 4 \text{ mm}$, $T_L = \text{constant}$	R_{thJA}	300	K/W
Junction temperature		T_J	175	$^\circ\text{C}$
Storage temperature range		T_{stg}	-65 to +175	$^\circ\text{C}$
Forward voltage (max.)	$I_F = 200 \text{ mA}$	V_F	1.1	V

Figure 2-38.

Observe the maximum power dissipation is 500 mW. Since zener diodes are made from silicon, the ideal forward voltage drop is 0.7 V. However, because of the diode's resistance, at a large forward current (e.g., 200 mA) the voltage drop can reach a maximum of 1.1 V.

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)								
PART NUMBER	ZENER VOLTAGE RANGE ⁽¹⁾	TEST CURRENT		REVERSE LEAKAGE CURRENT		DYNAMIC RESISTANCE $f = 1\text{ kHz}$		TEMPERATURE COEFFICIENT
	V_Z at I_{ZT1}	I_{ZT1}	I_{ZT2}	I_R at V_R		Z_Z at I_{ZT1} ⁽¹⁾	Z_{ZK} at I_{ZT2}	α_{VZ}
	V	mA		μA	V	Ω		%/K
	NOM.			MAX.		MAX.	MAX.	TYP.
1N5221	2.4	20	0.25	100	1	30	1200	- 0.085
1N5222	2.5	20	0.25	100	1	30	1250	- 0.085
1N5223	2.7	20	0.25	75	1	30	1300	- 0.08
1N5224	2.8	20	0.25	75	1	30	1400	- 0.08
1N5225	3	20	0.25	50	1	29	1600	- 0.075
1N5226	3.3	20	0.25	25	1	28	1600	- 0.07
1N5227	3.6	20	0.25	15	1	24	1700	- 0.065
1N5228	3.9	20	0.25	10	1	23	1900	- 0.06
1N5229	4.3	20	0.25	5	1	22	2000	0.055
1N5230	4.7	20	0.25	5	2	19	1900	0.03
1N5231	5.1	20	0.25	5	2	17	1600	0.03
1N5232	5.6	20	0.25	5	3	11	1600	0.038
1N5233	6	20	0.25	5	3.5	7	1600	0.038
1N5234	6.2	20	0.25	5	4	7	1000	0.045
1N5235	6.8	20	0.25	3	5	5	750	0.05
1N5236	7.5	20	0.25	3	6	6	500	0.058
1N5237	8.2	20	0.25	3	6.5	8	500	0.062
1N5238	8.7	20	0.25	3	6.5	8	600	0.065
1N5239	9.1	20	0.25	3	7	10	600	0.068
1N5240	10	20	0.25	3	8	17	600	0.075

Figure 2-38 (continued).

The acronym JEDEC stands for the Joint Electron Device Engineering Council. This organization establishes the industry standards for part numbers, standard package styles, test circuits and conditions, and parameter symbols. JEDEC part numbers for rectifier, small-signal, and zener diodes begin with 1N¹⁹. The nominal zener voltage V_Z is measured at a given breakdown (test) current called I_{ZT} . Z_Z is the dynamic resistance (r_Z) measured at this DC operating point. Also observe the temperature coefficient is negative below 5 volts and positive above 5 volts. This agrees with the discussion provided in Section 2-6. Zener diodes are available with a suffix (e.g., a 1N5225B). Tolerances in the nominal breakdown voltages associated with the part number suffix are illustrated in Table 2-2.

¹⁹Note that diode part numbers begin with number one (1) and NOT an "I". Beginners sometimes use **IN** by mistake. Some instructors have a pet peeve about this common mistake. It could *raise* his or her ire and *lower* your grade.

Table 2-2 Breakdown Voltage Tolerance

Part Number	Nominal V_{ZT} @ I_{ZT}	Tolerance	Breakdown Voltage Range
1N5240	10 V @ 20 mA	$\pm 20\%$	10 V $\pm$ 2 V
1N5240A	10 V @ 20 mA	$\pm 10\%$	10 V $\pm$ 1 V
1N5240B	10 V @ 20 mA	$\pm 5\%$	10 V $\pm$ 0.5 V
1N5240C	10V @ 20 mA	$\pm 2\%$	10 V $\pm$ 0.1 V

The zener dynamic resistance diode model has been indicated in Fig. 2-39. If we apply KVL, we obtain Eq. 2-11.

$$V_Z = V_{Zo} + I_Z r_Z \quad (2-11)$$

The order of the terms on the right-hand side of the equation is not important.

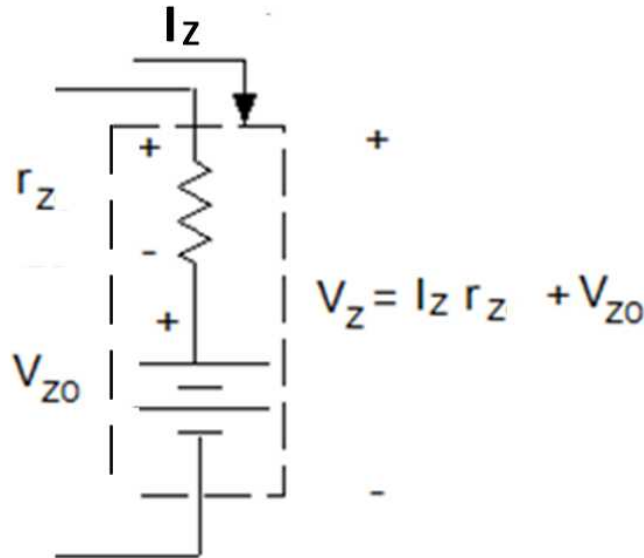


Figure 2-39.

A partial data sheet is included in Fig. 2-40. The data sheet values have been mapped to the zener diode equivalent circuit. The nominal zener voltage (V_{ZT}) is 3 V when the zener test current (I_{ZT}) of 20 mA flows through it, the dynamic resistance (Z_Z) of 29Ω as measured at the zener test current is also given. Equations 2-12 and 2-13 are provided by these observations.

$$V_{ZT} = V_{Zo} + I_{ZT} r_Z \quad (2-12)$$

$$r_Z = Z_Z @ I_{ZT} \quad (2-13)$$

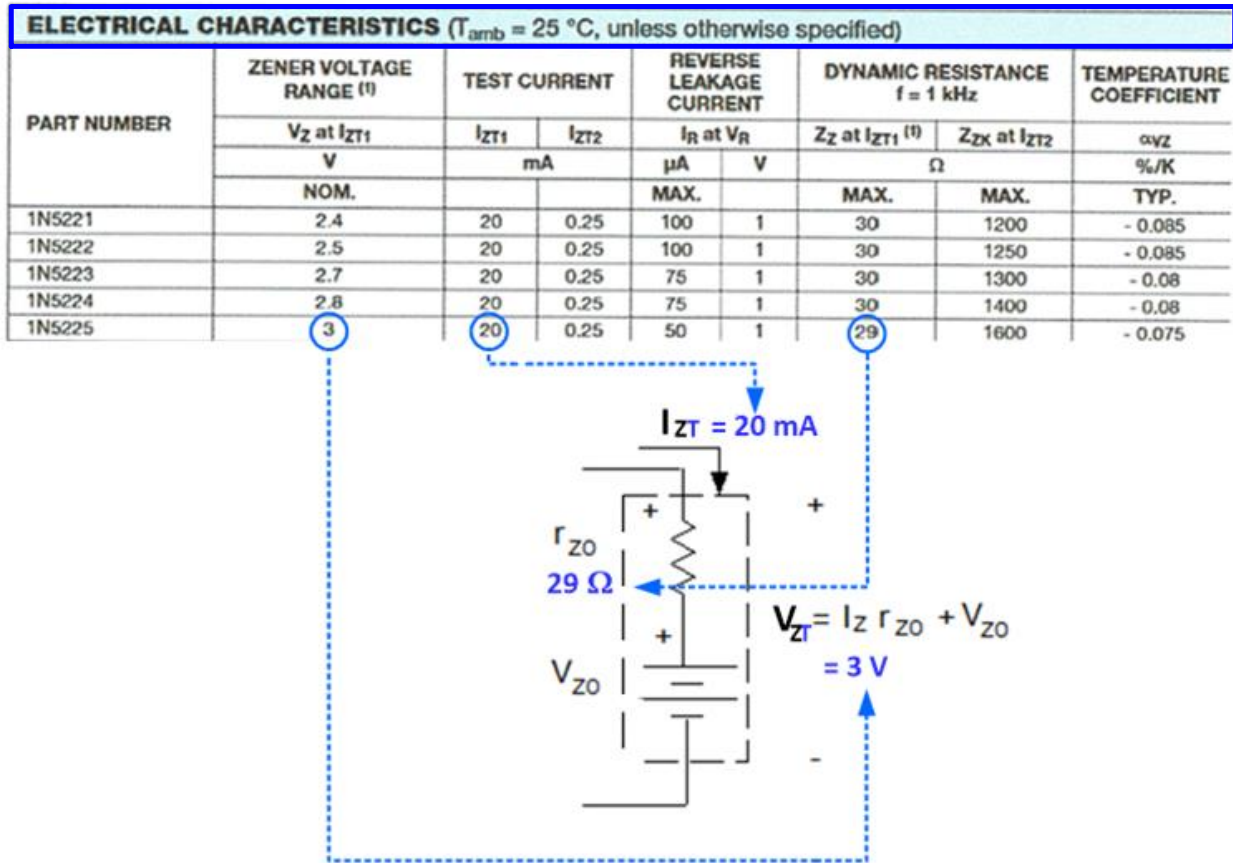


Figure 2-40.

The only unknown quantity for the model is V_{Z0} . We solve Eq. 2-12 for V_{Z0} which yields Eq. 2-14.

$$V_{Z0} = V_{ZT} - I_{ZT}r_Z \quad (2-14)$$

Example 2-11. A 1N5225B zener diode is used in the circuit given in Fig. 2-41(a). Determine its dynamic resistance zener diode model, draw the equivalent circuit, and then determine I_Z and V_Z for the circuit.

Solution: Observe that the zener's nominal breakdown voltage of 3 V has been indicated next to its schematic symbol in Fig. 2-41(a). This is customary practice. We next secure the data sheet for the 1N5225B. It is given in Fig. 2-40. According to the data sheet V_{ZT} is 3 volts at a test current (I_{ZT}) of 20 mA. The zener impedance (Z_Z) is 29 Ω at the test current of 20 mA. Therefore, r_Z is 29 Ω . We apply KVL and find the required offset voltage (V_{Z0}). We use Eq. 2-14.

$$V_{Z0} = V_{ZT} - I_{ZT}r_Z = 3\text{ V} - (20\text{ mA})(29\ \Omega) = 2.42\text{ V}$$

Next, we draw the equivalent circuit as shown in Fig. 2-41(b). Kirchhoff's voltage law and Ohm's law allows us to determine I_Z .

Using the Zener Dynamic Resistance Diode Model

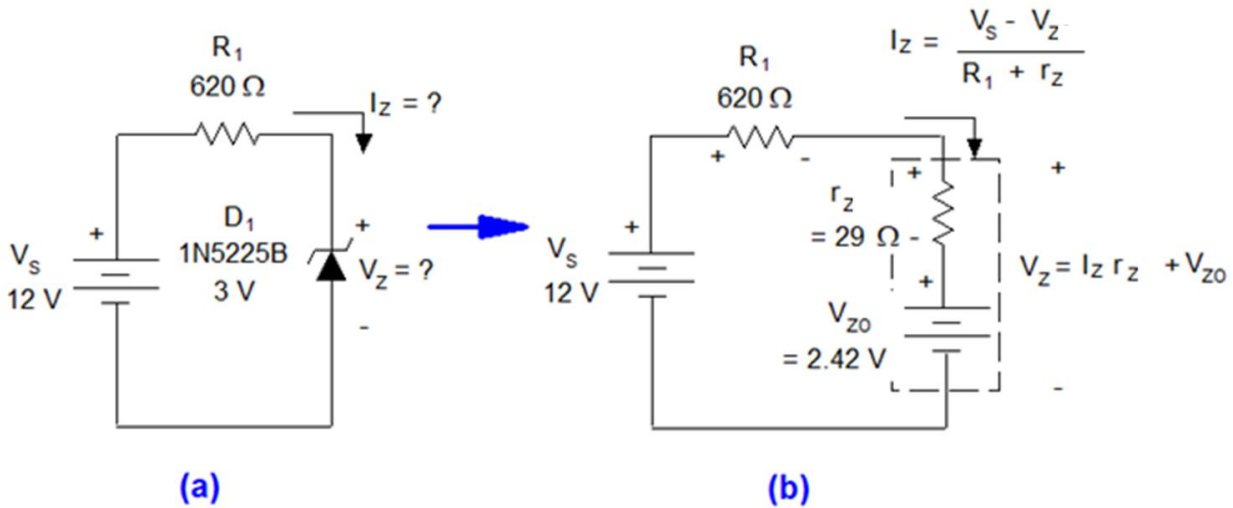


Figure 2-41.

$$I_Z = \frac{V_S - V_{Z0}}{R_1 + r_Z} = \frac{12\text{ V} - 2.42\text{ V}}{620\ \Omega + 29\ \Omega} = 14.8\text{ mA}$$

Now we employ the zener dynamic resistance diode model to compute the voltage across the 1N5225B zener diode.

$$V_Z = V_{Z0} + I_Z r_Z = 2.42\text{ V} + (14.8\text{ mA})(29\ \Omega) = 2.85\text{ V}$$

Because the zener's operating current of 14.8 mA is below its test current of 20 mA, it only drops 2.85 V. This is 5% below its nominal breakdown voltage.

Because of the variation in the zener voltage with reverse current, it is often necessary to employ the zener dynamic resistance model in precision applications. ***The zener dynamic resistance diode model requires an applied reverse voltage, which is greater than V_{Z0} .*** If the reverse bias is insufficient, we treat the zener diode as an open circuit.

The zener dynamic diode model *is* used frequently. This is easy because the zener's dynamic resistance is made available to us on their data sheets. However, just as the knee-voltage diode model is the most often used model to analyze a forward-biased diode, the ideal zener diode model is the usual selection to examine the operation of a reverse-biased zener diode.

2-10 Using Thevenin's Theorem

Thevenin's theorem is a technique that can be used to simplify complex linear circuits. It is used extensively in the analysis of electronic circuits. Because it is so fundamental to our work, we state it briefly.

Thevenin's theorem is based on a property demonstrated by all linear circuits. The theorem states that linear DC circuits containing resistors, and voltage and/or current sources may be resolved into a single equivalent voltage source (V_{TH}) in series with a single equivalent resistance (R_{TH}).

To illustrate the application of Thevenin's theorem to solve electronics circuit problems, consider Example 2-12.

Example 2-12. A 1N4005 silicon rectifier diode is used in the circuit given in Fig. 2-42(a). Find the current through it and the voltage across it.

Solution: To solve this problem we must find the Thevenin equivalent circuit driving the diode, and then determine the appropriate diode model. This will enable us to find I_D and V_D . To find the Thevenin equivalent we disconnect the diode from terminals a and b. Then we compute the open-circuit voltage V_{TH} . Refer to Fig. 2-42(b).

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_S = \frac{2 \text{ k}\Omega}{3 \text{ k}\Omega + 2 \text{ k}\Omega} (15 \text{ V}) = 6 \text{ V}$$

Next, we find the Thevenin equivalent resistance. The voltage source is set to zero by replacing it with a short circuit. We then find the equivalent resistance "looking into" terminals a-b. This is depicted in Fig. 2-42(c).

$$R_{TH} = R_1 \parallel R_2 = 3 \text{ k}\Omega \parallel 2 \text{ k}\Omega = \frac{R_1 R_2}{R_1 + R_2} = \frac{(3 \text{ k}\Omega)(2 \text{ k}\Omega)}{3 \text{ k}\Omega + 2 \text{ k}\Omega} = 1.2 \text{ k}\Omega$$

The linear portion of the original circuit is replaced by its Thevenin equivalent circuit as shown in Fig. 2-42(d). Since the Thevenin equivalent voltage exceeds the knee voltage, we may use the knee-voltage diode model [see Fig. 2-42(e)]. We conclude the problem by noting V_D and calculating I_D .

$$V_D = V_K = 0.7 \text{ V}$$

$$I_D = \frac{V_{TH} - V_K}{R_{TH}} = \frac{6 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 4.42 \text{ mA}$$

As a final comment, we mention that had V_{TH} been less than V_K , we would have modeled the diode as an open switch.

The Circuits for Example 2-12

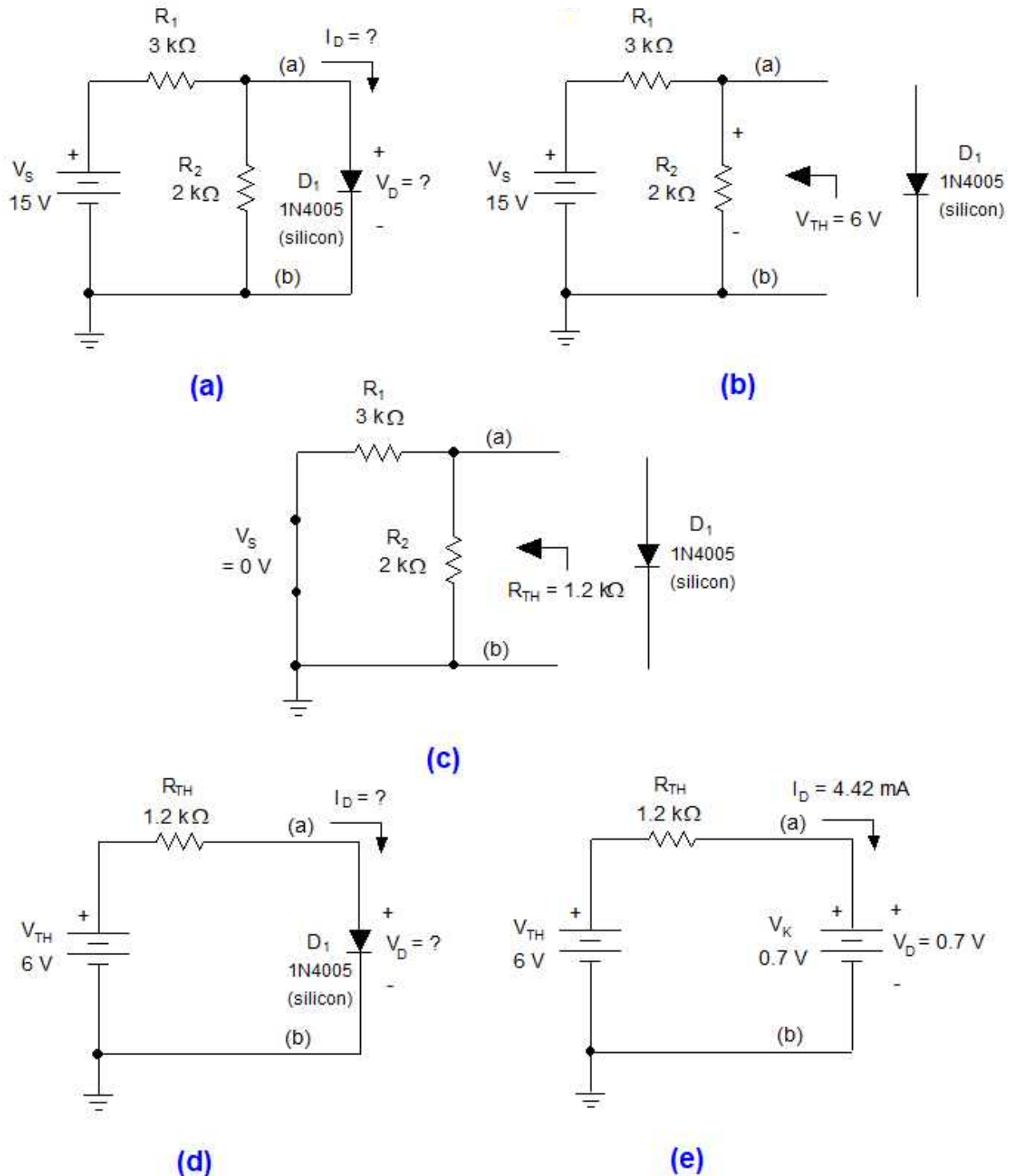


Figure 2-42.

Example 2-13. A 1N4733A 5.1-V zener diode is used in the circuit given in Fig. 2-43(a). Find the current through it and the voltage across it.

Solution: The circuit has been redrawn in Fig. 2-43(b) to consolidate the ground connections. The zener diode is disconnected and we find the Thevenin equivalent circuit “seen” by the diode.

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_S = \frac{3 \text{ k}\Omega}{2 \text{ k}\Omega + 3 \text{ k}\Omega} (30 \text{ V}) = 18 \text{ V}$$

$$R_{TH} = R_1 \parallel R_2 = 2 \text{ k}\Omega \parallel 3 \text{ k}\Omega = 1.2 \text{ k}\Omega$$

The Thevenin equivalent circuit is shown in Fig. 2-43(c). Since V_{TH} exceeds V_Z , we assume the zener diode is in breakdown. The ideal zener diode model is used to give the equivalent circuit shown in Fig. 2-43(d).

$$V_Z = 5.1 \text{ V}$$

$$I_Z = \frac{V_{TH} - V_Z}{R_{TH}} = \frac{18 \text{ V} - 5.1 \text{ V}}{1.2 \text{ k}\Omega} = 11.1 \text{ mA}$$

The Circuits for Example 2-13

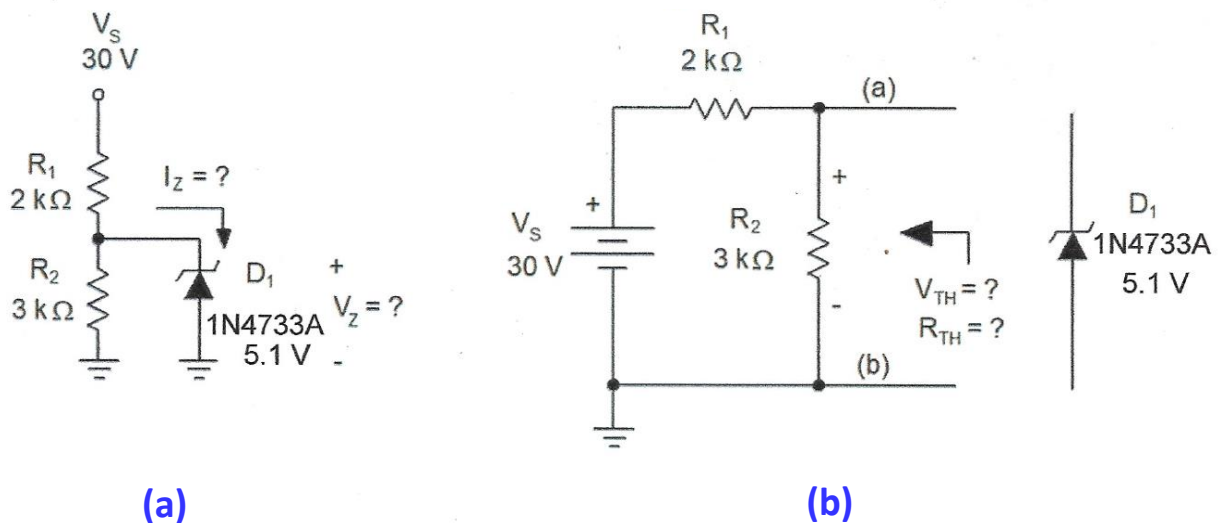


Figure 2-43.

The Circuits for Example 2-13

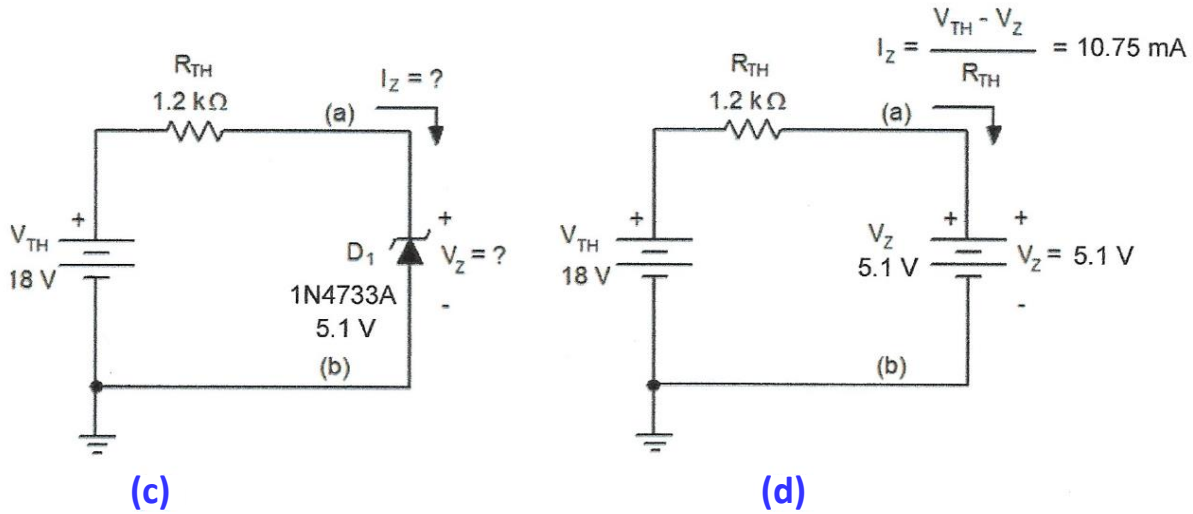


Figure 2-43 (continued).

EDA – Using Multisim

With Thevenin's theorem and our various models, we can solve a variety of problems. Another tool at our disposal is Multisim. Multisim provides an *exponential* approximation of both the forward-bias characteristics and the reverse breakdown mode of operation. In Fig. 2-44, we see the Multisim equivalent circuit and solution for the circuit analyzed in Example 2-13. The 1N4733A 5.1-V zener diode (exponential) model is included in the Multisim library of components.

We run Multisim again as explained previously. We place resistors, a DC voltage source, ground, and the zener diode. We also use digital multimeters to measure the zener current and the voltage across the zener diode. Remember that ammeters act like short circuits and voltmeters act like open circuits. This means no current flows through XMM2 and XMM1 reads the zener diode current.

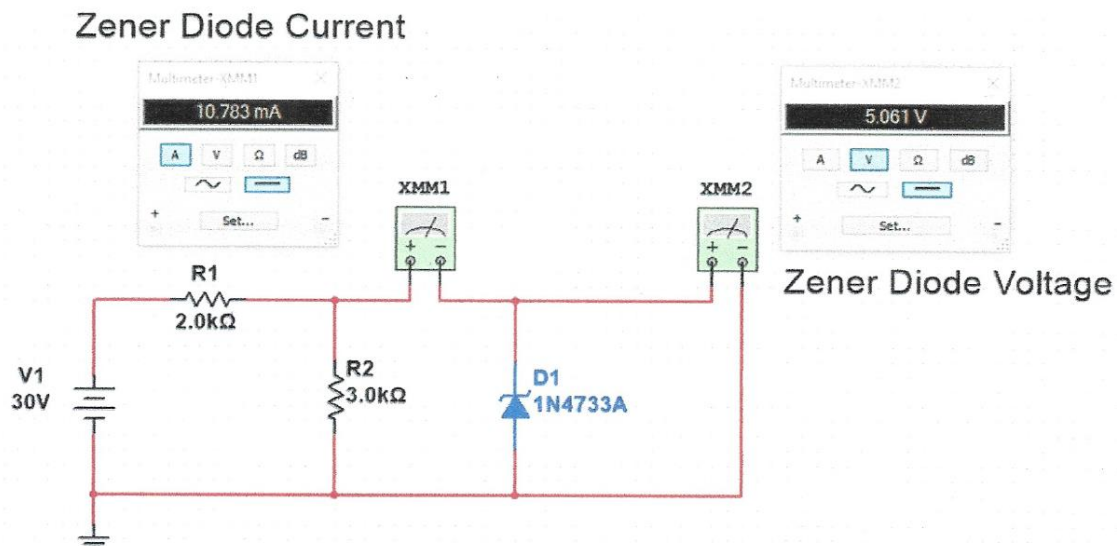


Figure 2-44.

The various components are added as illustrated in Fig. 2-45. We need a DC voltage source [Fig. 2-45(a)], ground [Fig. 2-45(b)], the 1N4733A zener diode [Fig. 2-45(c)] is in the ZENER library, and two resistors [Fig. 2-45(d)].



Figure 2-45.

The components are connected by clicking on Place and Wire as shown in Fig. 2-46. A short cut is available. Place the mouse arrow on a component terminal and the arrow will turn into a dot. Click on the terminal and you will see a wire. Move the wire to the destination terminal and click on that terminal. The two terminals will be wired together.



Figure 2-46.

The suite of virtual laboratory equipment is located on the right-side vertical tool bar. We select a digital multimeter (DMM) to measure the DC current and another for the DC voltage measurement [see Fig. 2-47(a)]. Once the circuit is wired and the instruments are in place, we may RUN (start) the simulation by clicking on the green arrow [Fig. 2-47(b)] at the far left of the top toolbar. The instrument readings are displayed by double clicking on the DMM icons. The simulation is stopped by clicking on the red STOP button. The results should appear as shown in Fig. 2-44.

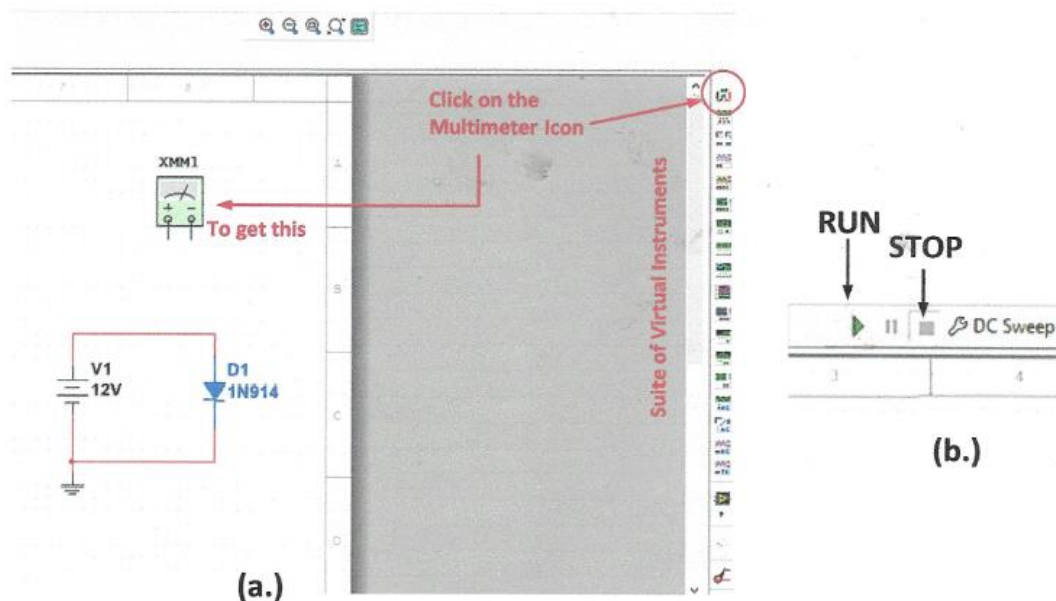


Figure 2-47.

Problems for Chapter 2

Drill Problems

Section 2-1

- 2-1. The *resistance* of a forward-biased diode _____ (increases, decreases) as its forward current increases.
- 2-2. In the case of a rectifier diode the forward-bias portion of its V - I characteristic is normally in the _____ (1st, 2nd, 3rd, 4th) quadrant of the V - I plane.
- 2-3. The knee voltage (V_K) of a silicon diode is _____ (0.2, 0.3, 0.7, 1.6 V) nominally.
- 2-4. The knee voltage (V_K) of a germanium diode is _____ (0.2, 0.3, 0.7, 1.6 V) nominally.
- 2-5. The knee voltage (V_K) of a gallium compound p - n junction is _____ (0.2, 0.3, 0.7, 1.6 V) nominally.
- 2-6. The circuit given in Fig. 2-3 has its V_S adjusted to 12 V. Resistor R_I is changed to a 2-k Ω unit. If V_D is 0.72 V find I_D .
- 2-7. The circuit given in Fig. 2-3 has its V_S adjusted to 25 V. Resistor R_I is changed to a 3-k Ω unit. If V_D is 0.86 V find I_D .
- 2-8. The circuit given in Fig. 2-4 has its V_S adjusted to 35 V. Resistor R_I is changed to a 20-M Ω unit. Find V_R if I_R is 30 nA.
- 2-9. The circuit given in Fig. 2-4 has its V_S adjusted to 15 V. Resistor R_I is changed to a 10-M Ω unit. Find V_R if I_R is 100 nA.

Section 2-2

- 2-10. Assume the reverse saturation current (I_S) of a diode is 0.5 pA. Use the Shockley diode equation to graph its forward V - I characteristic curve. Use Fig. 2-18 as a guide. Show one (1) sample calculation in detail.
- 2-11. Assume the reverse saturation current (I_S) of a diode is 0.05 pA. Use the Shockley diode equation to graph its forward V - I characteristic curve. Use Fig. 2-18 as a guide. Show one (1) sample calculation in detail.
- 2-12. Using the V - I curve data points provided in Table 2-2, graph the forward V - I characteristic curve. Make sure your horizontal axis is ruled out to 3 volts and the vertical axis includes 30 mA. Assume the diode is used in the circuit shown in Fig. 2-19. V_S is 3 V and R_L is 100 Ω . Find V_{OC} and I_{SC} . Superimpose the DC load line on the V - I characteristic curve. Determine the Q point. (Specifically, this means find V_D and I_D .)

- 2-13. Using the V - I curve data points provided in Table 2-2, graph the forward V - I characteristic curve. Make sure your horizontal axis is ruled out to 3 volts and the vertical axis includes 30 mA. Assume the diode is used in the circuit shown in Fig. 2-19. V_S is 3 V and R_L is 150 Ω . Find V_{OC} and I_{SC} . Superimpose the DC load line on the V - I characteristic curve. Determine the Q point. (Specifically, this means find V_D and I_D .)

Table 2-2. V - I Curve Data for Probs. 2-12 and 2-13.

V_D (V)	I_D (mA)
0.75	73
0.7	28
0.65	11
0.6	4
0.55	1.6
0.5	0.6
0.45	0.2
0.4	$\cong 0$
0.35	$\cong 0$
0.3	$\cong 0$
0.25	$\cong 0$
0.2	$\cong 0$
0.15	$\cong 0$
0.1	$\cong 0$
0.05	$\cong 0$
0.0	$\cong 0$

Section 2-3

- 2-14. A diode is forward biased as indicated in Fig. 2-22. The supply voltage V_S is 25 V and R_I is 10 k Ω . Use the ideal diode model to find V_D and I_D .
- 2-15. A diode is forward biased as indicated in Fig. 2-22. The supply voltage V_S is 12 V and R_I is 1 k Ω . Use the ideal diode model to find V_D and I_D .
- 2-16. A diode is reverse biased as indicated in Fig. 2-22. The supply voltage V_S is 25 V and R_I is 1 k Ω . Use the ideal diode model to find V_R and I_R . What are V_D and I_D ?
- 2-17. A diode is reverse biased as indicated in Fig. 2-22. The supply voltage V_S is 12 V and R_I is 1 k Ω . Use the ideal diode model to find V_R and I_R . What are V_D and I_D ?

Section 2-4

- 2-18. A *silicon* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 5 V and R_I is 1 k Ω . Use the knee-voltage diode model to find V_D and I_D .
- 2-19. A *silicon* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 25 V and R_I is 3 k Ω . Use the knee-voltage diode model to find V_D and I_D .
- 2-20. A *germanium* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 5 V and R_I is 1 k Ω . Use the knee-voltage diode model to find V_D and I_D .
- 2-21. A *germanium* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 25 V and R_I is 3 k Ω . Use the knee-voltage diode model to find V_D and I_D .
- 2-22. A *silicon* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 0.5 V and R_I is 3 k Ω . Use the knee-voltage diode model to find V_D and I_D .
- 2-23. A *germanium* diode is forward biased as indicated in Fig. 2-24. The supply voltage V_S is 0.1 V and R_I is 30 k Ω . Use the knee-voltage diode model to find V_D and I_D .

Section 2-5

- 2-24. A reverse-biased diode has an I_R of 0.1 μ A. Given that it is used in Fig. 2-27, find its V_R using the current-source model.
- 2-25. A reverse-biased diode has an I_R of 0.5 μ A. Given that it is used in Fig. 2-27, find its V_R using the current-source model.

Section 2-6

- 2-26. An *n*-type semiconductor that has been doped heavily is denoted as _____ (n , n^+ , or n^-).
- 2-27. A *p*-type semiconductor that has been doped heavily is denoted as _____ (p , p^+ , or p^-).
- 2-28. An *n*-type semiconductor that has been doped lightly is denoted as _____ (n , n^+ , or n^-).
- 2-29. A *p*-type semiconductor that has been doped lightly is denoted as _____ (p , p^+ , or p^-).
- 2-30. A true *zener* diode has a breakdown voltage of _____ (greater than, less than) 5 volts and exhibits a _____ (negative, positive) temperature coefficient.
- 2-31. A true *avalanche* diode has a breakdown voltage of _____ (greater than, less than) 5 volts and exhibits a _____ (negative, positive) temperature coefficient.

Section 2-7

- 2-32. A 5.6-volt zener diode is used in the circuit given in Fig. 2-32. V_S is 15 V and R_I is a 2-k Ω unit. Find I_Z and V_Z using the ideal zener diode model.
- 2-33. A 15-volt zener diode is used in the circuit given in Fig. 2-32. V_S is 25 V and R_I is a 2-k Ω unit. Find I_Z and V_Z using the ideal zener diode model.
- 2-34. A 5.6-volt zener diode is used in the circuit given in Fig. 2-32. V_S is 3 V and R_I is a 20-k Ω unit. Find I_Z and V_Z using the ideal zener diode model.

- 2-35. A 15-volt zener diode is used in the circuit given in Fig. 2-32. V_S is 12 V and R_I is a 200- Ω unit. Find I_Z and V_Z using the ideal zener diode model.
- 2-36. Zener and avalanche diodes are made from _____ (germanium, gallium arsenide, silicon).
- 2-37. A 15-volt zener diode is used in the circuit given in Fig. 2-48. V_S is 20 V and R_I is a 4.7-k Ω unit. Find I_D and V_D .

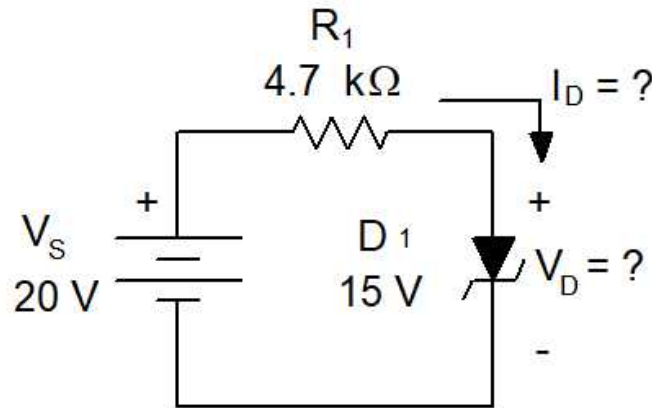


Figure 2-48.

Section 2-8

- 2-38. What is *bulk resistance*? What is *contact resistance*?
- 2-39. Draw the V - I characteristic of a 1-V source in series with a 20- Ω resistor. Use Fig. 2-35 as a guide. Make sure your vertical axis includes 100 mA and your horizontal axis should extend out to at least 5 V. Determine the static (DC) resistance at 20 mA and 70 mA. What is the dynamic resistance?
- 2-40. Draw the V - I characteristic of a 2-V source in series with a 10- Ω resistor. Use Fig. 2-35 as a guide. Make sure your vertical axis includes 100 mA and your horizontal axis should extend out to at least 5 V. Determine the static (DC) resistance at 20 mA and 70 mA. What is the dynamic resistance?

Section 2-9

- 2-41. A 1N5222B zener diode is to be used in a circuit. The circuit is to be analyzed using the zener dynamic resistance diode model. Use the data sheet presented in Fig. 2-38 to find V_{ZO} and r_Z . What is the voltage across a 1N5222B if I_Z is 40 mA?
- 2-42. A 1N5224A zener diode is to be used in a circuit. The circuit is to be analyzed using the zener dynamic resistance diode model. Use the data sheet presented in Fig. 2-38 to find V_{ZO} and r_Z . What is the voltage across a 1N5224A if I_Z is 40 mA?
- 2-43. A zener diode is to be used in the circuit given in Fig. 2-41(a). It is given that V_S is 22 V, R_I is 1 k Ω , V_{ZO} is 14.8 V, and r_Z is 10 Ω . The circuit is to be analyzed using the zener dynamic resistance diode model. Find V_Z and I_Z .

- 2-44. A zener diode is to be used in the circuit given in Fig. 2-41(a). It is given that V_S is 15 V, R_I is 510 Ω , V_{ZO} is 6.4 V, and r_Z is 20 Ω . The circuit is to be analyzed using the zener dynamic resistance diode model. Find V_Z and I_Z .

Section 2-10

- 2-45. A *silicon* diode is used in the circuit given in Fig. 2-42(a). V_S is 12 V, R_I is 5.1 k Ω , R_2 is 10 k Ω . Find the Thevenin equivalent circuit (R_{TH} and V_{TH}) driving the diode. Use the Thevenin equivalent circuit and the knee-voltage diode model to find I_D and V_D .
- 2-46. A *silicon* diode is used in the circuit given in Fig. 2-42(a). V_S is 3 V, R_I is 2 k Ω , R_2 is 1 k Ω . Find the Thevenin equivalent circuit (R_{TH} and V_{TH}) driving the diode. Use the Thevenin equivalent circuit and the knee-voltage diode model to find I_D and V_D .
- 2-47. A 1N4005 rectifier diode is used in the circuit given in Fig. 2-49. Find I_D and V_D . (Hint: Use Thevenin's theorem and the diode's knee-voltage model.)

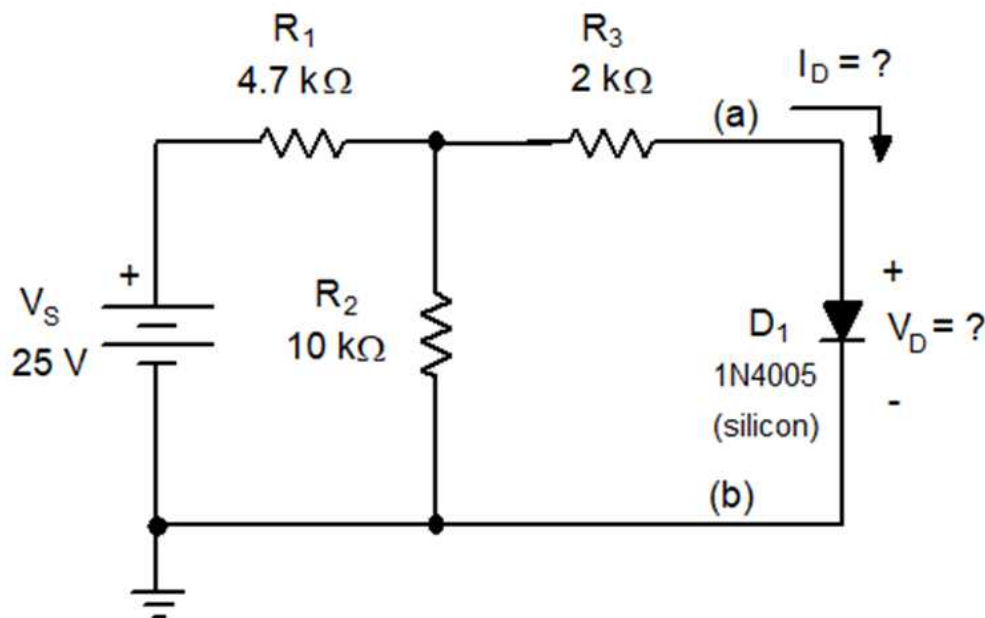


Figure 2-49.

- 2-48. Find I_D and V_D for the diode given in Fig. 2-49. Assume that resistor R_2 is changed to 100 Ω . All other component values are unchanged. (Hint: Use Thevenin's theorem and the diode's knee-voltage model.)
- 2-49. Find I_Z and V_Z for the zener diode given in Fig. 2-50. (Hint: Use Thevenin's theorem and the ideal zener diode model.)

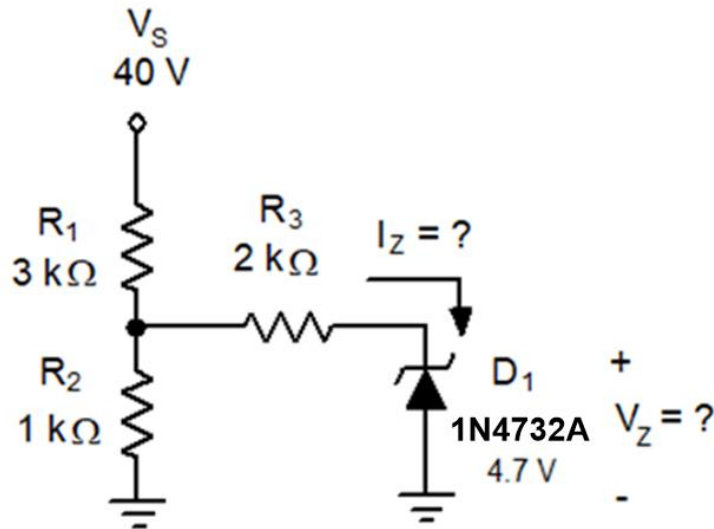


Figure 2-50.

- 2-50. Find I_Z and V_Z for the zener diode given in Fig. 2-50. Assume that V_S is reduced to 10 V. (Hint: Use Thevenin's theorem and the ideal zener diode model.)

EDA Problems

Section 2-1

- 2-51. The 1N914 diode in Fig. 2-17 is to be replaced with an 1N4002G rectifier diode. Use Multisim to obtain its V - I characteristic curve.
- 2-52. The 1N914 diode in Fig. 2-17 is to be replaced with an 1N4009 rectifier diode. Use Multisim to obtain its V - I characteristic curve.

Section 2-10

- 2-53. Use Multisim to obtain the V - I characteristic curve for a 1N4733A zener diode. Use Fig. 2-17 as a reference. (The zener diode should be rotated such that its anode is up.) Run the sweep from -5.5 V to +1 V linearly in steps of 0.01 V. (Hint: Both the forward and reverse bias regions should be shown. The zener diode has a nominal breakdown voltage of 5.1 V.)
- 2-54. Use Multisim to analyze the circuit shown in Fig. 2-49. Use a 1N4005G. Obtain the solution for Prob. 2-47. Specifically, find I_D and V_D . This means a DMM adjusted to measure current should be in series with the diode and a DMM adjusted to measure voltage should be across the diode.
- 2-55. Use Multisim to analyze the circuit shown in Fig. 2-50. Obtain the solution for Prob. 2-49. Specifically, find I_Z and V_Z . This means a DMM adjusted to measure current should be in series with the diode and a DMM adjusted to measure voltage should be across the diode.

3

Diode Applications and Additional Devices

Rectifier and small-signal diodes are found extensively in electronics circuits. Our aim here is to present several representative diode circuit examples. Many of the standard analysis techniques developed in Chapter 2 will be applied. We shall also examine a variety of two-terminal special-purpose solid-state devices. Some are used as transducers to allow electronic systems to operate on non-electrical signals. Others are designed to be optoelectronic displays to promote human interface. The specific topics covered in this chapter include

- Diode Clippers and Limiters
- Diode Clamper Circuits
- Temperature Effects on P - N Junction Operation
- Thermistors and PTCs
- Varistors
- Light-Emitting and Laser Diodes
- Photoconductive Cells, Photodiodes, and Solar Cells
- Frequency Effects on P - N Junction Operation
- The Schottky Diode
- The Varactor Diode

3-0 Study Objectives

After completing this chapter, you should be able to:

- Analyze the operation of diode clipper and limiter circuits.
- Describe the operation and use of diode clamper circuits.
- Use Multisim to analyze clipper and clamper circuits.
- Explain the effects of temperature on forward- and reverse-biased p - n junctions.
- Recognize the frequency limitations on diode switching speed and its effects.
- Describe the operation of the Schottky diode, recognize its schematic symbol, and analyze its operation in a circuit.
- Describe operation of the varactor diode and recognize its schematic symbol.
- Cite the common failure modes of rectifier and zener diodes, and varistors.

3-1 Diode Clippers and Limiters

Diodes are often used to *clip* or *limit* voltage signals. One such application is shown in Fig. 3-1. The diodes are 1N4148 small-signal silicon units. The triangular symbol is used to represent an *amplifier*. Although we begin our study of amplifiers in Chapter 8, let us digress slightly to explain its role.

An amplifier is designed around devices such as discrete transistors and/or linear integrated circuits. Its sole function is to take small (voltage) signals and make them larger. It should make the signals larger *without* altering their shape. An amplifier that alters the shape of an input signal is said to produce *distortion*. Ideally, a voltage amplifier should not draw an appreciable current from its signal source. Stated another way, this means *the amplifier's input should act like an open circuit*. When an amplifier is being driven by an *external signal source*, it may be desirable to protect its input from receiving a signal that is too large. [An *external signal source* might be a compact disk (CD) or an MP3 player for instance.] A diode clipper circuit can be used to protect the amplifier's input as shown in Fig. 3-1.²⁰

A Diode Clipper Used to Protect an Amplifier's Input

A small "safe" signal.

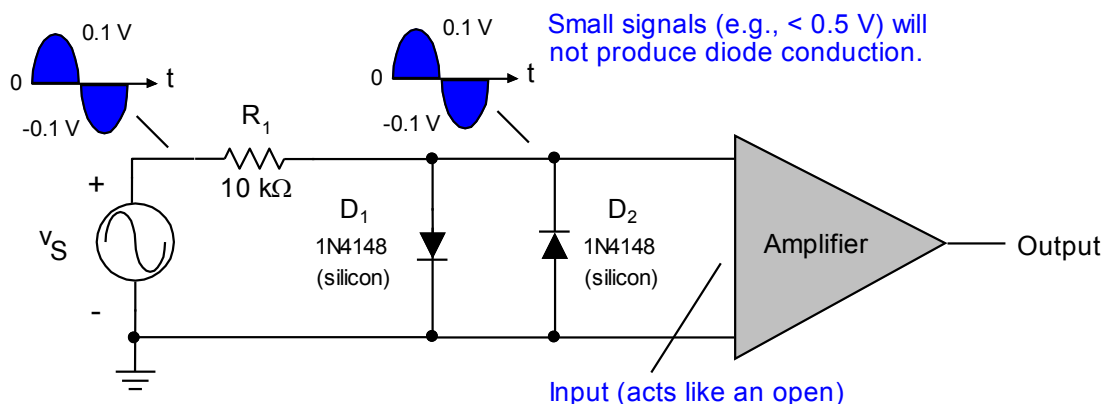


Figure 3-1

During the positive half-cycle of the input signal, diode D_1 is forward biased. During the negative half-cycle of the input signal, diode D_2 is forward biased. The diodes will not be biased into conduction with low-level inputs (e.g., less than 0.1 V peak).

Recall that the knee-voltage model has us replace a diode with an open switch when the applied forward bias is less than the diode's knee voltage (e.g., 0.7 V for a silicon diode). Typically, a "real" silicon diode will not produce significant conduction for a forward bias that is less than about 0.5 V . This is reflected in the equivalent circuit shown in Fig. 3-2(a). This means *the presence of the protective diodes will not affect the circuit's operation provided the input signals are small*.

²⁰An amplifier with a protected input is a "happy" amplifier. However, anything we can do to make an electronic system more "forgiving" the longer it will last and customer satisfaction reigns supreme. Whenever input signals are produced externally, it is essential to provide input protection.

The Diode Clipper in Action

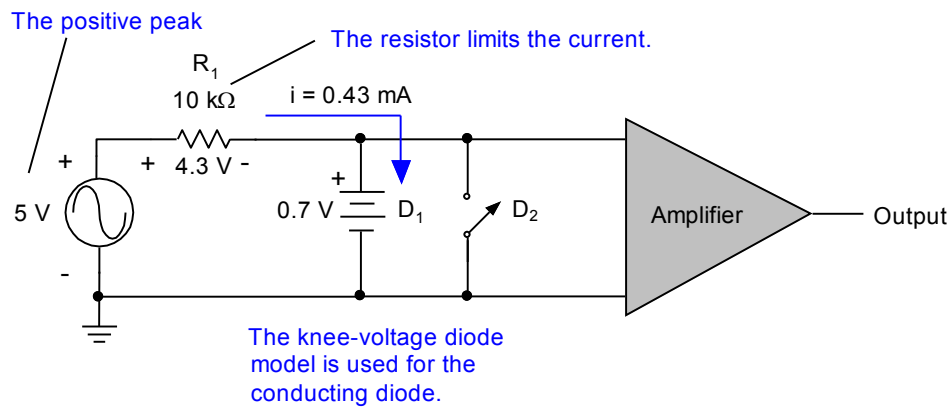
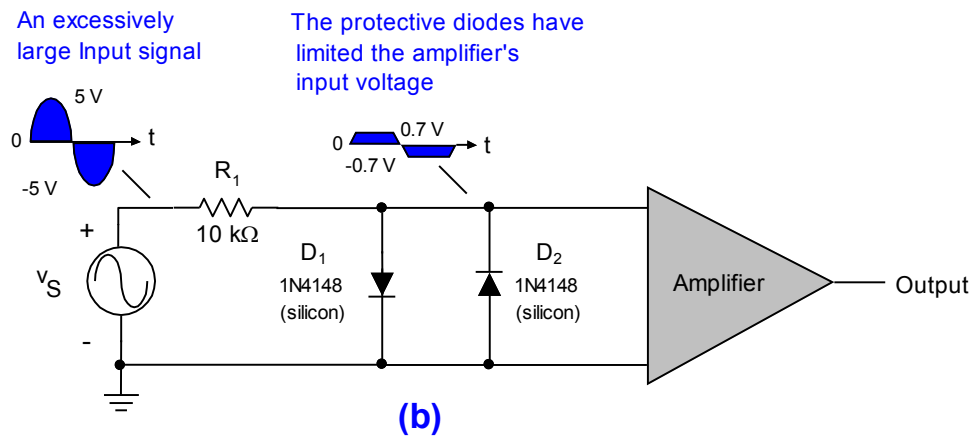
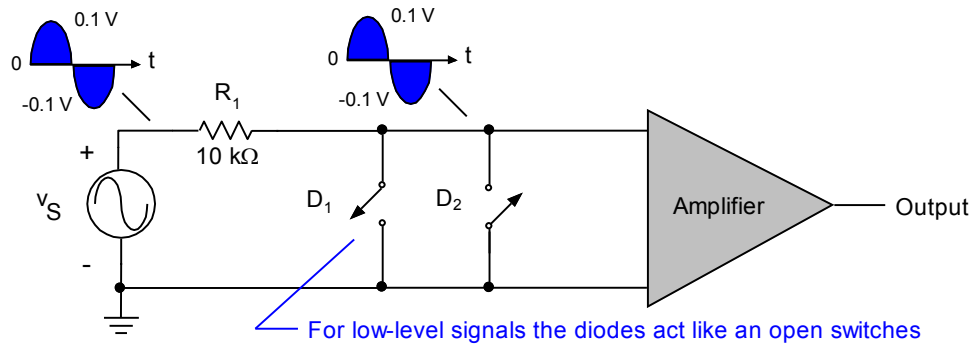


Figure 3-2

If the input signal becomes too large (e.g., 5 V peak), the diodes will go into conduction. This is shown in Fig. 3-2(b). During the positive half-cycle, diode D_1 goes into conduction to limit the amplifier's input voltage to 0.7 V. During the negative half-cycle, diode D_2 goes into conduction to limit the amplifier's input voltage to -0.7 V. The voltage waveform across the amplifier's input will be clipped as indicated in Fig. 3-2(b). The purpose of resistor R_1 is to limit the currents through the diodes. Figure 3-2(c) shows the peak current will be limited to 0.43 mA.

A Biased Diode Clipper Circuit

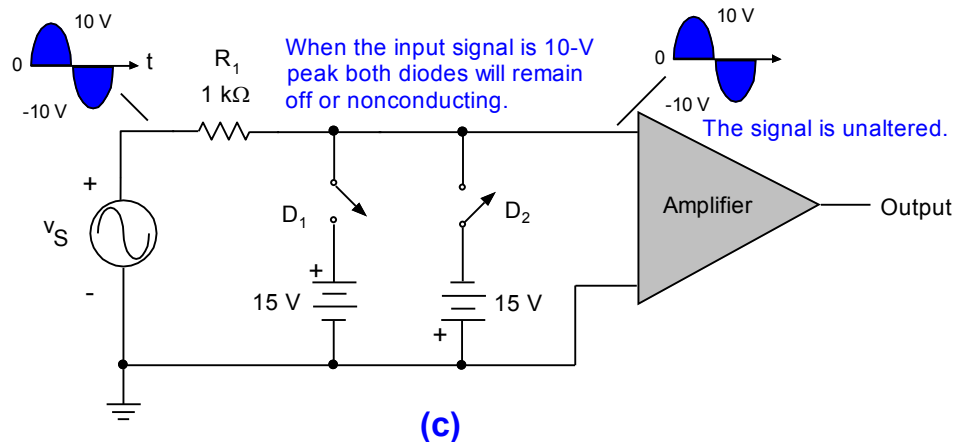
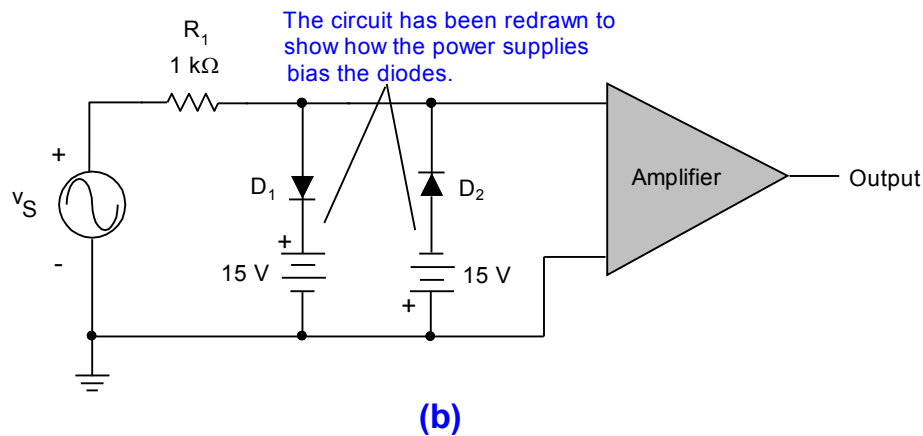
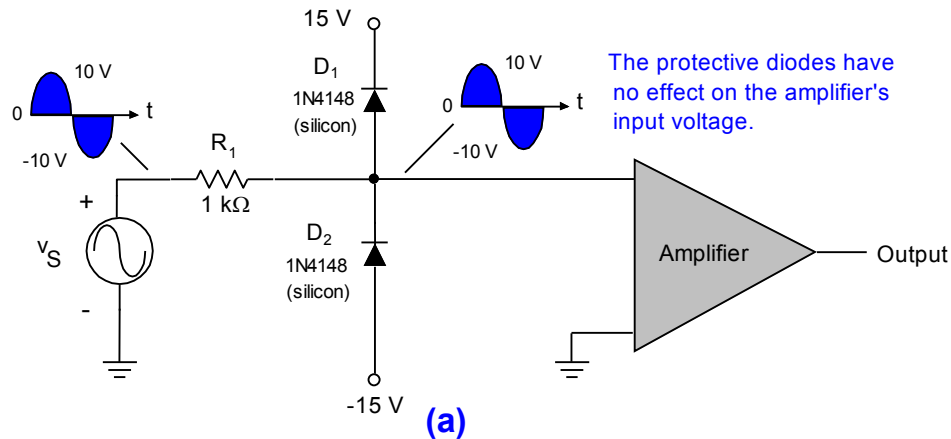


Figure 3-3

Diode clippers can be biased to limit signals to significantly larger peak values [see Fig. 3-3(a)]. In this application, it is assumed the normal input signals are on the order of 10 V peak. The circuit has been redrawn in Fig. 3-3(b). As can be seen in Fig. 3-3(c), for inputs of 10 V peak both diodes are nonconducting. *This means the input signal will be unaffected by the presence of the diode clipper circuit.* Diode D_1 remains off because its anode never becomes *more positive* than its cathode. Diode D_2 remains off because its cathode never becomes *more negative* than its anode. Think about these two statements carefully.

In Fig. 3-4 we see the effects of diode conduction. The large input signal is clipped or limited to 15.7 V peak. At the positive peak, the anode of diode D_1 becomes 0.7 V more positive than its cathode. This causes diode D_1 to conduct. During the negative cycle, the cathode of diode D_2 becomes 0.7 V more negative than its anode. This causes diode D_2 to conduct.

The Biased Diode Clipper Circuit Limits the Signal Reaching the Amplifier's Input

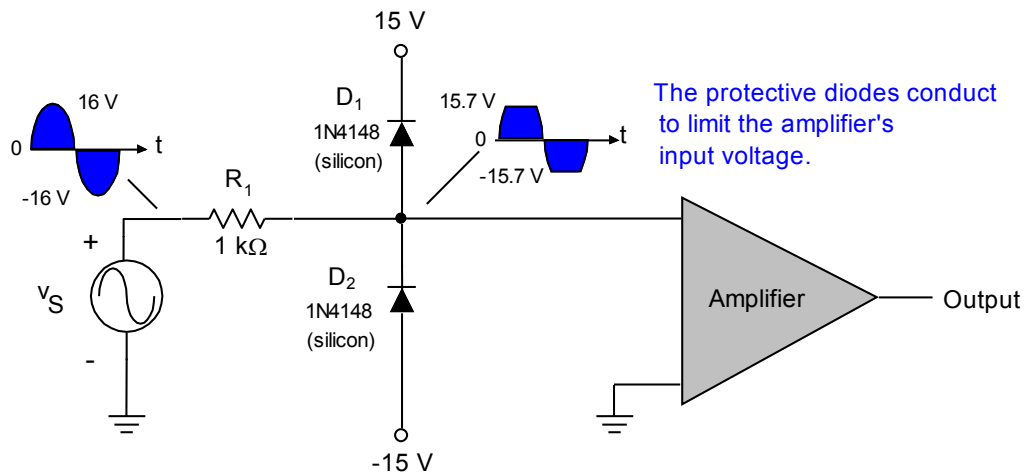


Figure 3-4.

If we represent diode D_1 by its knee-voltage model, we obtain the equivalent circuit shown in Fig. 3-5(a). Diode D_2 is clearly reverse biased and acts like an open switch. Its cathode is taken to +15.7 V by the limiting action of diode D_1 . Since its anode is biased to -15 V, this means the reverse bias across diode D_2 is 30.7 V. Examine Fig. 3-5(a) carefully.

Using the Knee-Voltage Diode Model to Analyze the Biased Diode Clipper Circuit

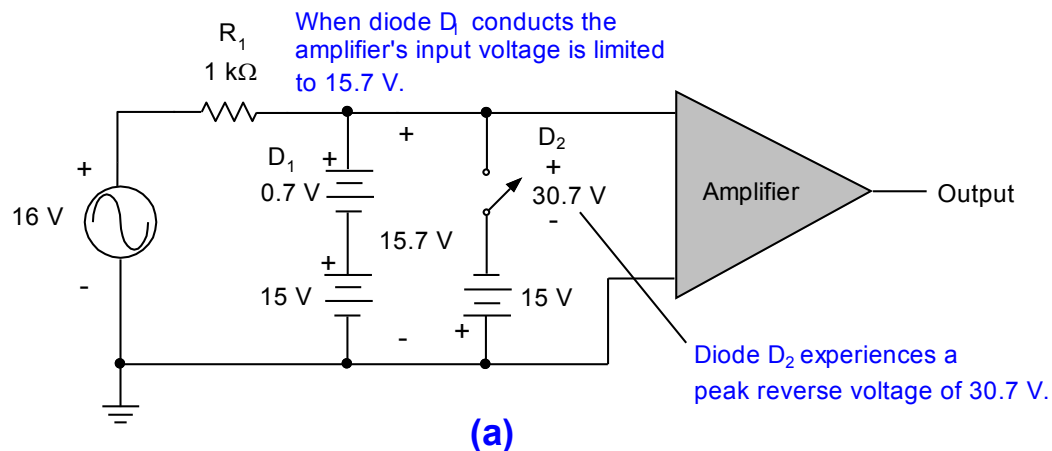


Figure 3-5.

The situation is reversed in Fig. 3-5(b). When the signal becomes negative enough diode D_2 goes into conduction to limit the input voltage level to -15.7 V . Diode D_1 will also receive a reverse bias of 30.7 V .

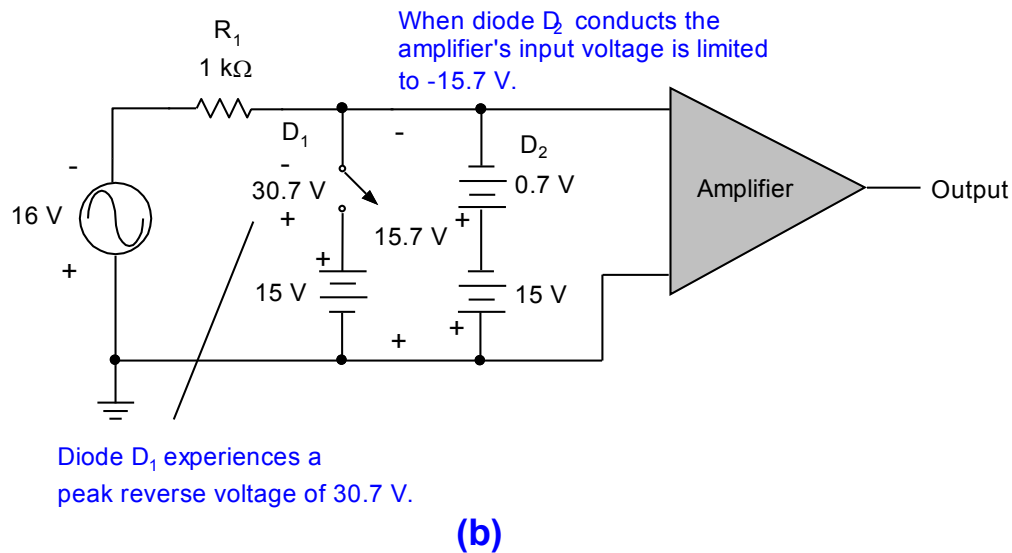


Figure 3-5 (continued).

3-2 Diode Clamper Circuits

A **diode clamper circuit** is shown in Fig. 3-6. The clamper circuit is also referred to as a **DC restorer** or a **signal level shifter**. It provides us with the background necessary to understand the **gate-leak bias** techniques used in (field-effect transistor) sinusoidal oscillator circuits.

As can be seen in Fig. 3-6, the 1-kHz input signal v_s is pure AC. Specifically, it has a DC level of zero. However, at the circuit's output (taken across the diode) the AC signal is riding on a 4.3-V DC level. The operation of this circuit is detailed in Fig. 3-7(a) and (b).

The Diode Clamper Circuit

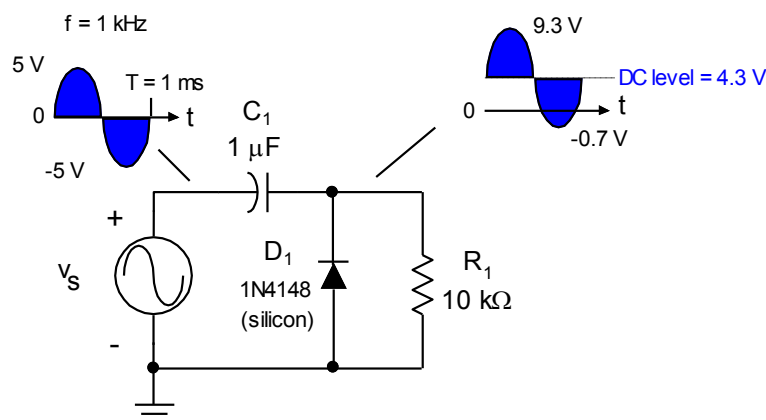


Figure 3-6.

Diode Clamper Circuit Operation

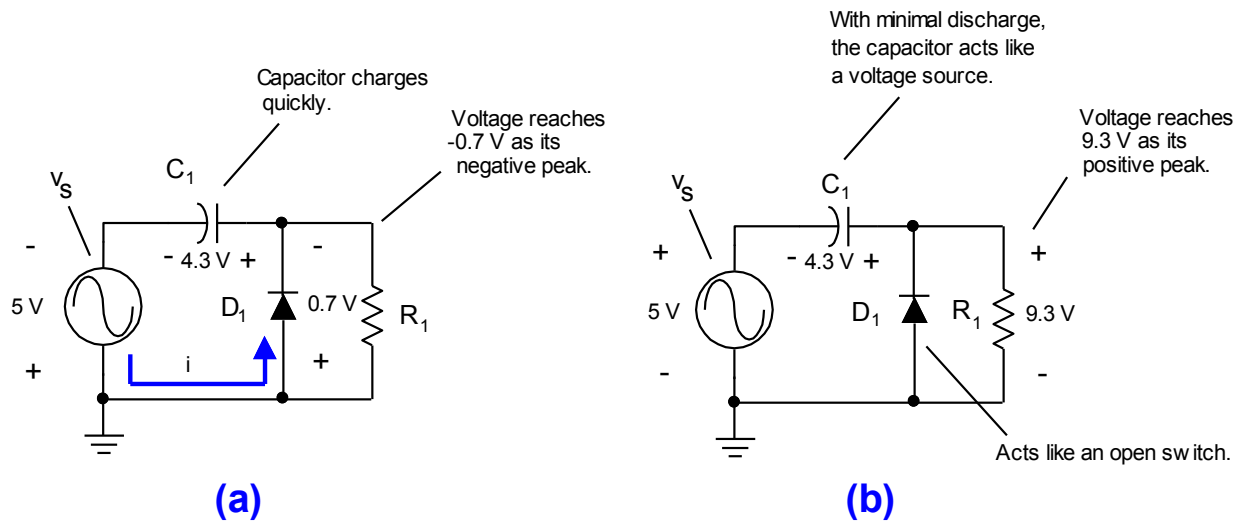


Figure 3-7.

When the signal reaches its negative peak (-5V) the diode is forward biased, and the capacitor charges quickly to 4.3 V [see Fig. 3-7(a)]. The charging time is very small since the diode's forward resistance is very low. When the signal reaches its positive peak (5 V), the diode is reverse biased. Consequently, the capacitor will discharge through the resistor. The discharge time constant ($R_1 C_1$) is very large. The design criterion for the circuit is given by Eq. 3-1.

$$\tau = R_1 C_1 \geq 10T \quad (3-1)$$

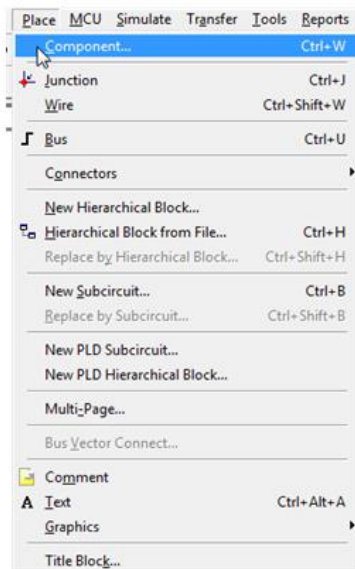
where τ (Greek letter tau) is the time constant and T is the period of the *lowest* signal frequency to be level shifted.

Equation 3-1 specifies the minimum discharge R - C time constant needs to be at least ten times longer than the longest signal period. This will ensure the capacitor will never discharge significantly when the circuit is operating. For example, in Fig. 3-6 we have a T of 1 ms and a τ of 10 ms. In Fig. 3-7(b) we see that the capacitor acts like a DC voltage source. Its voltage adds to v_s . At the signal's positive peak, the total instantaneous voltage across the diode is 9.3 V.

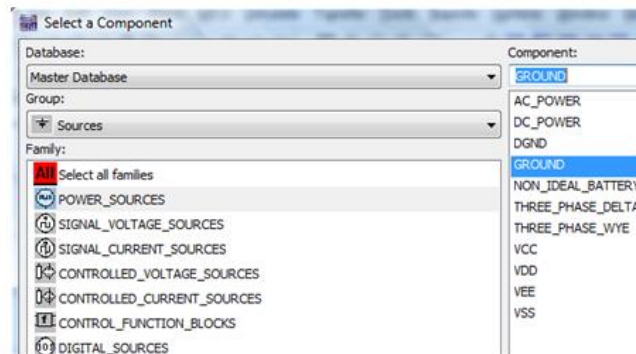
Multisim Can Be Used to Perform a Transient Analysis of the Clamper

Multisim can be employed to analyze the clamper circuit given in Fig. 3-6. We click on Place and then select component. This is shown in Fig. 3-8(a). We select Sources Group and then choose POWER_SOURCES. We add GROUND and AC_POWER as shown in Fig. 3-8(b).

Click on Place
and then select
Component.



(a.)

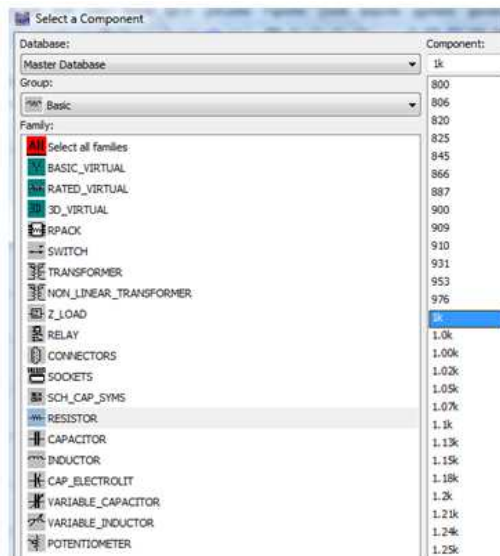


(b.)

Select the Sources Group and the choose
Power Sources. Add Ground and AC_POWER.

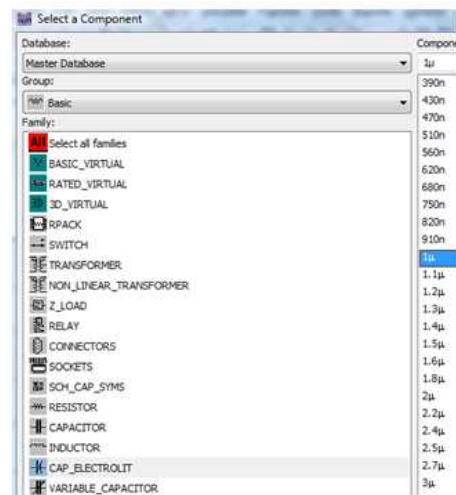
Figure 3-8.

From the Basic Group we add a resistor and an electrolytic capacitor. Remember an electrolytic capacitor is polarized, can only have a DC voltage impressed across it. This is illustrated in Fig. 3-9.



Select the Basic Group
and add a resistor.

(a.)



Next we add an electrolytic capacitor.

(b.)

Figure 3-9.

Position the parts as shown in Fig. 3-11. Figure 3-10 shows how to flip and rotate highlighted (selected) components. Remember the Ctrl-R keys (depressed simultaneously) can be used to rotate the parts as needed. This shortcut is indicated in Fig. 3-10(a).

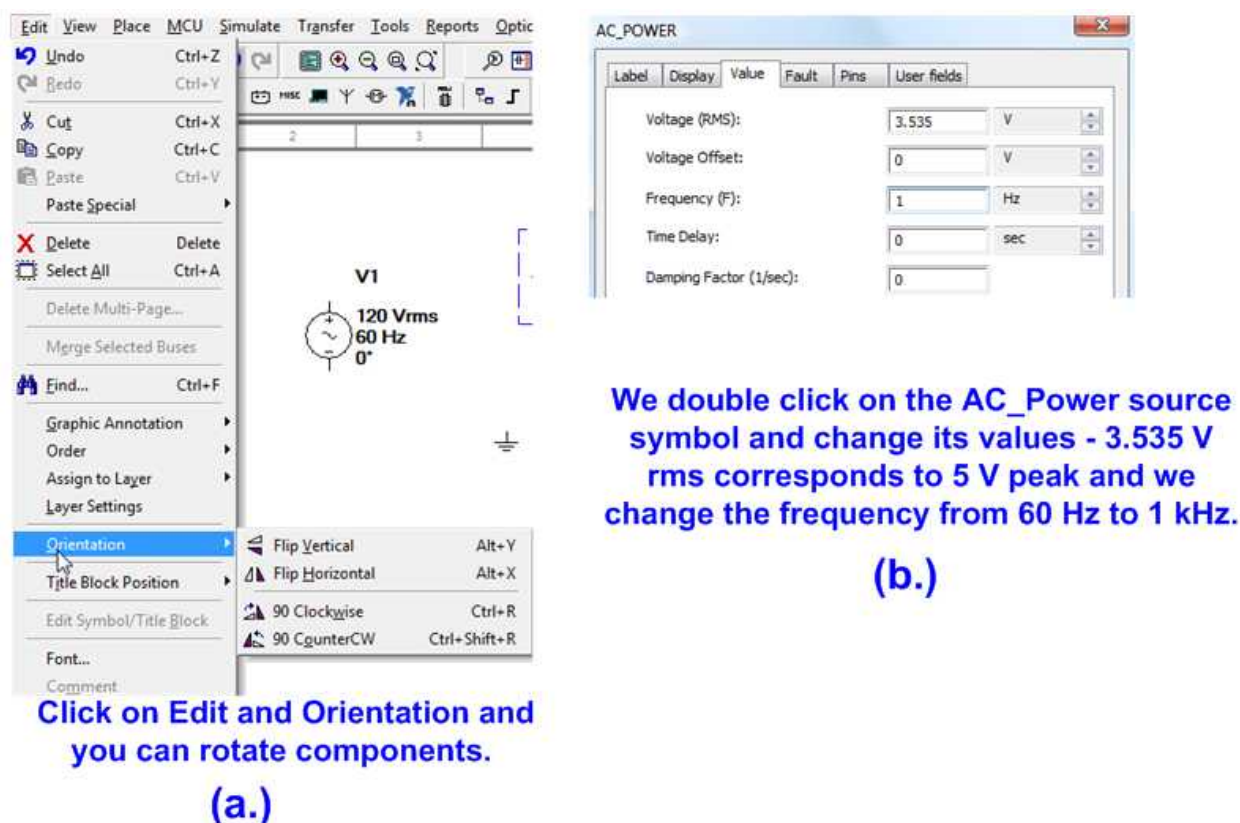


Figure 3-10.

By double clicking on the source and the resistor, we can edit their values as illustrated in Fig. 3-10(b). An oscilloscope is used to observe the voltage waveform across the resistor [see Fig. 3-11].

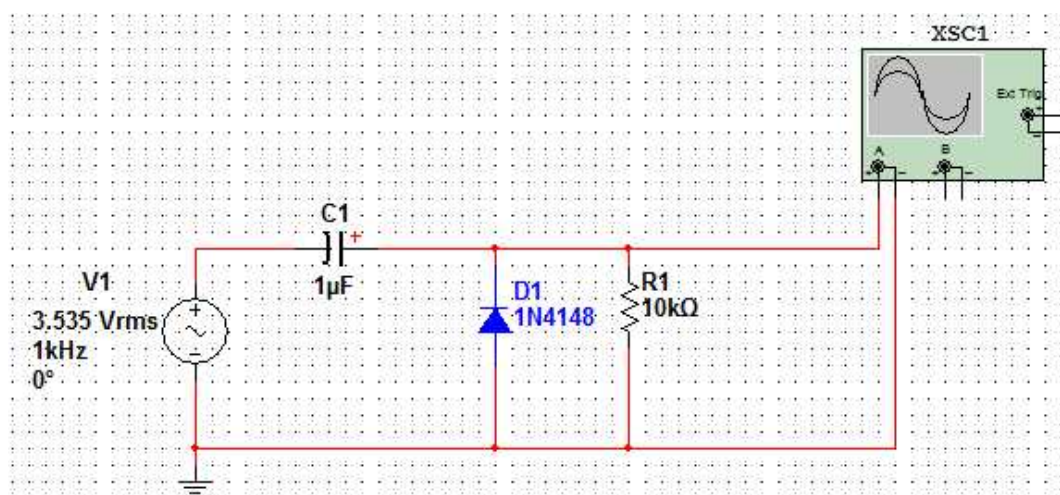


Figure 3-11.

The waveform is shown in Fig. 3-12. A single (Sign.) sweep is used to capture the start-up transient. The initial positive half-cycle does not cause diode conduction. The first negative half-cycle causes a large diode current to flow which results in the charge of the capacitor. From that point on the diode conduction replenishes the capacitor charge.

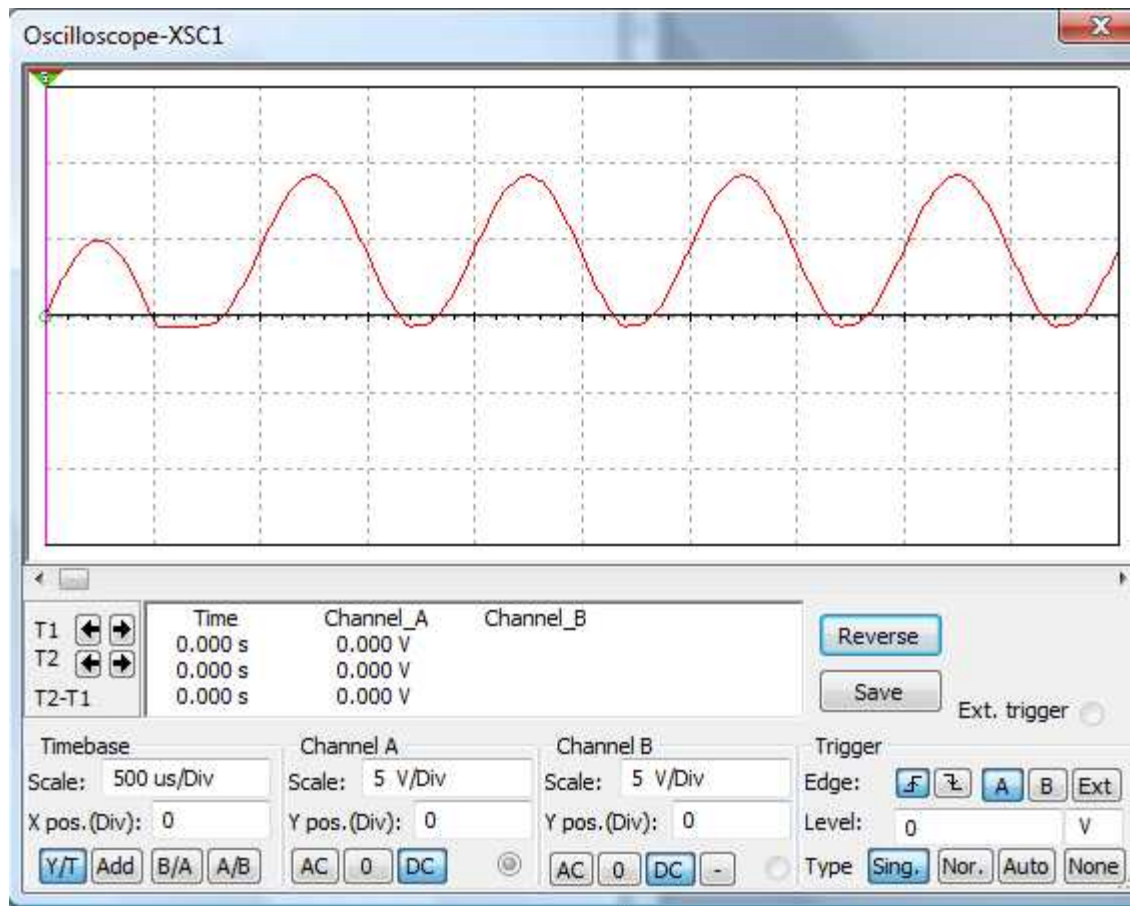


Figure 3-12.

3-3 Temperature Effects on *P-N* Junction Operation

The *p-n* junction is fundamental to the operation of virtually all solid-state devices. Understanding the effects of temperature on the *p-n* junction can therefore be extended to many solid-state devices. Knowing how temperature affects the operation of diodes and transistors, will help us understand concepts such as *temperature compensation* and *bias stability* as applied to transistor and integrated circuit amplifiers. We focus here on the diode.

The forward V - I characteristic of a diode is a strong function of temperature. Temperature changes significantly alter the barrier potential. As the junction temperature is *increased*, the forward voltage drops required to push a given current through the diode will *decrease*. Consider Fig. 3-13. Since the voltage decreases with increasing temperature, it is described as having a **negative temperature coefficient** (or a negative “tempco” for short). It has been found that the forward voltage drop across a *silicon* p - n junction decreases about $1.8\text{ mV per degree Celsius}$ (or a temperature coefficient of $-1.8\text{ mV/ }^{\circ}\text{C}$). Germanium demonstrates a negative temperature coefficient of approximately $-2.02\text{ mV/ }^{\circ}\text{C}$. Typically, **a tempco of $-2\text{ mV/ }^{\circ}\text{C}$ is used for both silicon and germanium**. This is stated by Eq. 3-2.

$$V_D(T) = V_D(25^{\circ}\text{C}) - \frac{2\text{ mV}}{^{\circ}\text{C}}(T - 25^{\circ}\text{C}) \quad (3-2)$$

where $V_D(T)$ is the forward voltage drop at temperature T ,
 $V_D(25^{\circ}\text{C})$ is the forward voltage drop at 25°C , and
 T is the temperature in $^{\circ}\text{C}$

Note that *functional notation* is being used here. Specifically, $V_D(T)$ is the voltage across the diode as a function of temperature. **The notation $V_D(T)$ does NOT mean multiply the voltage times the temperature T .**

Example 3-1. A silicon diode has a forward voltage drop of 0.7 V at 25°C . Determine its voltage drop at 45°C and at 15°C .

Solution: We apply Eq. 3-2 to determine the forward voltage drops.

$$V_D(T) = V_D(25^{\circ}\text{C}) - \frac{2\text{ mV}}{^{\circ}\text{C}}(T - 25^{\circ}\text{C})$$

Hence, at 45°C we obtain the result below.

$$V_D(T) = 0.7\text{ V} - \frac{2\text{ mV}}{^{\circ}\text{C}}(45^{\circ}\text{C} - 25^{\circ}\text{C}) = 0.7\text{ V} - 0.04\text{ V} = 0.66\text{ V}$$

We repeat the analysis at 15°C .

$$V_D(T) = 0.7\text{ V} - \frac{2\text{ mV}}{^{\circ}\text{C}}(15^{\circ}\text{C} - 25^{\circ}\text{C}) = 0.7\text{ V} + 0.02\text{ V} = 0.72\text{ V}$$

The Effect of Temperature on a Forward-Biased Silicon Diode (a tempco of $-2 \text{ mV } ^\circ \text{C}$)

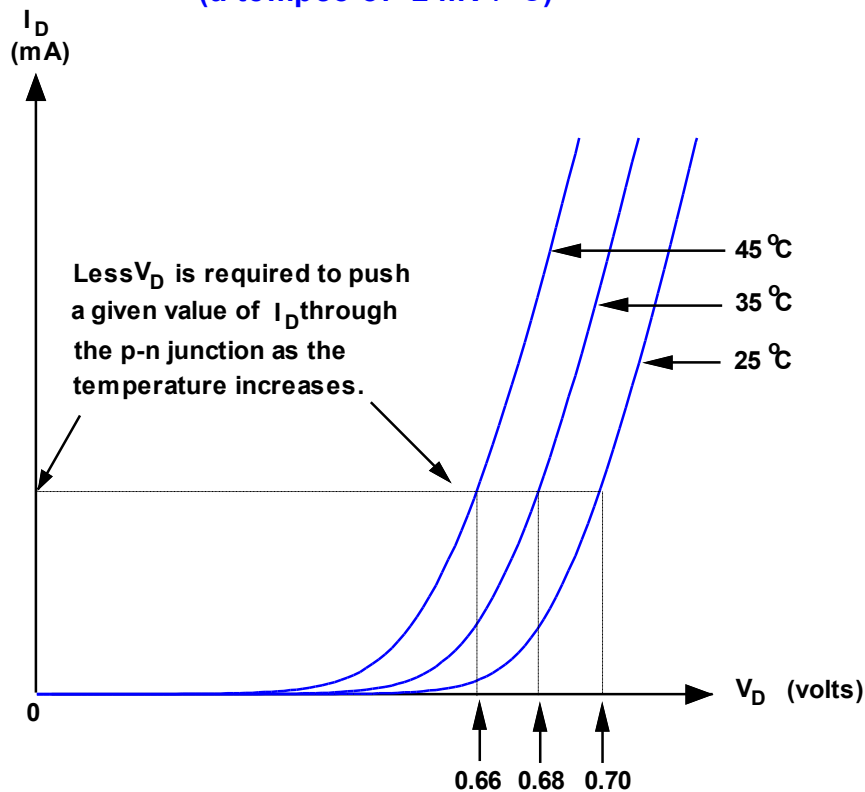


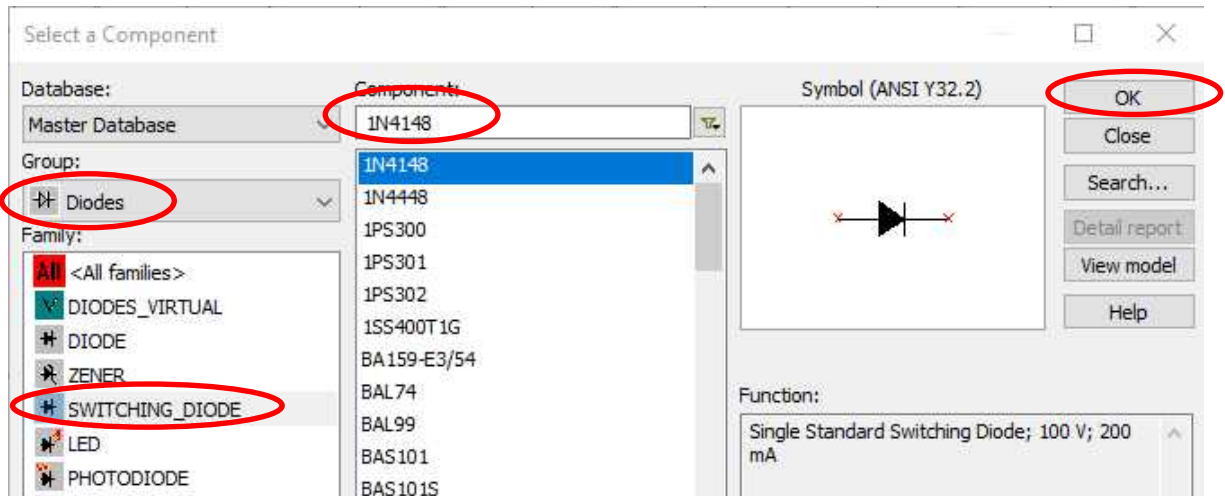
Figure 3-13.

Multisim Can Be Used to Observe the Effects of Temperature

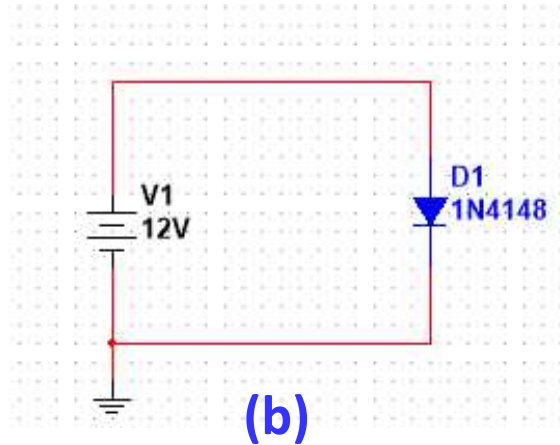
The reader is advised review the subsection “Using EDA to Produce the V - I Curve” included in Section 2-1 “The Diode V - I Characteristic Curve.” We will use a DC sweep to generate the V - I characteristic curve for a 1N4148 (switching) diode.

It is possible to have Multisim analyze a circuit at multiple temperatures. The solid-state device models (e.g., for diodes and transistors) used by Multisim include provisions to handle the effects of temperature. While resistors, capacitors, and inductors are also affected by temperature, Multisim assumes these components do not change with temperature unless we define some of the other built-in component models. We will not worry about the other component models at this point. It is important to understand that integrated circuits do not typically include provisions for temperature effects. The Multisim circuit is provided in Fig. 3-14(a).

We are using a 1N4148 switching diode. Click on **Place Component**. Select **Diodes** and **Switching Diodes**. Select the **1N4148**. Click on **OK** [Fig. 3-14(b)]. Place diode on the sheet and wire it to the DC voltage source and ground.



(a)



(b)

Figure 3-14.

The default temperature in Multisim is 27°C. Generate a graph of its V - I characteristic curve. We can generate another analysis at 50°C as shown in Fig. 3-15. A comparison of the two graphs is given in Fig. 3-16.

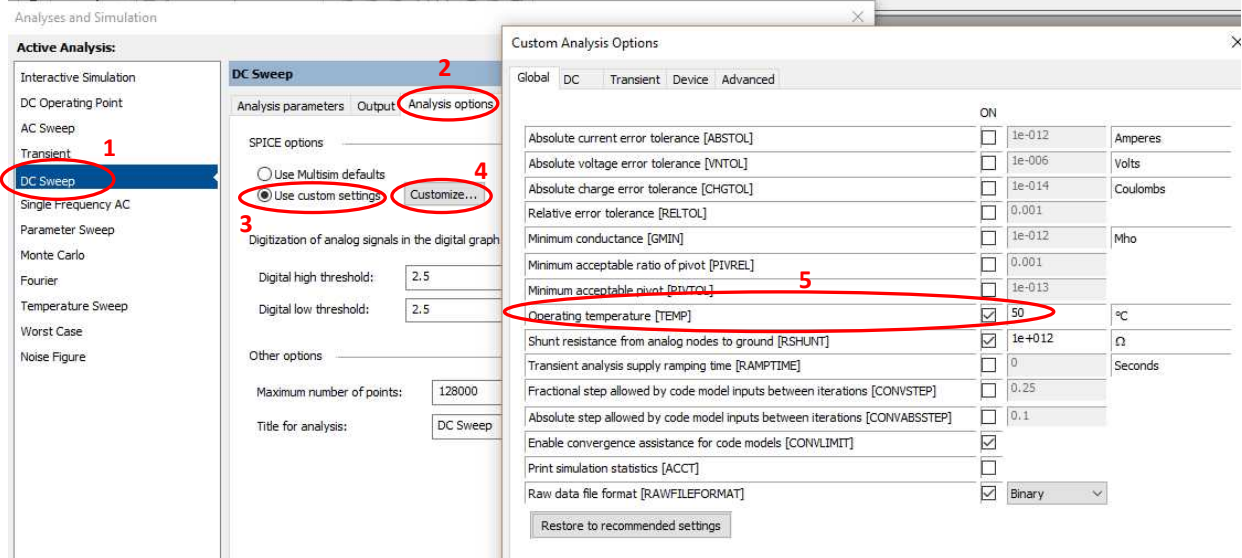


Figure 3-15.

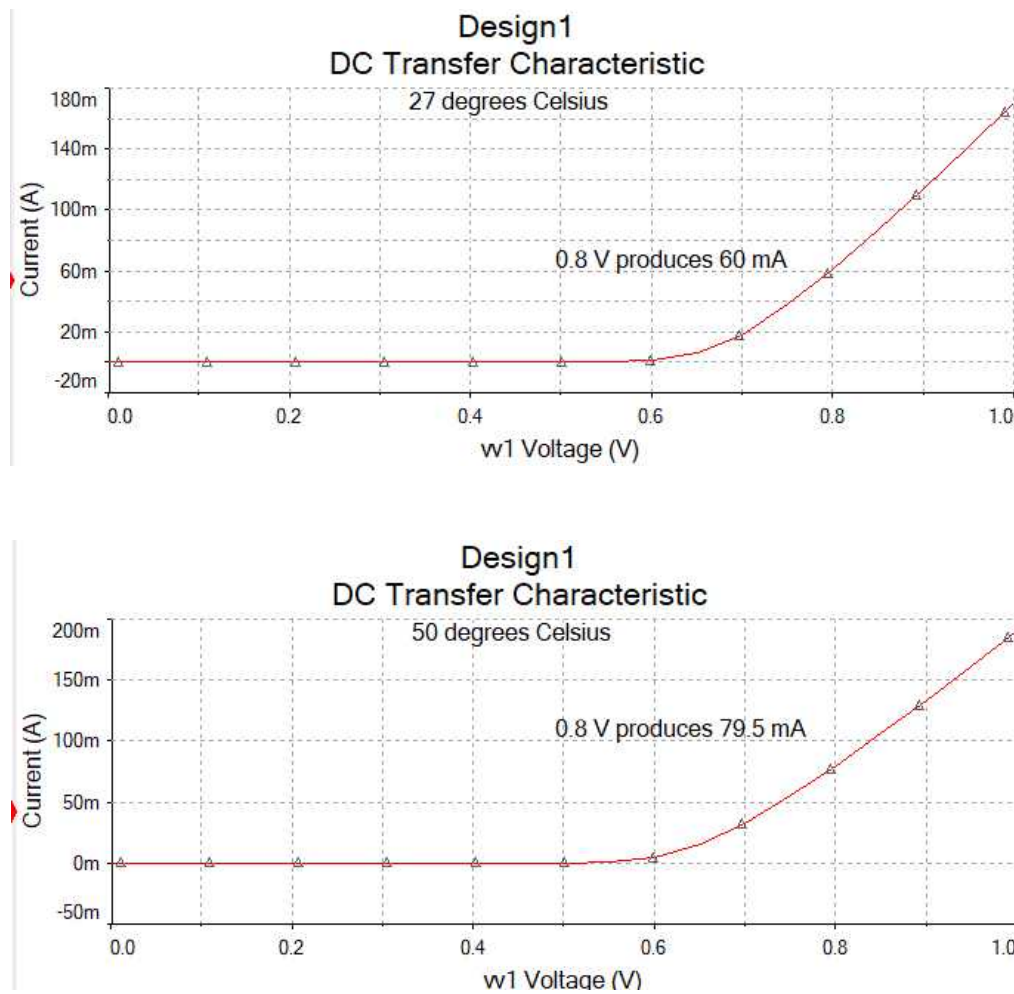


Figure 3-16.

An Increase in the Temperature Increases I_S

As we discovered in Chapter 1, a reverse-biased p - n junction will pass an extremely small current called the reverse saturation current I_S . The reverse saturation current is produced by minority carriers. Since minority carriers are liberated by thermal energy, the reverse saturation current is an extremely strong function of temperature. In fact, it has been shown that I_S ***approximately doubles for each 10°C rise in temperature***. This relationship is defined by Eq. 3-3. Note that functional notation has been used again.

$$I_S(T) = [I_S(25^\circ\text{C})]2^{(T-25)/10} \quad (3-3)$$

where $I_S(T)$ is the reverse saturation current at temperature T in $^\circ\text{C}$,
 $I_S(25^\circ\text{C})$ is the reverse saturation current at 25°C , and
 T is the temperature in $^\circ\text{C}$

Example 3-2. A silicon diode has a reverse saturation current of 5 nA at 25°C . Determine its reverse saturation current at 45°C and at 15°C .

Solution: We apply Eq. 3-3 to determine the reverse saturation current.

$$I_S(T) = [I_S(25^\circ\text{C})]2^{(T-25)/10}$$

Hence, at 45°C we obtain the result below.

$$I_S(45^\circ\text{C}) = [5\text{ nA}]2^{(45-25)/10} = [5\text{ nA}]2^2 = 20\text{ nA}$$

We repeat the analysis at 15°C .

$$I_S(15^\circ\text{C}) = [5\text{ nA}]2^{(15-25)/10} = [5\text{ nA}]2^{-1} = 2.5\text{ nA}$$

A reverse V - I characteristic, which illustrates the effects of temperature on the diode's V - I characteristic is given in Fig. 3-17. In Section 1-10 we saw the reverse current (I_R) of a real diode contains two components: the reverse saturation current I_S and the surface leakage I_{SL} [see Eq. 1-3]. Equation 3-3 does **not** apply directly to the I_R specification given on a data sheet. It only holds true for the I_S portion of I_R .

The Effect of Temperature on the Reverse Saturation Current of a Diode

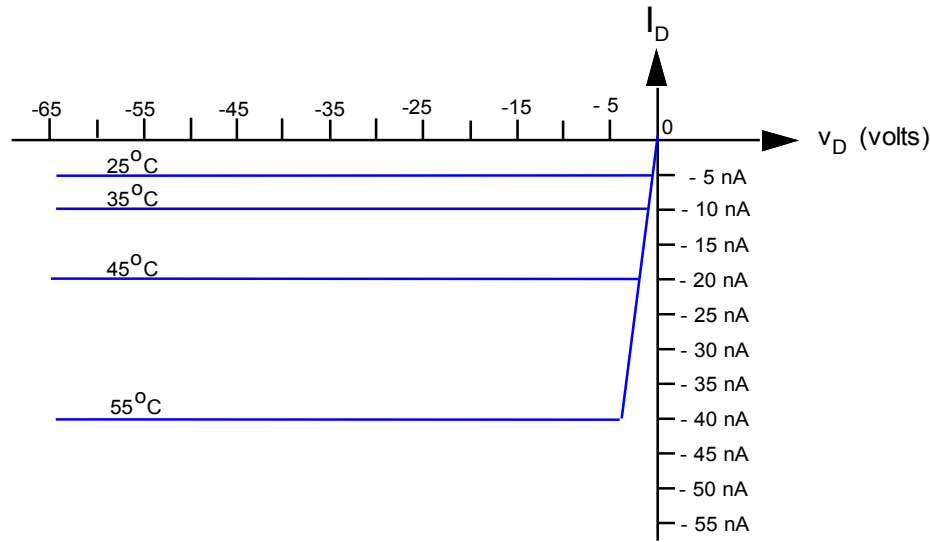


Figure 3-17.

3-4 NTC and PTC Thermistors

We have seen temperature effects can disturb the operation of electronic devices. Later we will see that this can cause problems in the electronic circuits which incorporate these devices. Generally, the effects of temperature are undesirable. However, solid-state devices like **negative temperature coefficient (NTC) thermistors** and **positive temperature coefficient (PTC) resistors** are designed to maximize their sensitivity to temperature. We consider the NTC thermistor first. These devices are often used to sense or monitor temperature changes. NTC thermistors come in a wide variety of packaging options as shown in Fig. 3-18.

The thermistor is a metal-oxide semiconductor device. It is usually made by sintering²¹ various mixtures of metallic oxides such as nickel, manganese, cobalt, or iron. Because the semiconductor molecules are covalently bonded, electrons will be released as the temperature is increased. Package styles are shown in Fig. 3-18. Devices with leads are soldered into holes and are described as “through-hole” devices. Surface-mount devices are mounted to the top or bottom of a printed circuit board. This technology offers improved component density. Typical schematic symbols are given in Fig. 3-18(d). The symbols that look like resistors are American while the symbols that use rectangles are International Electrotechnical Commission (IEC) standard representations.

²¹Sintering is a term from process metallurgy, which means a thin layer of small particles is heated to form larger particles.

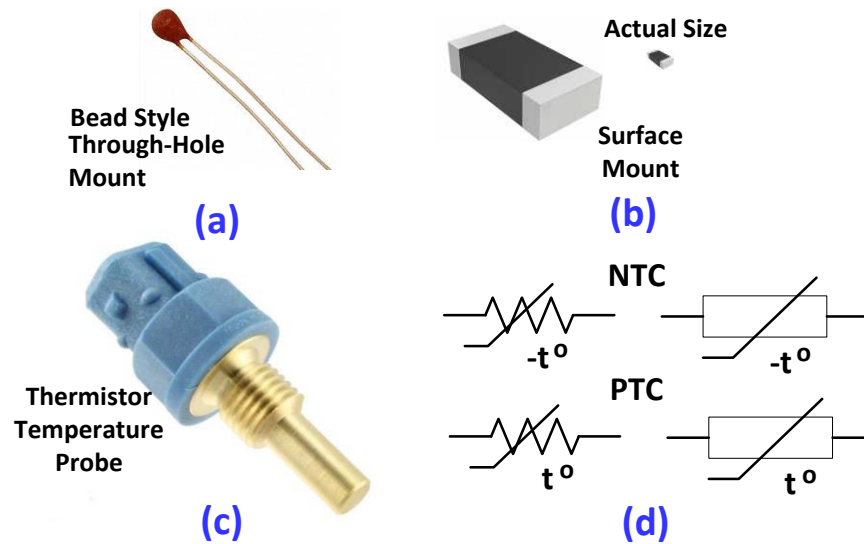


Figure 3-18.

NTC thermistors exhibit a negative temperature coefficient of resistance. This means their terminal resistance decreases as their temperature is raised. As can be seen in Fig. 3-19, the thermistor's response is highly non-linear. (This disadvantage can be overcome by using special linearizing circuitry, which means linearized thermistors are available.)

NTC Resistance-Temperature Curve

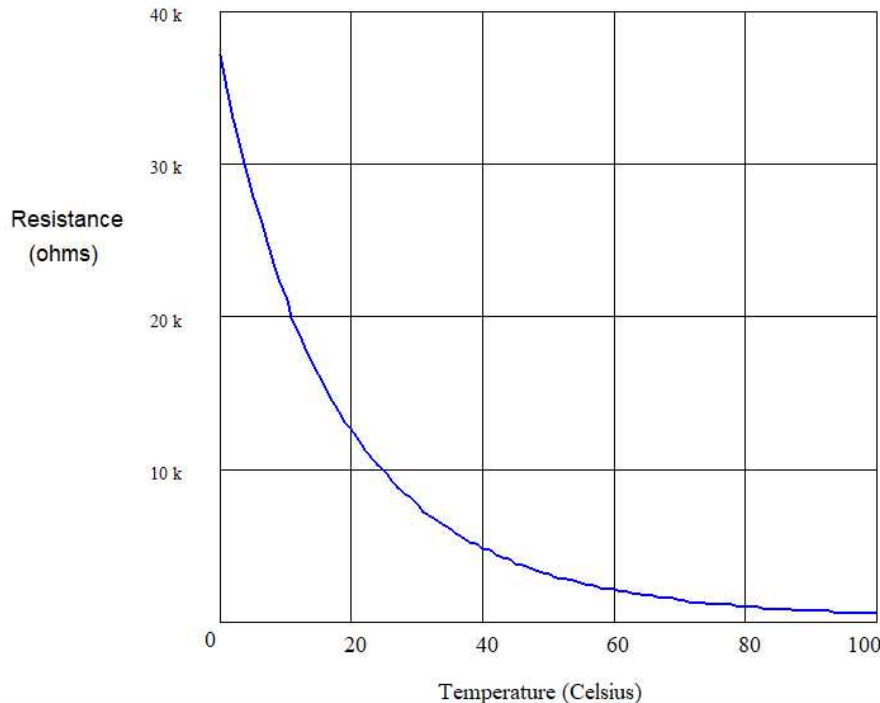


Figure 3-19.

NTC Thermistors are nonpolarized devices

The NTC thermistor is a *bilateral (or nonpolarized)* device. This means current flows equally well in both directions. In contrast, the rectifier and zener diodes are *unilateral devices* since their forward-bias V - I characteristics are different from their reverse-bias V - I characteristics. NTC thermistors are used for temperature measurement, to limit in-rush current on power up, and provide over-temperature shutdown functions. We will study specific applications of thermistors in our later work.

PTC Thermistors

The resistance of positive temperature coefficient (PTC) resistors increases with increasing temperature. This is the *same* temperature coefficient demonstrated by electrical conductors such as copper, aluminum, and platinum. However, the change in the resistance offered by semiconductor devices is several orders of magnitude greater than that demonstrated by electrical conductors. One such device is the PTC thermistor produced by Raychem called a “PolySwitch”. It is marketed as an automatically- resettable fuse. Self-heating (I^2R) produces the required temperature rise in this application.

The PolySwitch is a PTC thermistor that undergoes a large, abrupt change in resistance when an over current (or high temperature) heats it above a specific point. A typical resistance versus temperature curve is given in Fig. 3-20. Note that the vertical axis is a *logarithmic scale*. This allows a large range of data (in this case the resistance) to be compressed. In the 10°C span of temperature from 120°C to 130°C the resistance increases from slightly over $20\ \Omega$ to well over $2\ \text{M}\Omega$!

Resistance-Temperature Curve of a Polyswitch PTC Thermistor

In a 10-degree Celsius span, the resistance increases from about 20 ohms to well over 2 million ohms!

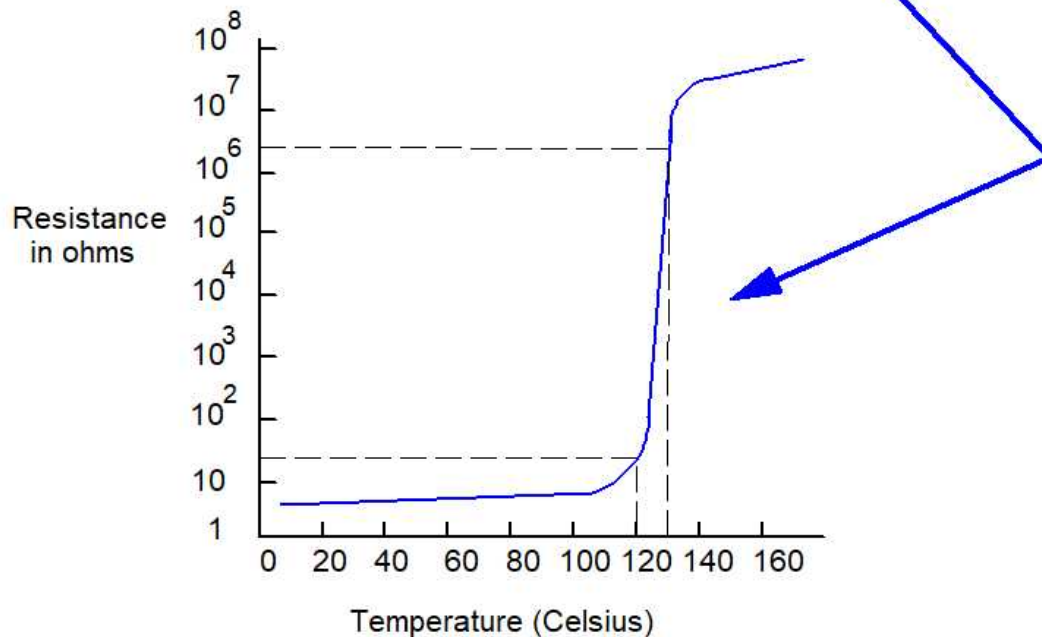


Figure 3-20.

The solid-state material used to make a PolySwitch device is a conductive-filled polymer²². As a solid-state fuse, the PolySwitch offers the advantage of being *automatically reset*. Once the fault is removed, the PolySwitch cools off and reverts to its normal (low resistance) state. Consider the reverse-polarity protection circuit shown in Fig. 3-21. (The PTC specifications are given in Table 3-1.)

Reverse-Polarity Protection Circuit

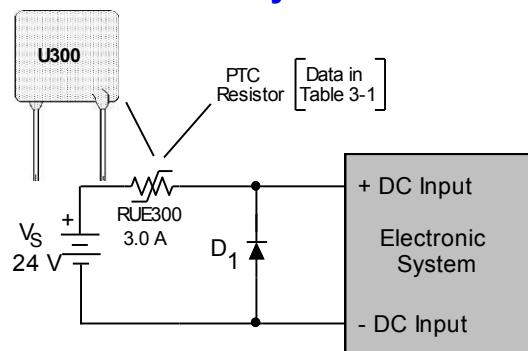


Figure 3-21.

²²Polymers are composed of large molecules that are formed from small, repeating molecular building blocks. Examples of polymers include nylon, Teflon, and Plexiglas.

Electronic systems typically require a source of DC power to operate. In some cases, an electronic system may use its own internal line-operated DC power supply (Chapter 4) or an external DC power supply such as a battery. Battery-operated equipment is prone to having its power supply reversed. (No matter what precautions are taken - polarized plugs and/or diagrams showing the proper way to install the batteries - someone will invariably reverse the batteries.) ***A reverse DC bias can destroy the electronic devices and any integrated circuits used in the system.***²³

In normal operation [Fig. 3-22(a)], diode D_I is reverse biased and acts like an open switch. However, the PTC resistor has a *holding current rating* of 3.00 A. (The data for the selected part is listed in Table 3-1.) This means it will pass a maximum of 3.00 A without increasing its resistance. The PTC resistor offers overcurrent protection. If a fault develops within the electronic system, the PTC resistor will limit the fault current. The PTC resistor has a *trip current rating* of 6.00 A.

When un-tripped (cool), the normal resistance of the device is on the order of milliohms. Its resistance will increase several orders of magnitude when switched. The PTC resistor will undergo a large abrupt resistance increase when an overcurrent or high temperature heats it above a specific point.

Table 3-1.

The RUE300 PTC Resistor Characteristics

I_H = Hold Current = 3.00 A	R_{UT} = Untripped Resistance = 0.02 to 0.05 Ω
I_T = Trip Current = 6.00 A	R_T = Tripped Resistance = V^2 / P_d
P_d = 2.0 W	(where V is the applied voltage)
Maximum Voltage = 30 V	Operating Temperature Range = 0 to 60 $^{\circ}\text{C}$
Maximum Interrupt I = 40 A	

When the PTC device is tripped, its resistance will reach a point of equilibrium such that the device power dissipation will be constant at a given temperature. In the case of the RUE300 PTC resistor, the “magic” power dissipation is 2.0 W. The current will be limited to the value given by Eq. 3-4.

$$I_{LIMIT} = \frac{P_d}{V} \quad (3-4)$$

where I_{LIMIT} is the equilibrium current through the PTC resistor,
 P_d is the equilibrium power dissipation, and
 V is the applied voltage (during the fault) across the PTC resistor.

²³ As a graduate instructor I was to teach a portion of a course that dealt with a linear integrated circuit called an operational amplifier. I experimented with one until I was confident in its capability. Manufacturers warned repeatedly the power supply should never be reversed. My last experiment was to do precisely that. ***The integrated circuit caught on fire*** and I had a good anecdote for my students!

Example 3-3. Given the reverse-polarity protection circuit indicated in Fig. 3-21. Find the maximum voltage drop across the PTC resistor if the electronic system draws 3.00 A [Fig. 3-22(a)]. What is the current through the diode if the DC voltage source V_S is accidentally reversed as indicated in Fig. 3-22(b)? Find the tripped resistance of the PTC resistor.

Solution: According to the data presented in Table 3-1, the PTC resistor's maximum untripped resistance is 50 m Ω . Therefore, the voltage drop across the un-tripped device is

$$V_{UT} = I_H R_{UT} = (3.00 \text{ A})(0.05 \Omega) = 0.15 \text{ V}$$

In Fig. 3-22(b), the current through the diode will be limited to I_{LIMIT} as given by Eq. 3-4. Since we have 24 V applied and the forward-biased diode drops 0.7 V, the voltage drop across the PTC thermistor is 23.3 V. This is an application of Kirchhoff's Voltage Law.

$$V_{PTC} = V_S - V_D = 24 \text{ V} - 0.7 \text{ V} = 23.3 \text{ V}$$

$$I_{LIMIT} = \frac{P_d}{V} = \frac{2.0 \text{ W}}{23.3 \text{ V}} = 85.8 \text{ mA}$$

The tripped resistance can be determined via Ohm's law or by using the power formula given in Table 3-1.

$$R_T = \frac{V^2}{P_d} = \frac{(23.3 \text{ V})^2}{2 \text{ W}} = 271 \Omega$$

Reverse-Polarity Protection Circuit Operation

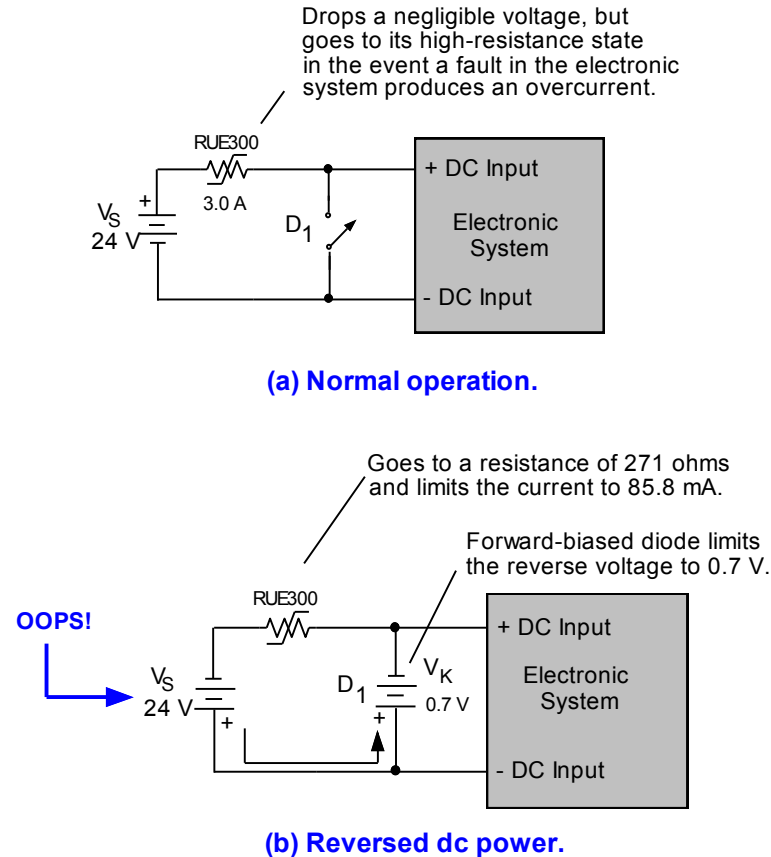


Figure 3-22.

3-5 Varistors

Metal oxide varistors [Fig. 3-23] are voltage-dependent, non-linear resistors. In this regard, their terminal resistance depends on the voltage impressed across them. Typical package styles are shown in Fig. 3-23(b). Varistors have an electrical behavior, which is like placing two back-to-back zener diodes in series [see Fig. 3-23(c)]. A typical V - I characteristic curve is shown in Fig. 3-23(d). The schematic symbols remind us of the V - I characteristic curve. Varistors are designed to provide protection from voltage transients. A varistor acts like an open circuit when subjected to voltages below its breakdown voltage rating.

The Varistor: A Transient-Suppression Device

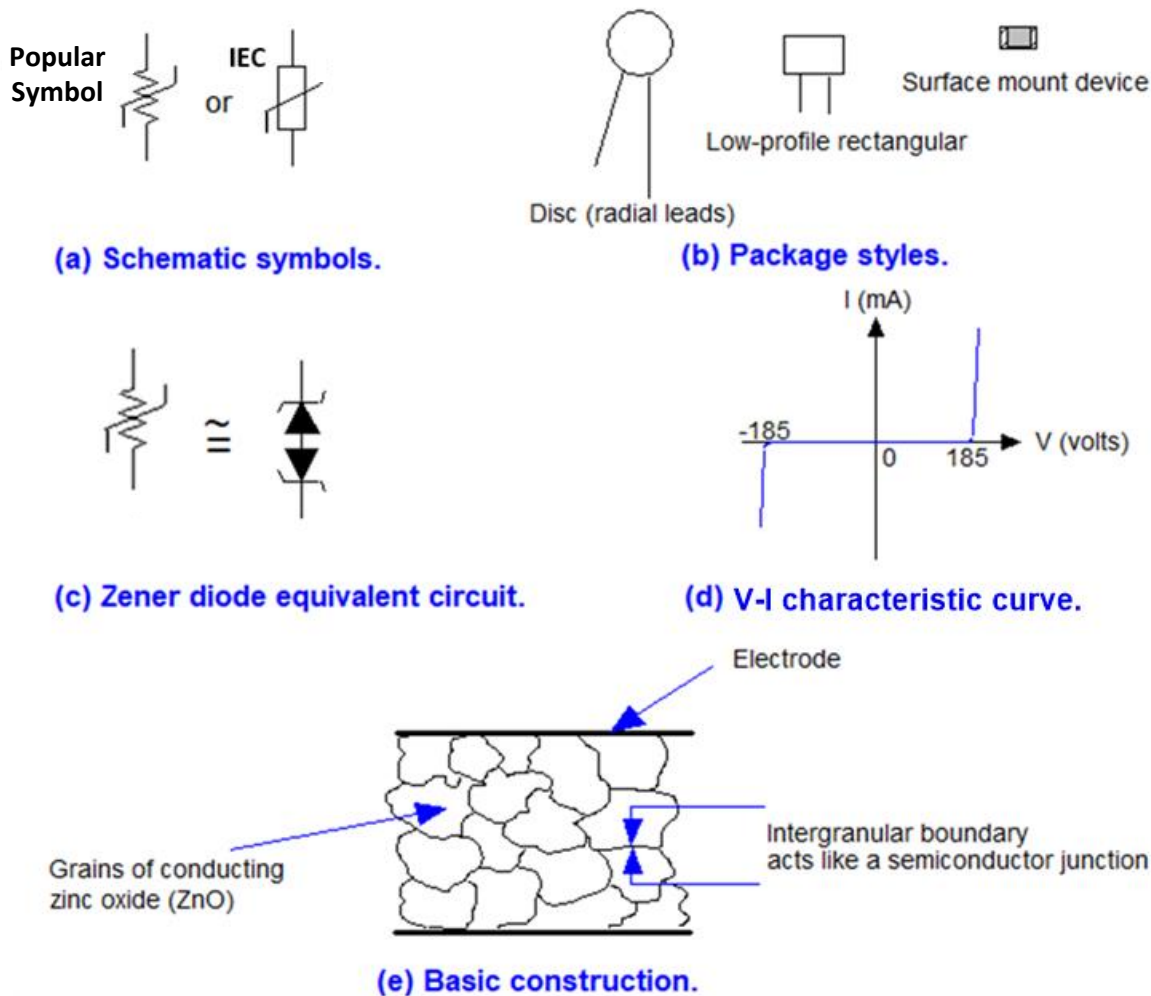


Figure 3-23.

When a varistor experiences a voltage that exceeds its breakdown voltage rating, it will begin to conduct. It will act like a voltage source that is receiving current. It is this characteristic that permits a varistor to clamp a transient voltage to a safe level.

Varistors are constructed by sintering²⁴ zinc oxide-based powders into ceramic parts. Each zinc oxide (ZnO) grain acts as if it has a semiconductor junction at the grain boundary. A cross-section of the material is depicted in Fig. 3-23(e). The varistor can be considered a multi-junction device composed of many series and parallel connections of grain boundaries.

The most common application of a varistor is to place it across the AC power line connections to line-operated equipment [see Fig. 3-24]. The varistor acts like an open circuit until a power-line transient (produced by other electrical equipment turning on or off, or by a nearby lightning strike) exceeds its breakdown voltage.

²⁴If you skipped reading the footnote in Section 3-4, you probably still don't know the definition of sintering. Feel guilty? It's waiting for you *there*.

Since a varistor conducts when its breakdown voltage is exceeded, it will dissipate power (energy). While a varistor is designed to absorb energy uniformly, there is a physical limit. Consequently, a line fuse (or a PTC resistor) should be used to limit the current through it. *If a varistor's power dissipation rating is exceeded, it will become a short circuit. This is the varistor's common failure mode.*

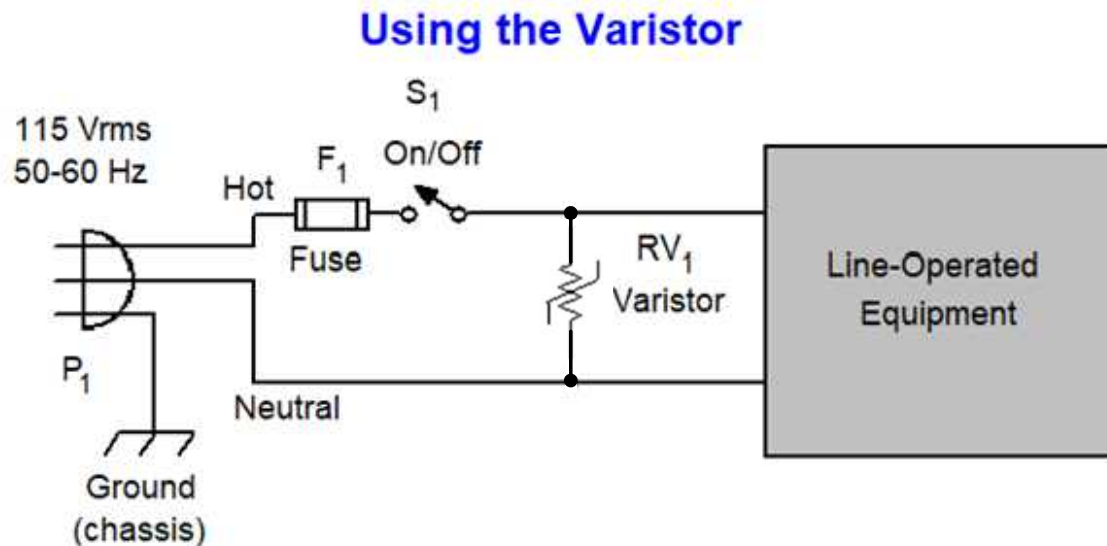


Figure 3-24.

In Fig. 3-24 we see how the varistor can be used in a circuit. The power line plug (P_1) provides the **hot, neutral, and ground** power line connections. The power line voltage is 115 Vrms nominally with a frequency of either 60 Hz (North America) or 50 Hz (Europe). When switch S_1 is closed power is applied. The varistor (RV_1) is in parallel with the power line input to the line-operated equipment. If an over-voltage transient appears across the power line, the varistor will conduct to limit the voltage appearing across the power-line input. If the varistor conducts too long, the fuse (F_1) will open to disconnect the line-operated equipment. Much more will be explained about the power line in Chapter 4. The fuse could be replaced by a PTC thermistor. Most of the PTC thermistor failure modes result in the device failing as an open circuit. However, if a large voltage is developed across, there is a possibility it can become a short circuit. If this is a concern, a fuse (with a higher over-current rating) can be placed in series with the PTC thermistor. The only time the fuse will open is if the PTC thermistor fails catastrophically as a short circuit.

3-6 Light-Emitting and Laser Diodes

When a p - n junction is forward-biased, electrons move from the n -side, through the depletion region, and into the p -type material. To make this move the electrons must overcome the depletion region barrier potential, lose energy, and fall into the holes on the p -side of the junction. When a free electron goes from the conduction energy band to the valence energy band where the holes reside, it must give up some of its energy.

In the case of silicon, the electrons fall through a series of intermediate levels. As many as 20 transitions can be involved for each electron. At each transition, the electron releases a *small packet of heat energy called a **phonon***. Semiconductor molecules formed from combinations of trivalent and pentavalent elements (such as gallium arsenide) behave differently. Their electrons tend to go directly from the conduction energy band to the valence energy band. In this case the electrons give up *packets of light energy called **photons*** [see Fig. 3-25].

Photons of light can be thought of as electromagnetic energy of extremely high frequency (e.g., terahertz or 10^{12} Hz). Because the frequency is so high, the corresponding wavelength of the electromagnetic waves is often used. The relationship between wavelength and frequency is given by Eq. 3-5.

$$\lambda = \frac{c}{f} = \frac{3 \times 10^8 \text{ m/s}}{f} = \frac{3 \times 10^{17} \text{ nm/s}}{f} \quad (3-5)$$

where λ = (Greek letter lambda) the wavelength in nanometers,
 c = the speed of light = 3×10^{17} nm/s, and
 f = the frequency in hertz

Electron Energy Release

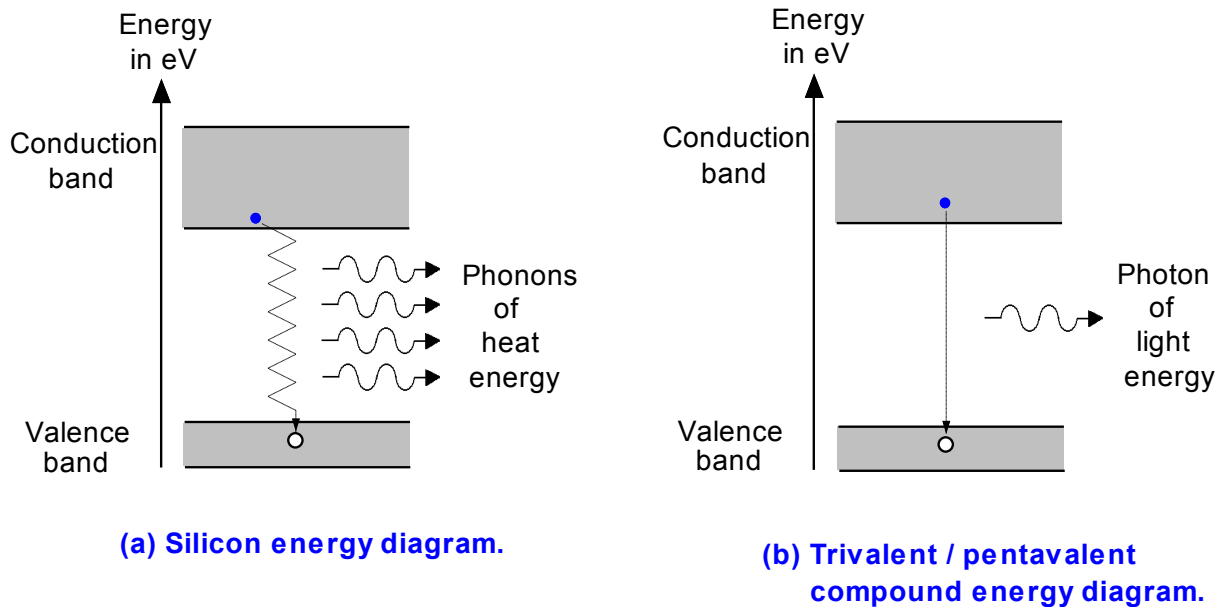


Figure 3-25.

Recall that the energy difference between the conduction and valence energy bands is called the *bandgap*. **The bandgap energy (W_g) determines the wavelength of the emitted light.** The relationship between the two is provided by Eq. 3-6.

$$\lambda = \frac{1240.5}{W_g}$$

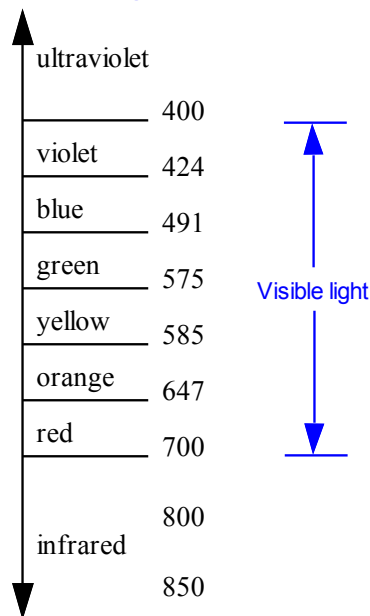
(3-6)

where λ = (Greek letter lambda) the wavelength in nanometers, and
 W_g = the bandgap energy in electron volts (eVs)

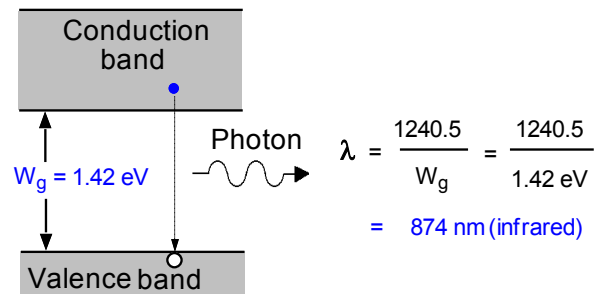
The wavelength of the emitted light determines the color. Consider Fig. 3-26. The electromagnetic band of visible light progresses from the infrared region to the ultraviolet region. (The order of the colors can be remembered by applying the mnemonic ROY G. BIV. The “I” refers to indigo which falls between blue and violet.) Gallium arsenide [Fig. 3-26(b)] with its bandgap of 1.42 eV produces photons of infrared light. Gallium phosphide [Fig. 3-26(c)] has a much larger bandgap of 2.26 eV and produces green light.

The Color of the Light Emission Depends on the Bandgap

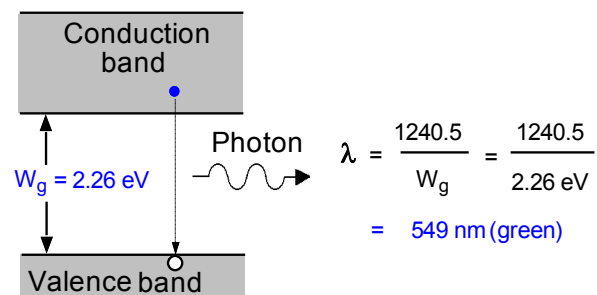
Light wavelength λ in nanometers



(a) The electromagnetic spectrum.



(b) Gallium arsenide (GaAs) emits infrared light.



(c) Gallium phosphide (GaP) emits green light.

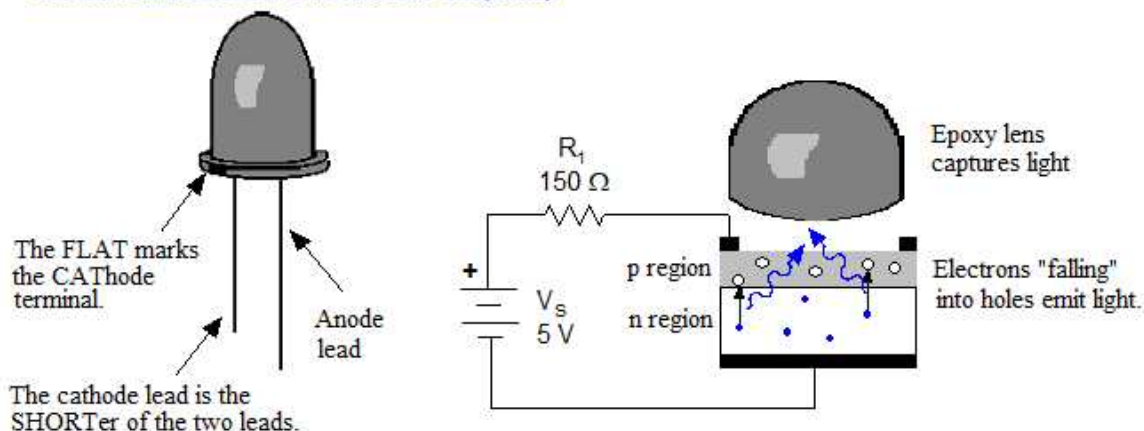
Figure 3-26.

A typical light-emitting diode (LED) package is illustrated in Fig. 3-27(a). The grisly mnemonic, “a roadkill kitten is a short flat cat” is intended to help us remember the flat on the LED package marks the cathode terminal and the cathode lead is the shorter of the two LED leads. Figure 3-27(b) shows that as an electron falls into the valence energy band, it will release a photon of light energy. Therefore, light is emitted from the *p*-side of the *p*-*n* junction. The epoxy lens serves to capture and diffuse the light. When holes move into the *n* side, they tend to capture electrons there. The light emitted within the *n*-region tends to be absorbed by the *n*-type material. Consequently, the light is lost, and the efficiency of the LED is reduced.

In Fig. 3-27(c) we see the structure of an LED. The diode is built upon a **substrate**. The substrate serves as a chassis (or holder) for the device. **Silicon dioxide (SiO_2)** is used as an electrical insulator. The SiO_2 layer is formed via the process of **passivation**. Pure heated oxygen is blown over the semiconductor to form the glasslike layer of SiO_2 . Also, note that a heavily doped *n*-type layer (n^+) is used to form the *p*-*n* junction. This tends to make the forward current favor electrons from the *n* side flowing to the *p* side rather than holes moving from the *p* side into the *n* side. Figure 3-27(d) depicts the LED’s schematic symbol.

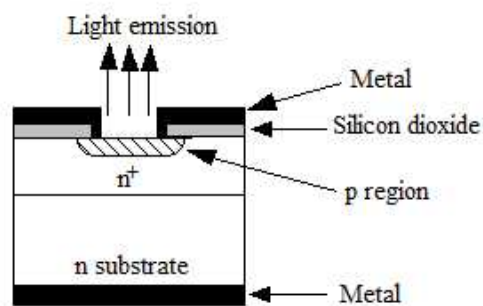
The LED

"A Road-Kill Kitten is a Short, Flat Cat(hode)"

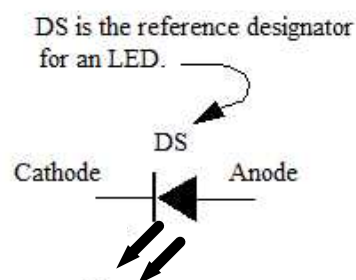


(a) A typical LED package.

(b) Basic LED operation.



(c) A typical LED structure.



(d) The schematic symbol.

Figure 3-27.

Typical V - I characteristic curves are presented in Fig. 3-28. Note that a silicon rectifier diode has been included for reference. ***Silicon carbide LEDs emit blue light.*** The blue LED is the latest addition to the LED family. LEDs, which emit visible light, are used widely as indicators. LEDs that emit infrared light are used in remote controls for televisions, computer projection systems, and sound systems. Infrared LEDs are also used in fiber-optic communication systems and in wireless mouse designs for computers.

The blue LED has helped revolutionize the optoelectronic industry. Red, green, and blue LEDs can be combined to generate practically any color including white light. ***Gallium Indium Nitride (GaInN) also produces a blue light.*** When a phosphorous filter is placed in its lens it produces a cool white light. It has become a popular choice for general lighting applications. LEDs are rugged, efficient, and offer lifetimes that are often in terms of many years. This makes them superior to incandescent and fluorescent lights.

LED Forward V-I Curves

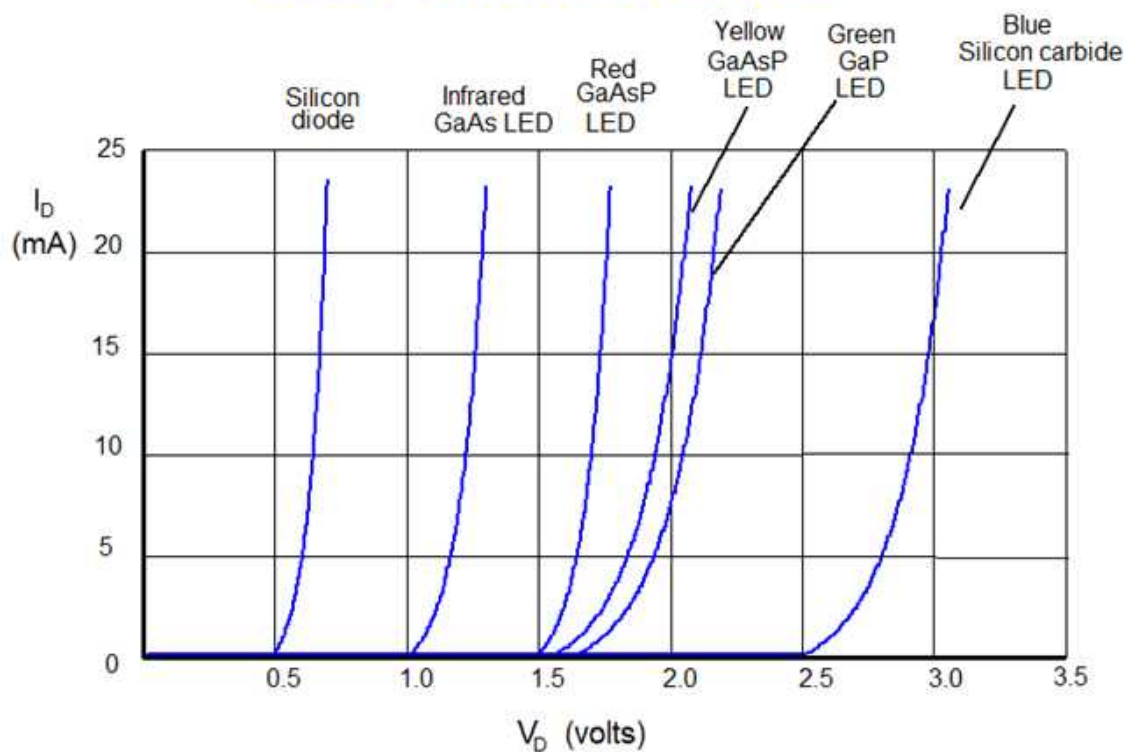


Figure 3-28.

Laser Diodes

Laser is the acronym for “light amplification by stimulated emission of radiation”. It refers to a phenomenon predicted by Einstein many years before a way was found to achieve it in practice. (An American physicist, G. Gould, invented the first practical laser in 1958.)

When an atom receives additional energy, the energy is absorbed by its orbital electrons. When an atom de-excites, its orbital electrons give up energy. An electron that falls from a higher orbit to a lower one can give up energy in the form of electromagnetic radiation (light).

If several atoms in a material are excited to the *same* level and one of the atoms emits its radiation before the others, then the passage of this radiation past the other atoms can also *stimulate* them to de-excite. It is significant that when the other atoms give up energy, it will be in phase (called **coherent**) and in the *same direction* as the stimulating energy [see Fig. 3-29]

Since the electrons fall through the same bandgap, the radiation emissions will all have the same wavelength. Light possessing one wavelength (one frequency or color) is called **monochromatic**. In a normal LED the radiation emissions are monochromatic, in random directions, and incoherent (*not* in phase). This is because the emissions are all spontaneous.

Figure 3-29 illustrates some spontaneous emissions but is also shows a **stimulated emission**. In this case atom 1 emits radiation spontaneously. When this radiation moves past other excited atoms (e.g., 2 and 3) it will stimulate them to de-excite.

To construct a laser the host material must promote atoms with long-lived excited states. When one of the atoms de-excites spontaneously, it will stimulate other atoms in its radiation path to also de-excite. If the ends of the laser are mirrored (Fig. 3-30) and a perpendicular spontaneous emission occurs, the light will be reflected back and forth between the two mirrors.²⁵

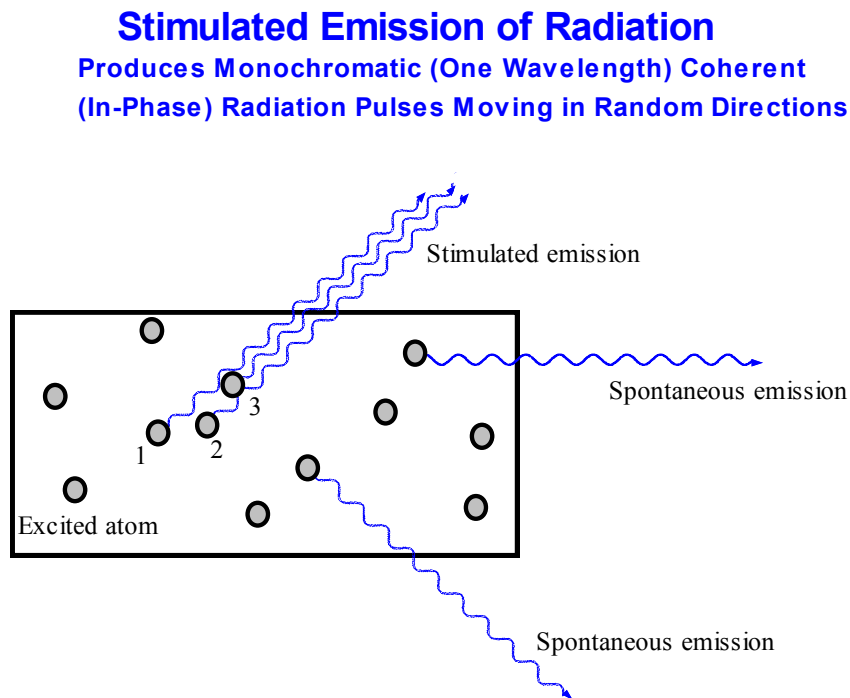


Figure 3-29.

²⁵It should not be surprising to learn the back-and-forth reflections occur at the *speed of light*.

Most of the atoms are quickly de-excited in this fashion. If one of the mirrors is only partially reflective (e.g., 60%) a pulse of light will build to the point of intensity such that it can break through. The result [Fig. 3-30(c)] is a beam of light that is monochromatic, coherent, and has very little divergence (which means a narrow beam is formed).

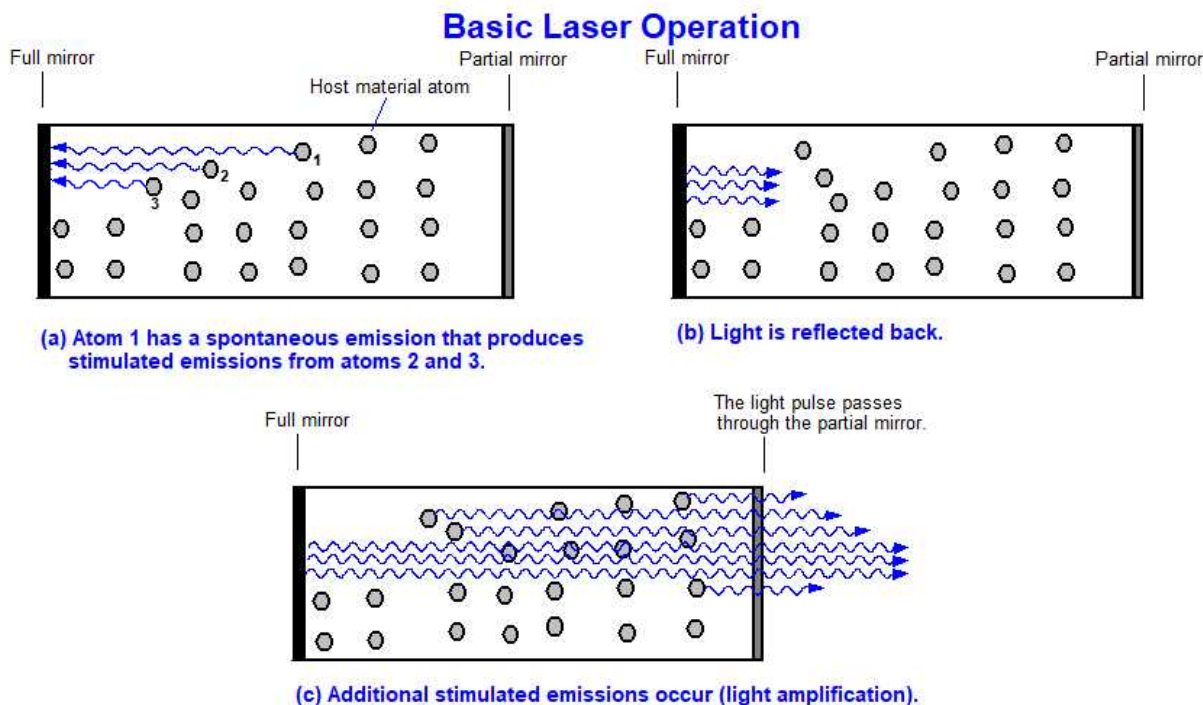


Figure 3-30.

The Operation of a Semiconductor Laser

Laser diodes are used in pointers, DVD and Blu-ray players, and are used in laser printers. Laser printers are discussed in the next subsection. A laser diode package and typical wiring diagrams are shown in Fig. 3-31. An internal photodiode is optically coupled to the laser diode (Section 3-7) to monitor the light intensity and control the *current* through the diode. Since it is this current that produces the clouds of electrons and holes, it is a convenient means of keeping the light intensity of the source constant. The photodiode works in conjunction with external electronic circuit. Laser light is dangerous. Eye protection must be worn.²⁶

²⁶ "DANGER: Laser radiation from a laser diode can cause eye injury. Do not look into the laser diode aperture with *remaining* good eye." - a warning suggested by Karl Hamilton of Hamilton Sundstrand.

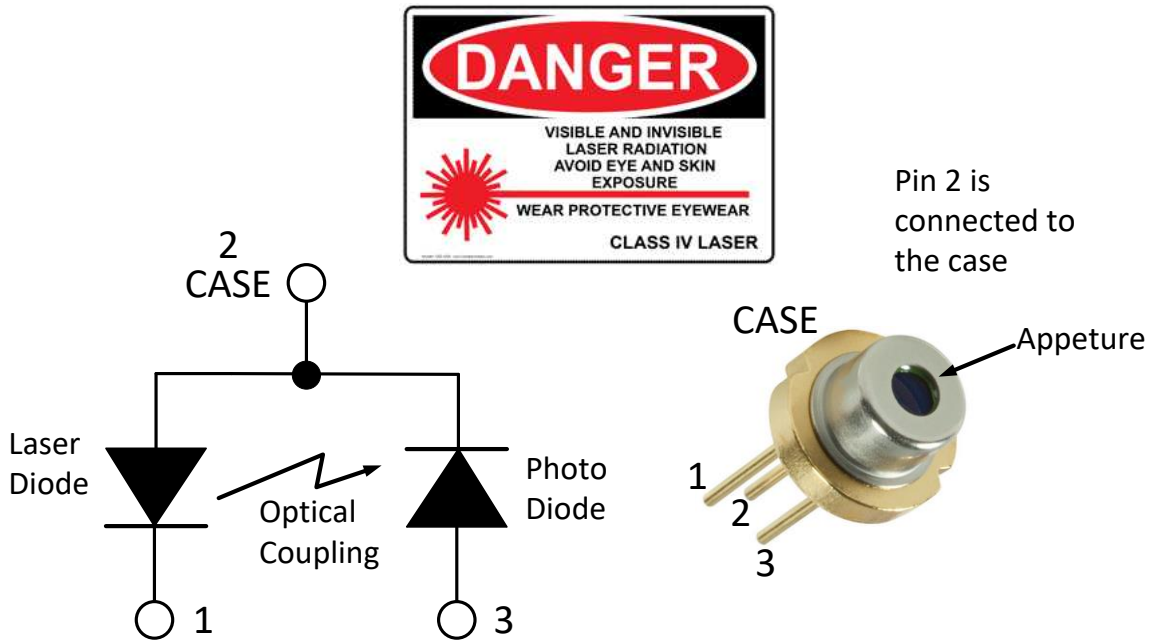


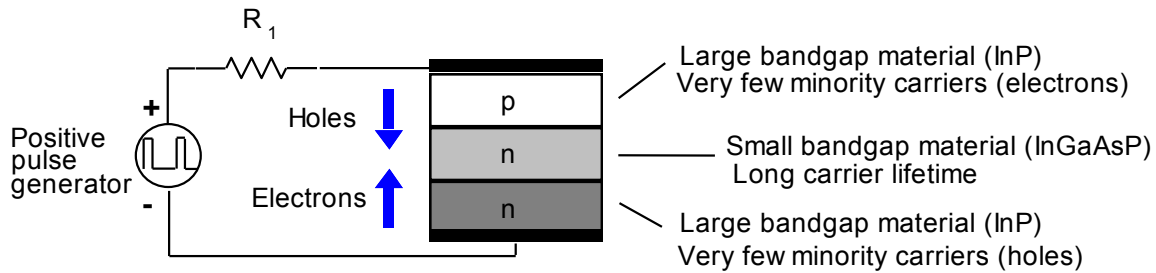
Figure 3-31.

The basic structure of a semiconductor laser is indicated in Fig. 3-32. The light-emitting, active region of the laser is constructed from a **heterojunction**. A heterojunction is created when a p - n junction is built using *different* semiconductors. A wide bandgap semiconductor such as indium phosphide (InP) is used to make p - and n -type regions. A wide bandgap material is not as prone to thermal ionization. Consequently, these materials have very few minority carriers. As a result, holes and electrons are injected into the narrow bandgap n -type material. (The narrow bandgap material used here is indium gallium arsenide phosphide, which is denoted InGaAsP). The holes and electrons are injected as depicted in Fig. 3-32(a).

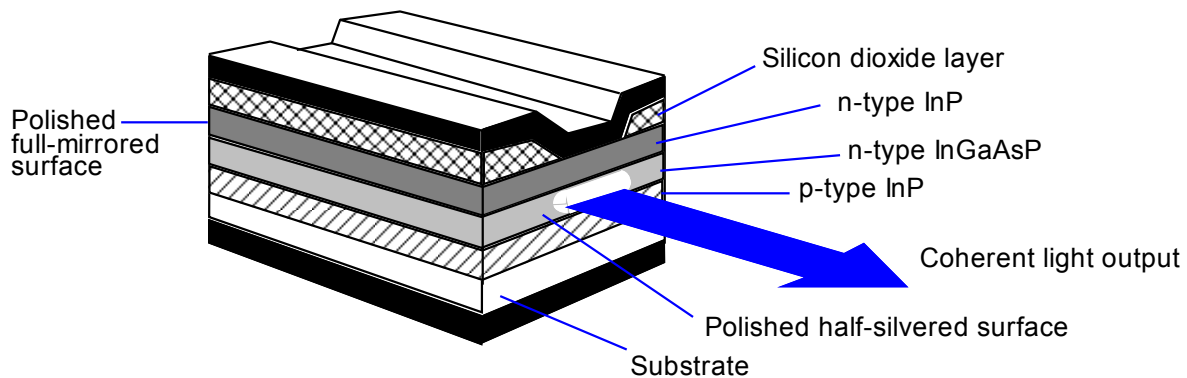
The InGaAsP is a long lifetime material. This mean the holes and electrons do not immediately recombine. Consequently, spontaneous emission is less likely to occur, which increases the probability of stimulated emissions when an incident beam impinges.

The laser diode is designed emit light from its edge. Both ends of the structure are flat and silvered. The less heavily silvered end serves as a light source. The more heavily silvered end allows a small fraction of the light to emerge which is used for control purposes.

The Basic Structure of the Semiconductor Laser



(a) The central (active) region of the laser diode.



(b) The structure of the laser diode.

Figure 3-32.

At low current levels, a laser acts like an ordinary LED. To obtain the necessary current without overheating the diode, short, high-amplitude pulses are often used. A pulse generator has been indicated in Fig. 3-32 (a).

An Application of the Laser Diode is the Laser Printer

Laser printers are comprised of a complex assembly of electronic, mechanical, and optical components. The basic operation of a laser printer is detailed in Fig. 3-33(a). A rotating mirror [Fig. 3-33(b)] reflects a pulsed laser beam, sweeping it across a negatively charged photosensitive drum. **The laser beam is used to selectively discharge individual pixels (picture elements) on the rotating drum. Charged pixels attract toner to “write black” while uncharged pixels, “write white”.** Sheets of paper roll against the drum and pick up the toner (powdered ink). The paper is then directed through a fusing element, which heats the page to melt the plastic toner and form the final image.

Electronic circuitry is required to control the mechanical systems, drive the laser diode, and to interface the parallel printer (input) port or USB connection to an external computer. Random access memory (RAM) is used to temporarily store data to be printed. The data for an entire page is stored before printing begins. A small on-board microcomputer is used to oversee the operation of the laser printer. The software (programming) effort required to control the operation of the microcomputer is substantial.

Operation of a Laser Printer

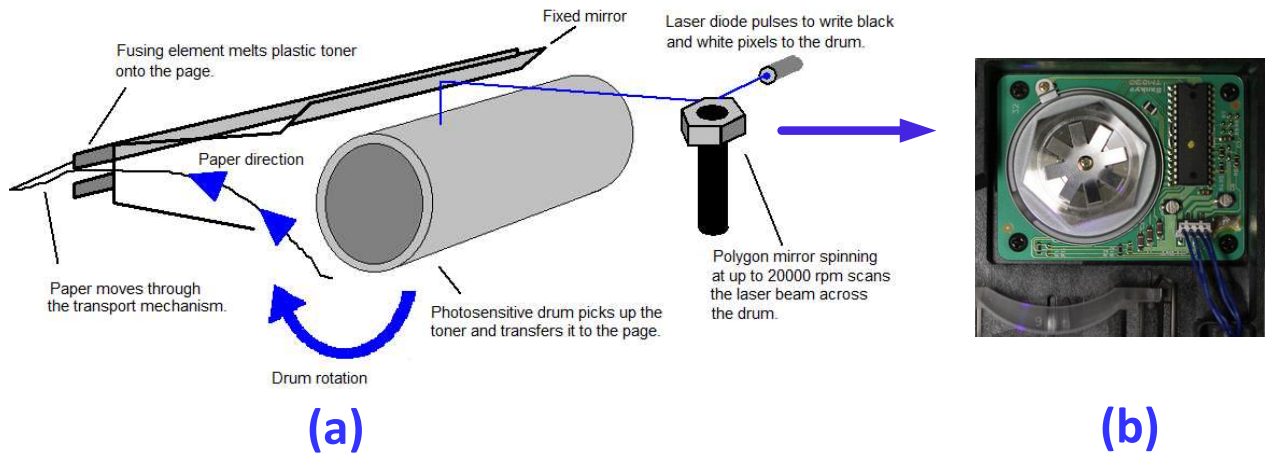


Figure 3-33.

To analyze circuits that incorporate LEDs or laser diodes, we typically apply the knee-voltage diode model. In Section 1-8 we explained the creation of the depletion region and its attendant barrier potential. We also mentioned the barrier potentials for the various gallium compounds tend to range from approximately 1.2 to 1.9 V. Inspection of Fig. 3-28 shows that at a forward current of 5 mA the gallium compound LEDs have forward voltage drops ranging from 1.2 to 1.9 V. (Silicon carbide has a voltage drop that approaches 2.8 V.) ***Without specific data on a given LED, we shall assume a knee voltage of 1.6 V.***

Example 3-4. A red (GaAsP) LED is used in the circuit shown in Fig. 3-34(a). Find the forward current (I_D) through it.

Solution: Assuming a knee voltage of 1.6 V, we use the knee-voltage diode model [Fig. 3-34(b)] to find I_D .

$$I_D = \frac{V_S - V_K}{R_1} = \frac{5\text{ V} - 1.6\text{ V}}{180\ \Omega} = 18.9\text{ mA}$$

Example 3-5. The red (GaAsP) LED given in Example 3-4 has been replaced with a blue (silicon carbide) unit. The blue LED has a knee voltage of approximately 2.8 V. Find the forward current (I_D) through it. Nothing else in Fig. 3-34 has been changed.

Solution: Assuming a knee voltage of 2.8 V, we use the knee-voltage diode model to find I_D .

$$I_D = \frac{V_S - V_K}{R_1} = \frac{5\text{ V} - 2.8\text{ V}}{180\ \Omega} = 12.2\text{ mA}$$

The Circuits for Examples 3-4 and 3-5

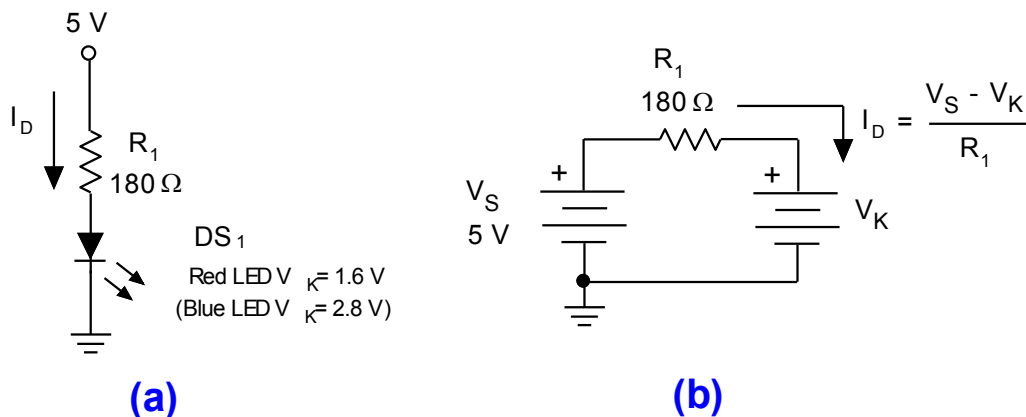
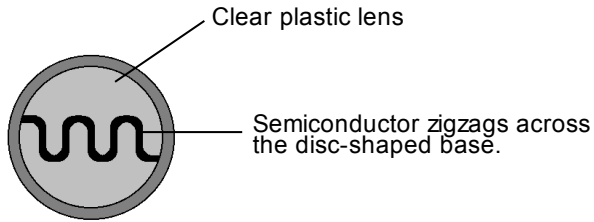


Figure 3-34.

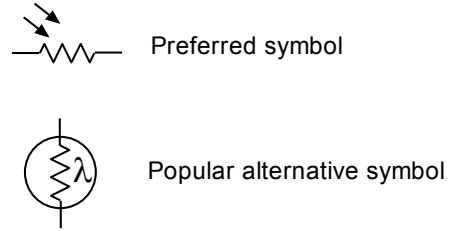
3-7 Photoconductive Cells, Photodiodes, and Solar Cells

A semiconductor's electrons are bound in covalent bonds. Light striking the surface of a semiconductor, with enough energy, will liberate electrons. The resistance of the semiconductor will be decreased since additional free electrons are available. In this instance the resistance will decrease as the light intensity is increased. A **photoconductive cell** is a two-terminal semiconductor device whose terminal resistance varies inversely with the intensity of the incident light. It is an example of a *light detector*. Photoconductive cells are also called **photoresistive cells** and **photoresistors**. Its basic structure, schematic symbol, and significant characteristics are shown in Fig. 3-35.

Photoconductive Cells



(a) Top view



(b) Schematic symbols

Semiconductor	Spectral Response	Response Time	Temperature Sensitivity
Cadmium Sulfide (CdS)	Visible light	100 ms	Relatively stable
Cadmium Selenide (CdSe)	Infrared	10 ms	Very susceptible

(c) Semiconductor summary

Figure 3-35.

The photoconductive cell does not incorporate a p - n junction. Instead, it relies on the effects of light energy on the resistance of a bulk semiconductor. To maximize the surface area of the semiconductor, a zigzag pattern is formed on the surface of the photoconductive cell [Fig. 3-35(a)]. Two of the most popular semiconductors used in the manufacture of photoconductive cells are cadmium sulfide (CdS) and cadmium selenide (CdSe). The differences between the two semiconductors are summarized in Fig. 3-35(c). Information from a typical CdS photocell data sheet has been included in Fig. 3-36.

CdS Photoconductive Photocell

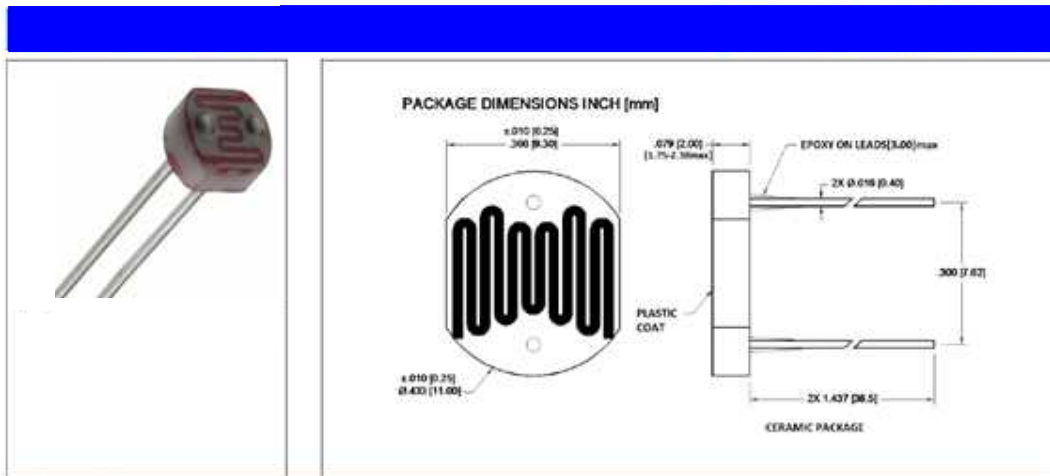


Figure 3-36. Data Sheet Information

A CdS photoconductive cell such as the unit shown in Fig. 3-36 have a visible light response from about 400 to 700 nm (see Fig. 3-26). These light-dependent resistors have a wide range of resistance options. Common applications include night light controls, camera exposure and shutter controls.

A Semiconductor's Bandgap Determines the Color It Likes

The energy bandgap (W_g) between the valence and the conduction energy bands determines the required wavelength of light required to produce a free electron. The W_g for cadmium sulfide is 2.42 eV while the W_g for cadmium selenide is only 1.74 eV. Applying Eq. 3-6 allows us to find the required wavelengths. Hence, we find for *cadmium sulfide*

$$\lambda = \frac{1240.5}{W_g} = \frac{1240.5}{2.42 \text{ eV}} = 512.6 \text{ nm} \quad \longrightarrow \quad \text{Blue/Green (Center of Visible Light)}$$

which means a cadmium sulfide photoconductive cell has a spectral response that is close to that of the human eye. Repeating the analysis for *cadmium selenide*

$$\lambda = \frac{1240.5}{W_g} = \frac{1240.5}{1.74 \text{ eV}} = 712.9 \text{ nm} \quad \longrightarrow \quad \text{Infrared}$$

which means the spectral response peaks for (invisible) infrared light. (The color spectrum is provided in Fig. 3-27.)

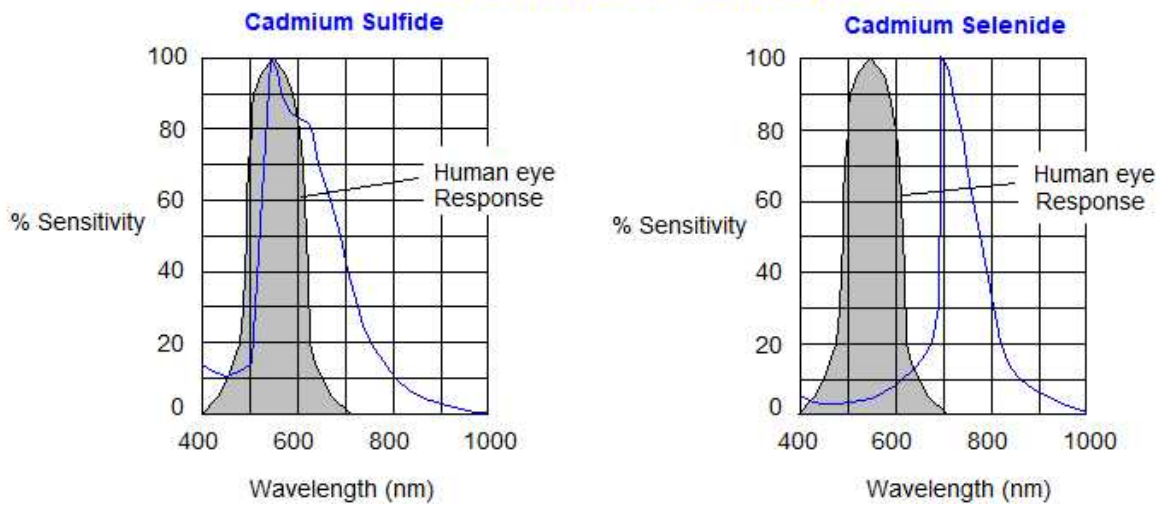
The spectral responses are illustrated in Fig. 3-37. Observe in Fig. 3-37 the resistance of a photoconductive cell decreases as the light intensity increases. The light intensity is measured in lumens per square meter (lm/m^2)²⁷. Luminous flux is the rate at which *visible* light energy is produced by a light source or the rate at which it is received on a surface.

One lumen is equivalent to 1.496 mW of optical power.

$$\text{Light intensity} = \frac{\text{Optical power}}{\text{Surface area}} = \frac{1.496 \text{ mW}}{\text{m}^2} = \frac{\text{lumen}}{\text{m}^2} = \frac{\text{lm}}{\text{m}^2} \quad (3-7)$$

²⁷Luminance has units of lux (Lx) in the SI system. One lux is equal to 1 lm/m^2 . Many manufacturers prefer to use the more intuitive lm/m^2 . This tends to reduce the number of phone calls from baffled electrical engineers and technicians.

Photoconductive Cell Response



CELL RESISTANCE vs. ILLUMINANCE

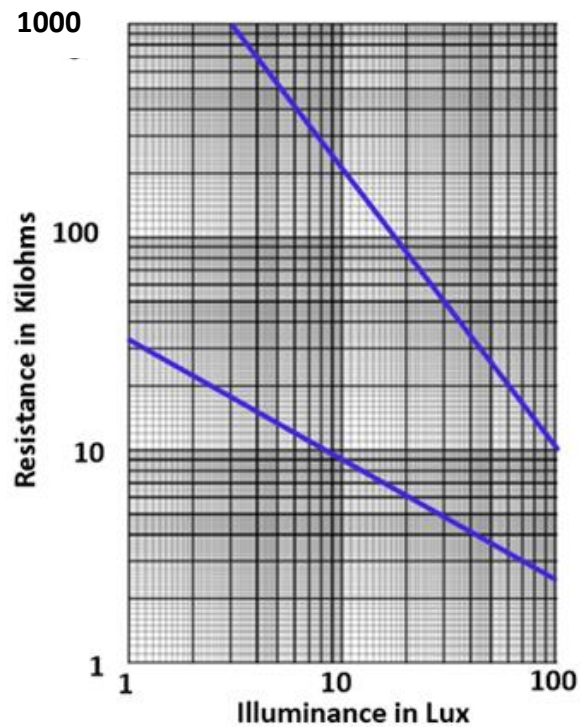


Figure 3-37.

Observe the graph of cell resistance versus illumination is plotted on (non-linear) a log-log scale, which makes the plots appear to be linear. The actual graphs are non-linear. This is not intended to be a deception. A logarithmic scale is used to compress the data so that its wide range can be presented compactly. (Think how difficult it would be to set up a *linear* graph which ranges from 1 to 1000 with enough resolution to read it accurately.) The two plots were derived from data supplied by a cell manufacturer. It shows the range of possible responses for the photoconductive cell.

The PIN Photodiode

The schematic symbols for the photodiode are provided in Fig. 3-38.



Figure 3-38.

In Fig. 3-39(a) we see a “regular” p - n junction with a window lens to expose the depletion region to light. Figure 3-39(b) shows the photodiode design used most widely. It incorporates a layer of intrinsic (pure and undoped) semiconductor between the p and n regions of the diode. The resulting structure is p - i - n and is usually written *PIN*. The basic structure is illustrated Fig. 3-39(c).

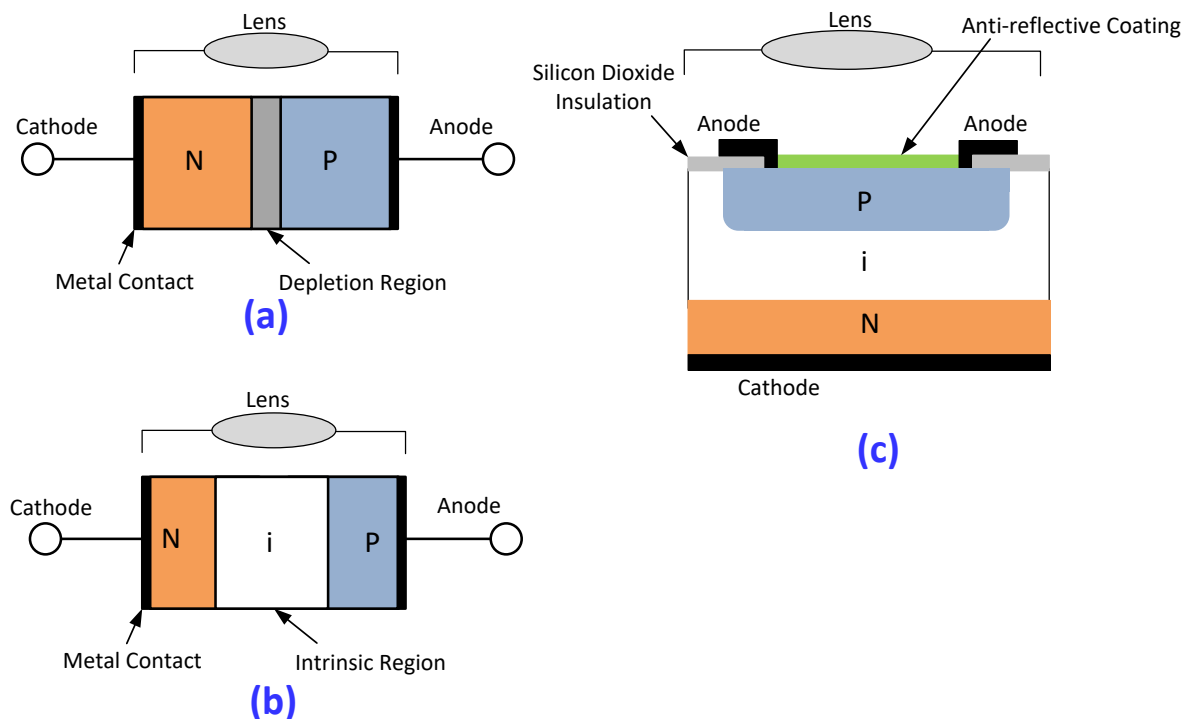


Figure 3-39.

Photodiodes are operated under reverse bias. When a “regular” p - n junction is reverse biased thermal energy produces minority carriers in the depletion region. These minority carriers produce a reverse current component called the reverse saturation current (I_S). In Fig. 3-39(a) a window is constructed to expose the depletion region to light energy. In this case the photons produce a reverse current that increases with light intensity.

The scheme in Fig. 3-39(a) is not very effective. The depletion region width may be too narrow to capture enough photons to generate a sufficiently large current. Further, contributions to the reverse current by the p - and n -regions is very limited. While the carriers may diffuse into the depletion region to contribute to the reverse current, diffusion takes time and that limits how quickly a photodiode can respond. The PIN photodiode [Fig. 3-39(b)] mitigates some of these problems.

The intrinsic region is devoid of majority carriers just like the depletion region. Its width is controlled to maximize the capture of photons. This raises the efficiency of the design – more current for the same light intensity. A capacitance is formed between the p - and n -regions. The p and n regions act like the plates of a capacitor. The depletion and intrinsic regions act like an insulator or dielectric. **Capacitance decreases as the plates are moved further apart.** When we compare Fig. 3-39(a) and Fig. 3-39(b) we see the plates of the capacitor are further apart in Fig. 3-39(b). This means there is less capacitance to slow down the response. (We investigate this further in section 3-10.) PIN photodiodes are used in high-speed fiber optical fiber data communications systems where data rates can be on the order of 160 Gbits per second.

The structure of a PIN photodiode is illustrated in Fig. 3-39(c), the metallization for the anode and cathode connections is shown. The actual anode metallization is circular. Silicon dioxide (SiO_2) is formed by blowing heated oxygen across silicon. The resulting glass-like material is an excellent electrical insulator [see Fig. 1-8]. In this application it is used to prevent shorting the p -region to the i -region.

A partial photodiode data sheet is provided in Fig. 3-40. Rather than lux or lumens/meter², this manufacturer is using mW/cm². The partial data sheet represents the kind of information manufacturers will provide.

PIN Photodiode in a “Sidelooker” Package

Features

- Daylight filter
- Sidelooker package
- Pin photodiode
- Wide reception angle, 120°



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters	Value	Units
T_{OPR}	Operating Temperature	-40 to +85	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to +85	$^\circ\text{C}$
T_{SOL-I}	Soldering Temperature (Iron)	240 for 5 sec.	$^\circ\text{C}$
T_{SOL-F}	Soldering Temperature (Flow)	260 for 10 sec	$^\circ\text{C}$
V_R	Reverse Voltage	32	V
P_D	Power Dissipation Derate linearly 2.5 mW/ $^\circ\text{C}$ above 25°C .	150	mW

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_R	Reverse Voltage	$I_R = 0.1\text{mA}$, $E_e = 0\text{mW/cm}^2$	32			V
$I_{R(D)}$	Dark Reverse Current	$V_R = 10\text{V}$, $E_e = 0\text{mW/cm}^2$			30	nA
λ_{PK}	Peak Sensitivity	$V_R = 5\text{V}$		940		nm
Θ	Reception Angle at 1/2 Power			± 60		$^\circ$
I_{PH}	Photo Current ⁽⁸⁾	$E_e = 1.0\text{mW/cm}^2$, $V_R = 5\text{V}$	30			μA
I_{SC}	Short Circuit Current ⁽⁸⁾	$E_e = 1.0\text{mW/cm}^2$		18		μA
C	Capacitance	$V_R = 3\text{V}$		25		pF
t_r	Rise Time	$V_R = 5\text{V}$, $R_L = 1\text{k}\Omega$		50		ns
t_f	Fall Time	$V_R = 5\text{V}$, $R_L = 1\text{k}\Omega$		50		ns

Figure 3-40.

A photodiode (Fig. 3-41) incorporates a reverse-biased p - n junction. Because the intrinsic region has very few charge carriers, its resistance is very large. An incident photon (of the proper wavelength) can give a bound electron enough energy to go from the valence energy band to the conduction energy band. When this occurs both a free electron and a hole are produced. These charge carriers are free to move. An increase in the number of carriers within the intrinsic region will increase the reverse current. Therefore, *the reverse current will increase as the light intensity is increased* [see Fig. 3-42(a)]. The light intensity is given in lm/m^2 .

Photo Diode Operation

The reverse current increases as the light intensity increases.

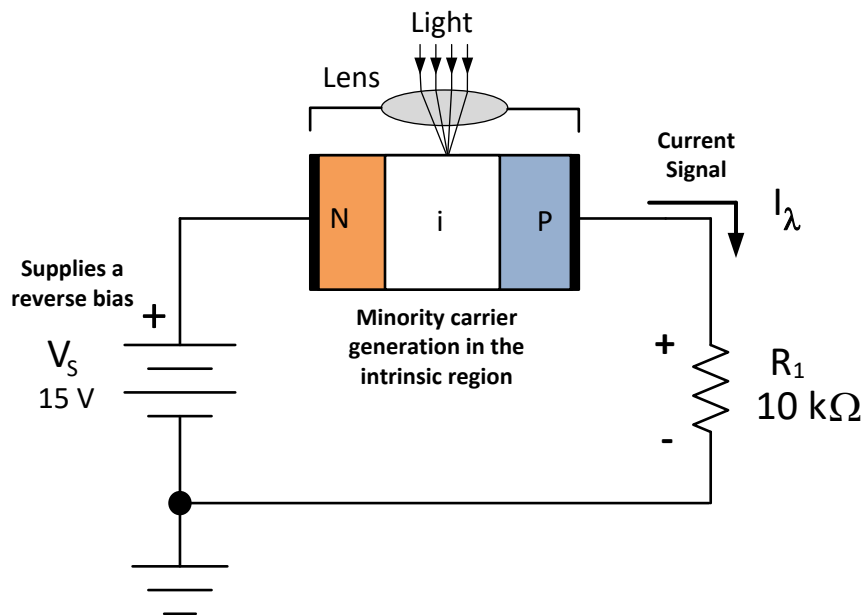


Figure 3-41.

When the diode's lens is covered, a small (thermally produced) reverse current will flow. This is called the **dark current** [see Fig. 3-42(a)]. Observe that it is also possible to operate in the fourth quadrant of the V - I characteristic. This is called the **photovoltaic region**. In this region of operation, the photo diode acts like a voltage source. Current leaves its positive terminal. *Current entering the positive terminal is called positive while current leaving positive terminal is called negative*. This is illustrated further with the V - I curve for a "regular" voltage source in Fig. 3-42(b). In the fourth quadrant, the voltage source is delivering energy. In the first quadrant it receives energy (like a resistor).

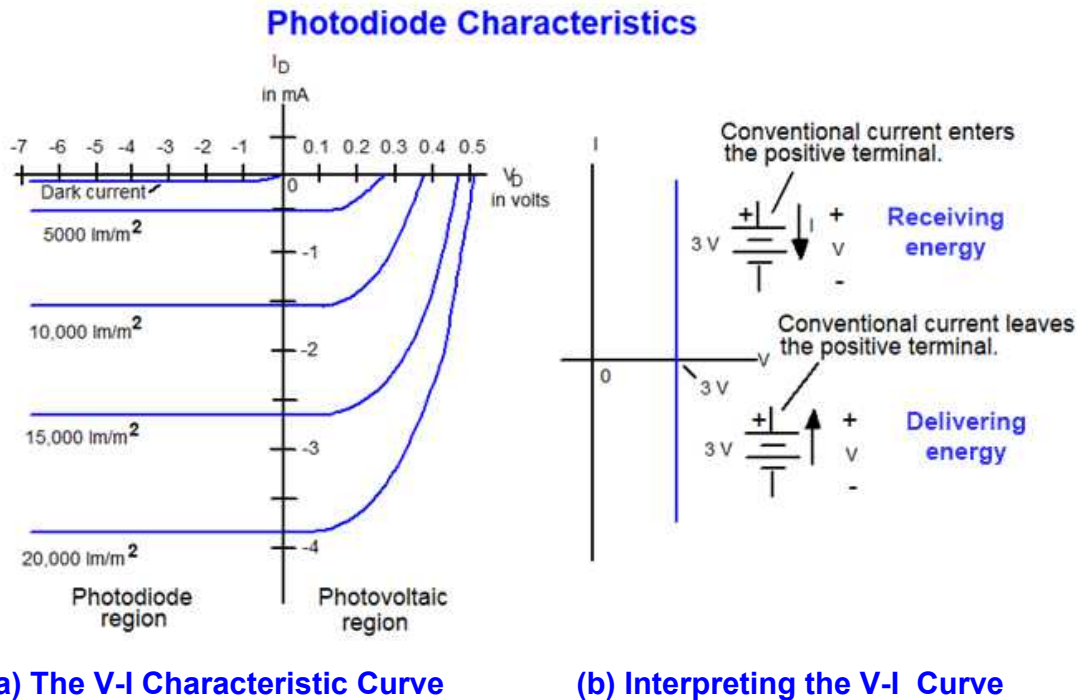


Figure 3-42.

Photodiodes are normally used in the reverse-bias mode of operation. Increased light intensity causes their reverse current to increase. Photodiodes are used in conjunction with LEDs in printers to determine when the printer is out of paper. The light produced by the LED is blocked by the paper, so the photodiode remains in the dark. When the paper supply is exhausted, light from the LED can reach the photodiode. The photodiode's increased current produces a signal, which alerts the printer control system.

Photodiodes are also used in the infrared-remote control systems found in televisions, radios, and in sound systems. To increase the detection area and the sensitivity, photodiodes can be placed in parallel. Consider Example 3-6.

Example 3-6. The three photodiodes shown in Fig. 3-43(b) have the characteristic curves illustrated in Fig. 3-42(a). Determine the voltage developed across resistor R_I if all three diodes are exposed to 5000 lm/m^2 of light intensity.

Solution: Examining the circuit, we see the diodes are reverse biased. Since I_λ is defined as a reverse current we can state

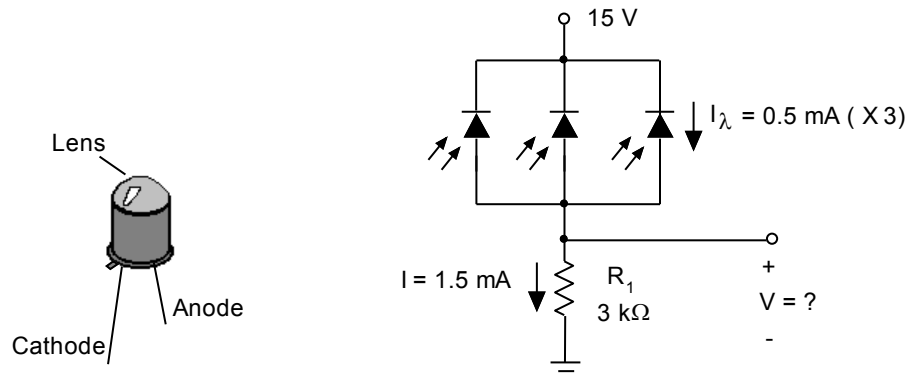
$$I_\lambda = -I_D$$

By inspection of Fig. 3-42(a) we see that at 5000 lm/m^2 the photodiodes have a reverse current of about 0.5 mA . (This means $I_D = -0.5 \text{ mA}$ and $I_\lambda = 0.5 \text{ mA}$.) Since we have three diodes in parallel, the total current is 1.5 mA . The voltage across R_I is determined below.

$$V = IR_I = (1.5 \text{ mA})(3 \text{ k}\Omega) = 4.5 \text{ V}$$

The Circuit for Example 3-6.

(The photodiodes "see" 5000 lm/m^2)



(a) Photodiode (metal can) package.

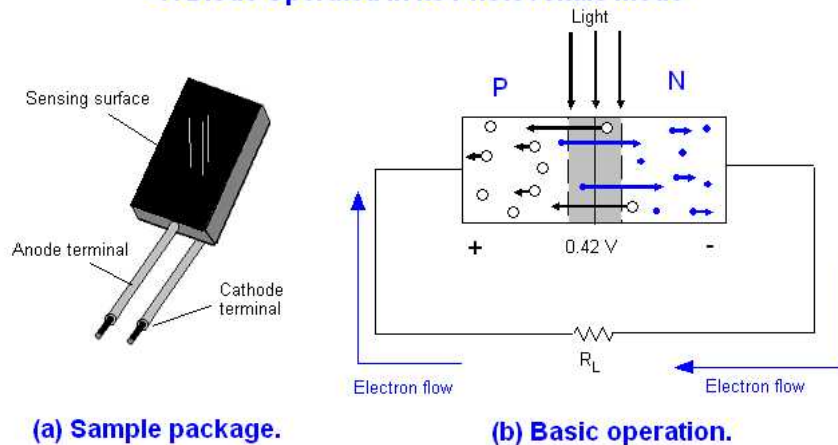
(b) The circuit.

Figure 3-43.

The Solar Cell

Essentially, a **solar cell** is a large photodiode operated in its photovoltaic mode. It is used to convert light energy into electrical energy. Low-current photodiodes are available packaged in a small can with a lens or window on top such as that indicated in Fig. 3-43(a). Solar cells require much larger surface areas. Consider a solar cell packaged in a rectangular shape [Fig. 3-44(a)]. The basic operation of a solar cell is described in Fig. 3-44(b). Its schematic symbols are given in Fig. 3-45.

The Solar Cell - A Diode Operated in its Photovoltaic Mode



(a) Sample package.

(b) Basic operation.

Figure 3-44.

Solar Cell Schematic Symbols

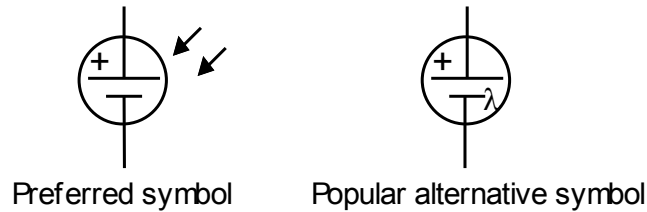


Figure 3-45.

Solar Cell Operation

Recall that a depletion region forms at a p - n junction [Fig. 3-44(b)]. The depletion region consists of ions locked into the crystalline structure. The barrier potential associated with the depletion region prevents majority carriers from diffusing across the p - n junction. Minority carriers (holes on the n side and electrons on the p side) are generated within the depletion region when subjected to light energy. Solar (photovoltaic) cells are designed so that minority carriers will be created by radiant energy striking the junction. (Minority carriers sufficiently close to the depletion region will also be swept across it.)

Radiant energy of the proper wavelength striking a valence electron creates a hole-electron pair. If a hole-electron pair is created on the n side, the electron remains as a majority carrier. However, the hole may diffuse into the depletion region and be swept across the p - n junction. Similarly, if a hole-electron pair is created on the p side, the hole remains as a majority carrier. The associated electron may diffuse into the depletion region and be swept across the p - n junction. This movement of minority carriers constitutes an electric current. The magnitude of the current depends on the number of hole-electron pairs created, which in turn depends on the radiant light intensity striking the cell.

No external bias is required to produce this current. The effect of electrons leaving the n side of the junction makes it negative. Similarly, the effect of the (positive-acting) holes on the p side makes it positive. The p - n junction is a voltage source.

Solar Cell Efficiency and Applications

The energy efficiency of solar cells is under constant improvement reaching up to 23 percent currently (2019). Small solar cells are used in low-power applications like watches, calculators, and cameras.

The cost associated with the manufacturer of solar cells has decreased dramatically since 2009. Consequently, many municipalities are constructing solar arrays to reduce their utility costs. Figure 3-46 provides a partial data sheet data sheet for a photovoltaic (PV) solar cell.

The overall cell dimension is about 6.14 inches square. The open-circuit voltage is ranges from 0.620 to 0.612 V. Many junctions are placed in parallel to provide a short-circuit current that can range from 8.88 to 8.75 A. Semiconductors are very sensitive to the effects of temperature. The open-circuit voltage has a negative temperature coefficient and the short-circuit current has a positive temperature coefficient.

Monocrystalline Silicon Solar Cell



Typical Values

- **Dimensions:** 6.14 in. X 6.14 in. (156 mm X 156 mm)
- **Percent Efficiency (η):** 17.5% to 18.4%
- **Open Circuit Voltage (V_{oc}):** 620 mV
- **Short Circuit Current (I_{sc}):** 8.8 A
- **Operating Voltage:** 500 mV
- **Operating Current:** 8.60 A to 8.80 A
- **Power Classification:** 4.30 W to 4.40 W
- **Peak Operation:** 500 nm to 900 nm

Figure 3-46.

Figure 3-47 illustrates the construction of a solar module. Individual solar cells are placed in series to increase the solar module voltage. Series strings can be connected in parallel to increase the available module current.

Monocrystalline Solar Module

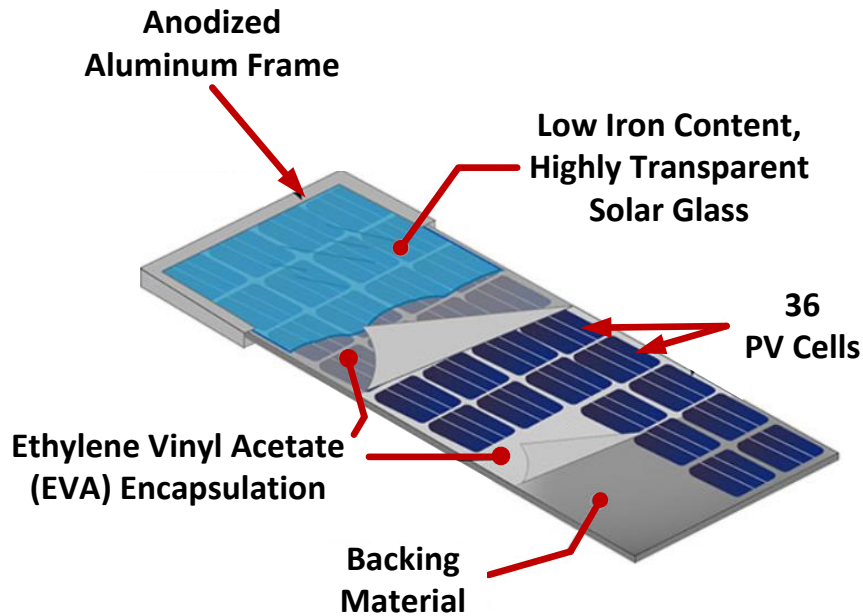


Figure 3-47.

A partial data sheet of a solar module is given in Fig. 3-48. The open-circuit voltage (V_{oc}) is 38.3 V and the short-circuit current (I_{sc}) is 9.09 A. (Current sources can be shorted while voltage sources get very upset.)

Monocrystalline Silicon 260 W Solar Module



Module Key Specifications:

- Solar module has 60 cells (6 X 10).
- Two series strings of 30 cells each.
- 1000 V insulation rating.
- Length by width is 65 in. X 39 in. (1662 mm X 990 mm).

Electrical Specifications Under Standard Test Conditions (STC):

- Maximum power output $P_{max} = 260 \text{ W}$
- Maximum power output voltage $V_{mp} = 31.0 \text{ V}$
- Maximum power output current $I_{mp} = 8.39 \text{ A}$
- Open circuit output voltage $V_{oc} = 38.3 \text{ V}$
- Short circuit output current $I_{sc} = 9.09 \text{ A}$

Figure 3-48.

Figure 3-49 provides an idealized V - I characteristic curve for a solar module. It behaves like a solar irradiance-controlled²⁸ current source. Current flows out of its positive terminal. That is taken as the reference so that places the V - I characteristic in the first quadrant. **The solar industry uses the I - V label as opposed to V - I .**

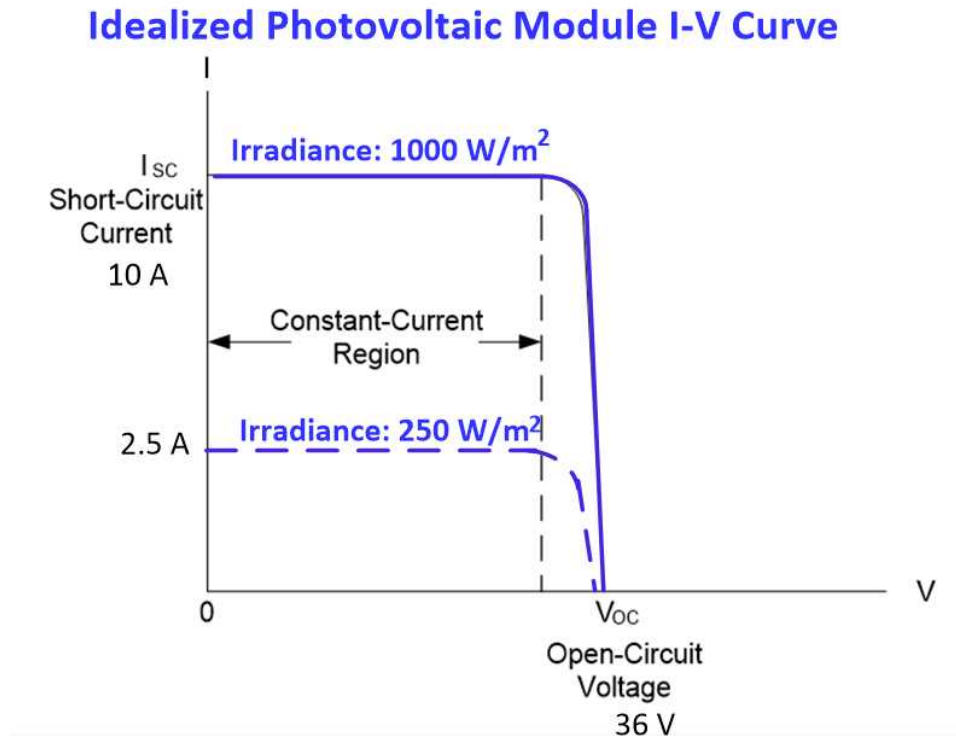


Figure 3-49.

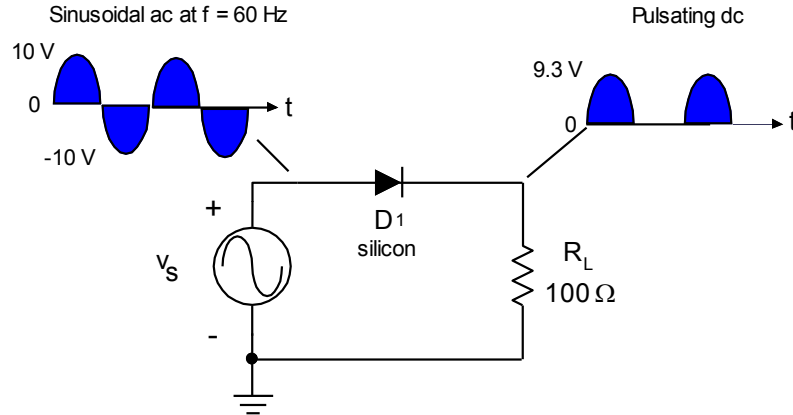
3-8 Frequency Effects on P - N Junction Operation

In Fig. 3-50(a) we see a diode that is being driven by a sinusoidal voltage source. During the positive half cycle, the diode is forward biased, and therefore conducts. The diode may be replaced with its knee-voltage diode model as indicated in Fig. 3-50(b). Because the (silicon) diode is assumed to drop 0.7 V, the peak voltage across the load resistor R_L is 9.3 V.

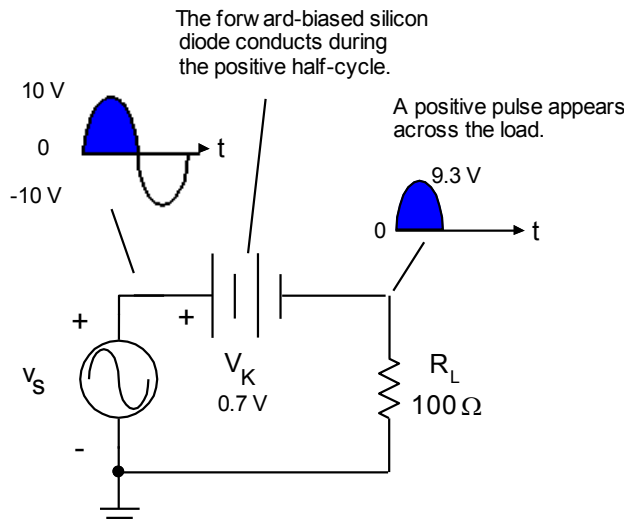
During the negative half cycle, the diode is reverse biased. Consequently, the diode may be modeled as an open switch as shown in Fig. 3-50(c). Because the current through R_L is zero, there is no voltage drop across it. The diode action converts the sinusoidal AC input voltage into a pulsating DC output voltage as indicated in Fig. 3-50(a). (A DC waveform has a positive or negative average value. A pure AC waveform has an average value of *zero*.) The diode circuit is called a **half-wave rectifier**.

²⁸ Solar irradiance is the power delivered per unit area and in this case, has units of watts per square meter (W/m^2).

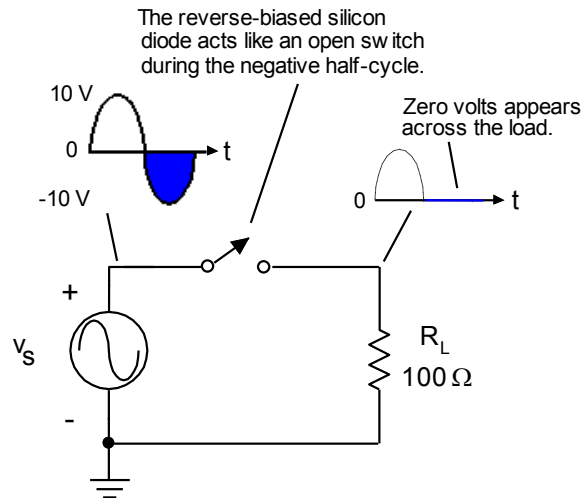
The Operation of the Half-Wave Rectifier Circuit



(a) The half-wave rectifier.



(b) The positive half-cycle.



(c) The negative half-cycle.

Figure 3-50.

The diode reverses from conduction to nonconduction very quickly, but the diode's switching action is *not* instantaneous. This becomes obvious as we increase the frequency of the AC source driving the half-wave rectifier circuit. At low frequencies [Fig. 3-51(a)] the diode's switching time is negligibly small. At higher frequencies, the diode begins to permit significant reverse current flow [Fig. 3-51(b) and (c)]. It takes a significant amount of time for a diode to switch from conduction (on) to nonconduction (off). Multisim was used to generate the waveforms for the 1N4148-silicon switching diode indicated in Fig. 3-51. A more sluggish diode such as a 1N4001 rectifier will exhibit the same kind of behavior, but at much lower frequencies. Consequently, the 1N4001-diode waveforms can be duplicated easily in the laboratory.

Frequency Effects on Diode Switching

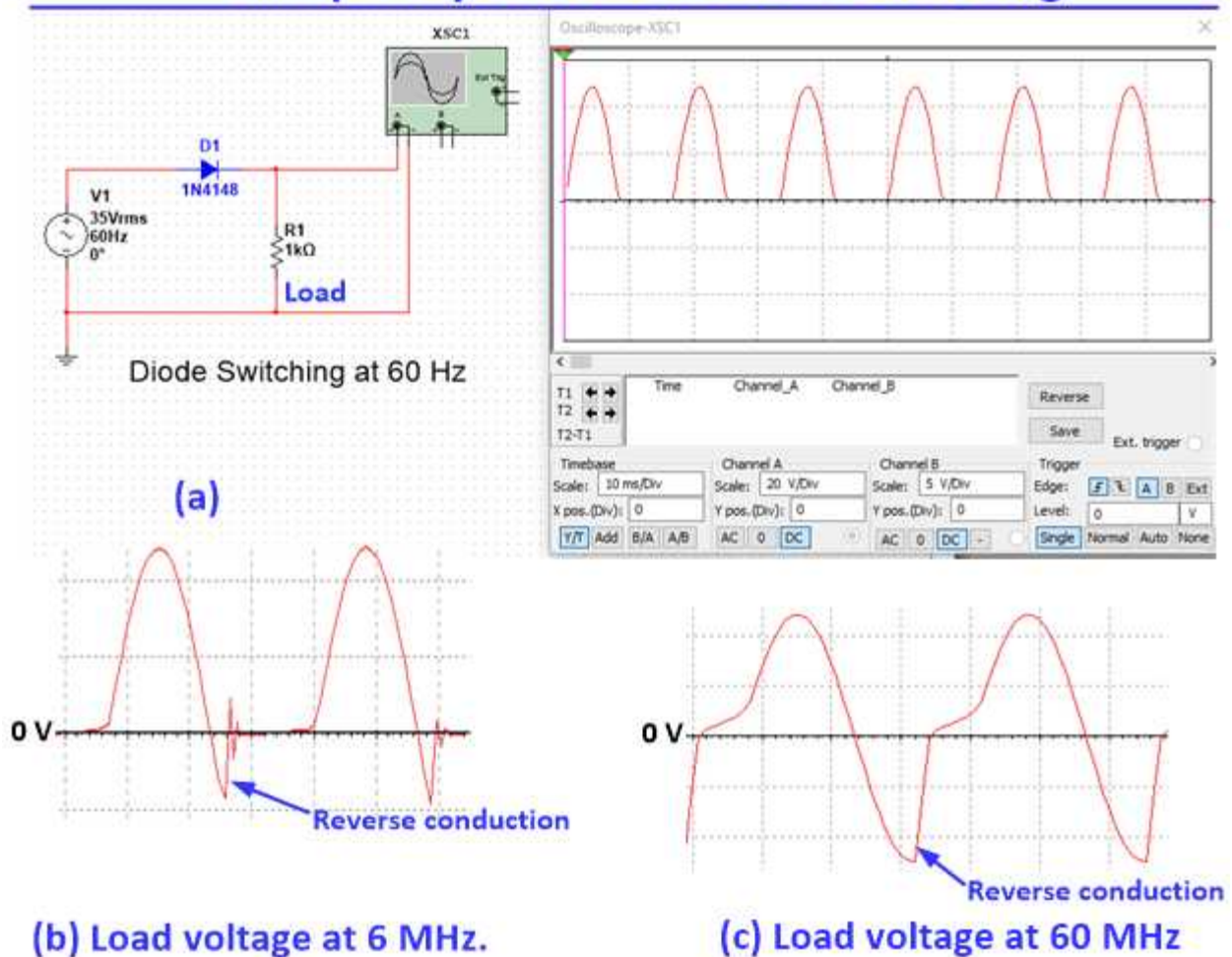


Figure 3-51.

Example 3-7. Use Multisim to construct the circuit shown in Fig. 3-51(a). Connect a two-channel oscilloscope as shown. Edit the source to provide 35 Vrms. Adjust the vertical sensitivity to 20 V/Div. Place the trigger in Auto mode. Run the simulation. The waveform may appear to run (move) across the screen. Change the trigger mode to Single. The waveform will become stationary. You may stop the simulation. Use Multisim to generate the load voltage waveforms shown in Fig. 3-51(b) and (c).

Solution: Double click on the source and change its frequency to 6 MHz. Run the simulation again. You will need to adjust the time base to display two or three cycles. Again, you can start the simulation with the oscilloscope in its Auto mode and then switch to the Single mode. You should see a waveform *like* the one shown in Fig. 3-51(b). Repeat the procedure with the source set to 60 MHz.

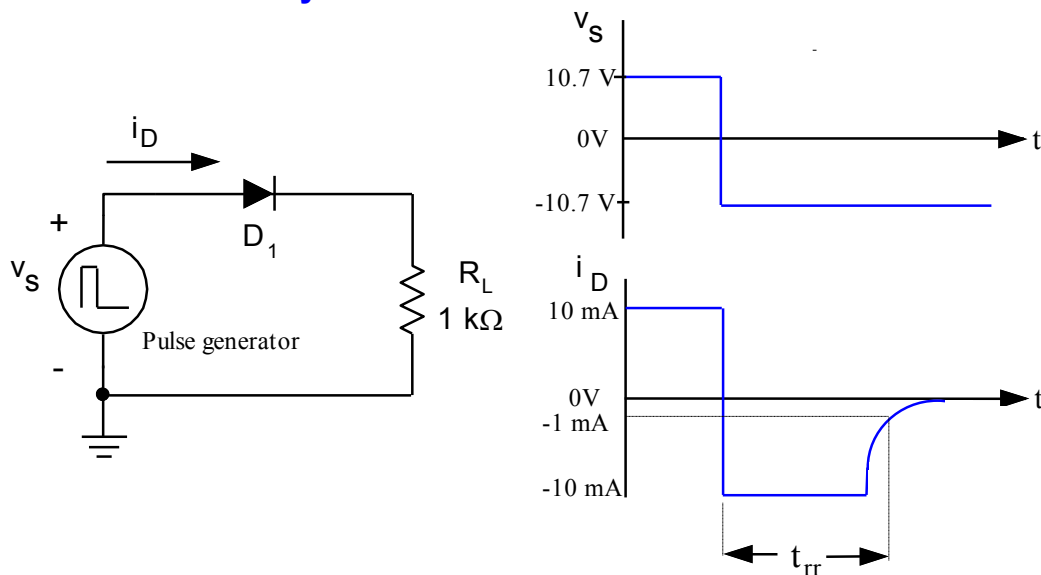
The Diode's Reverse Recovery Time (t_{rr})

When a p - n junction is forward-biased, electrons from the n side enter the p region. Similarly, holes from the p side move into the n region. As the carriers diffuse into the region on the opposite side of the junction, they become *minority* carriers. The minority carriers slowly recombine with the majority carriers. When the bias on a p - n junction is abruptly changed from forward to reverse, the minority carriers must be removed via drift and recombination before the p - n junction's depletion region can widen and shut off the reverse current.

A test circuit and waveforms are given in Fig. 3-52. **The reverse recovery time is denoted as t_{rr} on manufacturers' diode data sheets.** Typical values can range from (sluggish) microseconds to (speedy) nanoseconds. The reverse recovery time is defined on Fig. 3-52(b).

Diode Reverse Recovery Time (t_{rr})

- The time required for the diode's reverse current to decay to 10% of its maximum value.



(a) The test circuit.

(b) Waveforms.

Figure 3-52.

A Forward-Biased P-N Junction Exhibits Diffusion Capacitance

A forward-biased diode has a narrow depletion region. Recall the depletion region is formed by the ions embedded within the crystal lattice. These stored charges give rise to a capacitive effect known as *diffusion capacitance*. When a diode is reverse biased the depletion region must widen. This requires that the minority carriers on each side of the junction be removed. Since the minority carriers must diffuse or recombine, the process is relatively slow. This delay in the charge rearrangement at the junction is similar in nature to a capacitance. Diffusion capacitance also affects the behavior of bipolar transistors. Multisim includes a diffusion capacitance in both its diode and transistor models.

3-9 The Schottky Diode

A metal layer deposited on a lightly doped *n*-type silicon material creates a *Schottky-barrier*, or *hot-carrier*, diode. This unique diode is described in Fig. 3-53. The electrons in the *n*-type region are at higher energy levels than those in the metallic side. Since electrons always seek the lowest energy level, they diffuse from the *n* side toward the metallic side. A resulting thin, dense layer of ions forms at the interface [see Fig. 3-53(a)]. The corresponding barrier potential is typically 0.3 V. Again, it is the barrier potential that stops the diffusion process. Note that when metal is placed next to a *heavily* doped *n*-type region, an *ohmic connection* is formed. An ohmic connection passes current equally well in both directions. The diode is built on a *p*-type substrate.

The schematic symbols for the Schottky diode are shown in Fig. 3-53(b). Observe the cathode forms an “S”. The *V-I* characteristic of the Schottky diode is depicted in Fig. 3-53(c). (A silicon diode *V-I* characteristic has been included for reference.) The knee-voltage is defined to be equal to the barrier potential (0.3 V). Subsequently, 0.3 V is used in the knee-voltage diode model for the forward-biased Schottky diode.

The Schottky Diode

- A high-speed diode with a reverse recovery time of picoseconds and a low forward voltage drop.

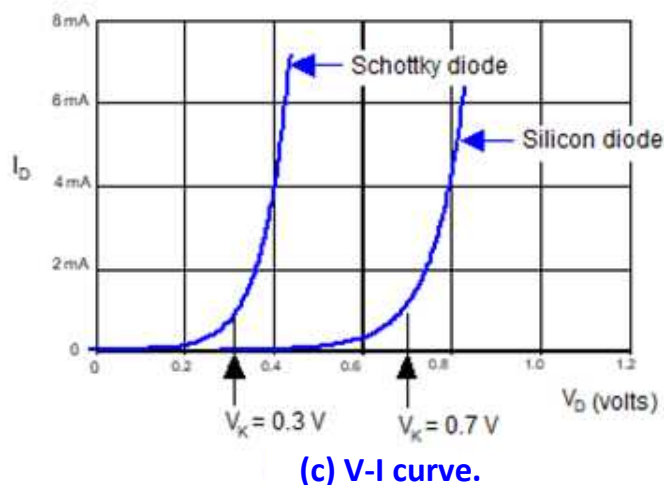
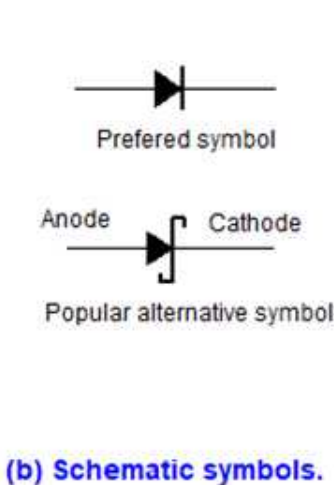
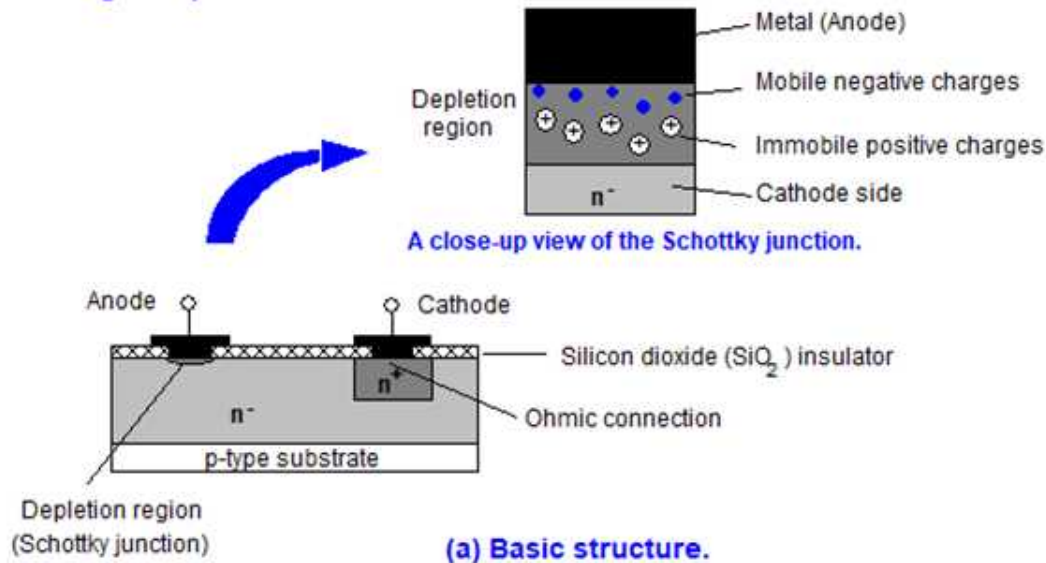


Figure 3-53.

Recombination is no longer involved because the injected electrons are majority carriers in the metal. Since minority carrier storage is no longer a factor, ***the Schottky diode can switch from conduction to nonconduction in a few picoseconds.*** Because the electrons travel through the diode with conduction-band energies, they are referred to as being ***hot carriers***.

Schottky diodes are very efficient because of their low forward voltage drops (since $P = V_D I_D$), and they are used in high-speed circuits. They are ideal in reverse-polarity protection circuits. Consequently, a Schottky diode can be used to replace the silicon diode (D_1) indicated in Fig. 3-21. Schottky junctions are also used in high-speed digital integrated circuits and other applications.

3-10 The Varactor Diode

As we saw in Section 3-8, a diffusion capacitance is associated with a forward-biased p - n junction. There is also a capacitance associated with a *reverse-biased* p - n junction. This capacitance is called a *junction capacitance*. To understand these capacitive effects, we can draw an analogy between the parallel-plate capacitor and the depletion region at the p - n junction. Consider Fig. 3-54(a).

When any two conductors (or semiconductors) are separated by an insulator (such as the depletion region) a capacitance will exist between them. Capacitance (C) is defined by Eq. 3-8.

$$C = \epsilon \frac{A}{d} \quad (3-8)$$

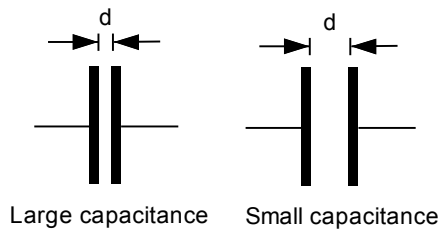
where ϵ (epsilon) is the dielectric constant, A is the area of one of the plates, and d is the distance between the plates. The capacitance is inversely related to the distance d between the plates. As the distance increases, the capacitance decreases. Conversely, as the distance decreases, the capacitance increases.

The capacitance associated with the p - n junction obeys this fundamental relationship. When a p - n junction is *forward-biased*, its depletion region is very *narrow*. Consequently, the capacitance is relatively large. When a p - n junction is *reverse-biased*, its depletion region *widens*. Subsequently, its capacitance is reduced. These ideas are depicted in Fig. 3-54(b). Equation 3-8 describes the linear relationship between the distance (d) between a capacitor's plates and its capacitance. However, a p - n junction has a **highly non-linear** relationship between its capacitance and the DC bias across it. This is illustrated in Fig. 3-54(c).

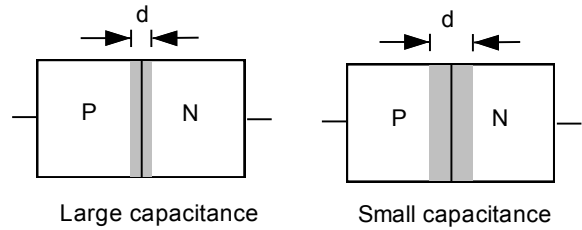
Varactor is a contraction for variable reactor. A varactor diode's schematic symbol is illustrated in Fig. 3-54(d). The varactor diode is also called a voltage-variable capacitor (VVC), a *varicap*, and a *tuning diode*. Varactor diodes are used in the tuning circuits found in DVD players/tuners, televisions, and AM/FM receivers.

The Varactor Diode

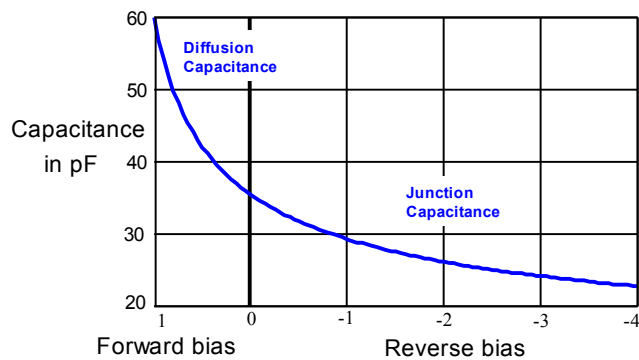
- A voltage-variable capacitor used to tune circuits.



(a) The parallel-plate capacitor.



(b) The p-n junction capacitance.



(c) The p-n junction capacitance versus voltage.



(d) Schematic symbol.

Figure 3-54.

Problems for Chapter 3

Drill Problems

Section 3-1

- 3-1. What is the primary purpose of an *amplifier*? Ideally, what should its input act like?
- 3-2. Why is it necessary to place a *diode clipper circuit* across the input of an amplifier? Explain briefly.
- 3-3. The circuit (R_I and the two diodes) in Fig. 3-55 is called a (an) _____.
 - (a.) Clamper
 - (b.) Limiter
 - (c.) Clipper
 - (d.) Clapper
 - (e.) Both b and c.
 - (f.) None of the choices.

The Circuit for Problems 3-3 through 3-5.

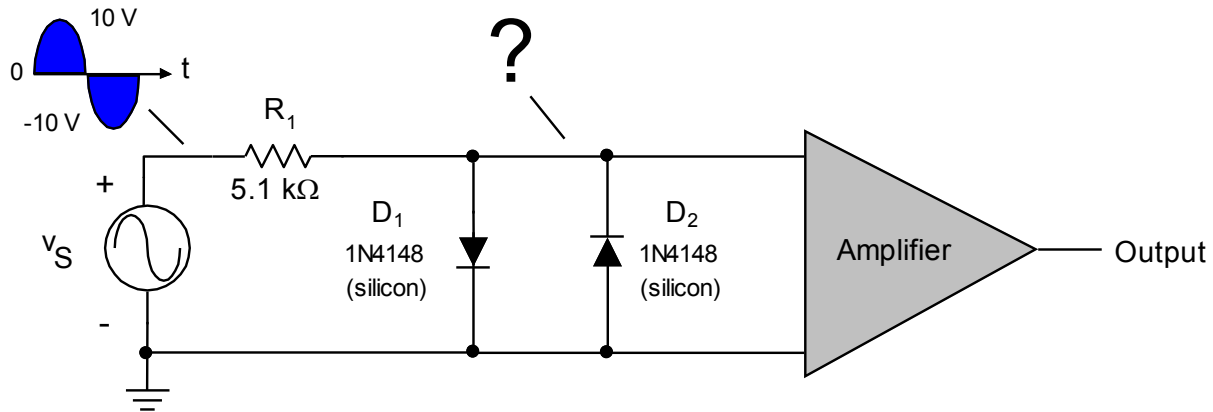


Figure 3-55.

- 3-4. Sketch the waveform that will appear across the amplifier's input in Fig. 3-55. Be sure to label the positive and negative peak values.
- 3-5. The input voltage has been reduced to 0.25 V peak. Sketch the waveform that will appear across the amplifier's input in Fig. 3-55. Be sure to label the positive and negative peak values.

The Circuit for Probs. 3-6 and 3-7.

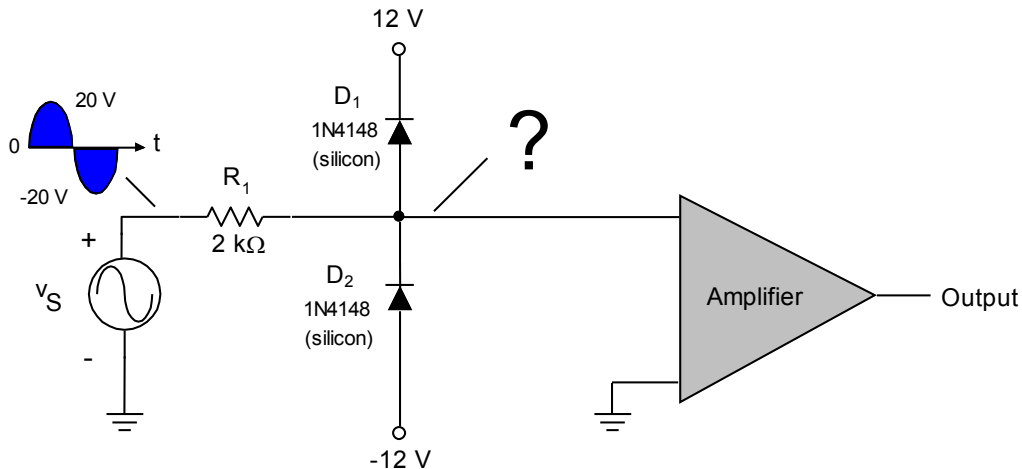


Figure 3-56.

- 3-6. Sketch the waveform that will appear across the amplifier's input in Fig. 3-56. Be sure to label the positive and negative peak values. What will be the current through diode D_1 when the source is at its 20-V peak?
- 3-7. The input voltage has been reduced to 5 V peak. Sketch the waveform that will appear across the amplifier's input in Fig. 3-56. Be sure to label the positive and negative peak values.

Section 3-2

- 3-8. The signal produced by the source v_s in Fig. 3-6 has been increased to 15 V peak. Sketch the waveform that will appear across resistor R_I . Be sure to label the positive and negative peak values. What is the DC level across R_I ?
- 3-9. Given the circuit shown in Fig. 3-57, sketch the waveform that will appear across resistor R_I . Be sure to label the positive and negative peak values. What is the DC level across R_I ?
- 3-10. Determine the *minimum* time constant for the circuit given in Fig. 3-57 if the *lowest* signal frequency is 1 MHz. If R_I is to be 1 k Ω , determine the nearest *standard* capacitor value. (Standard capacitor values can be found using an internet search engine.)

Section 3-3

- 3-11. The forward voltage drop across a diode demonstrates a _____ (positive, negative, zero) temperature coefficient (tempco).
- 3-12. A silicon diode has a forward voltage drop of 0.65 V at 25°C. Determine its voltage drop at 55°C and at 5°C.
- 3-13. A germanium diode has a forward voltage drop of 0.32 V at 25°C. Determine its voltage drop at 65°C and at 20°C.

The Circuit for Problems 3-9 and 3-10.

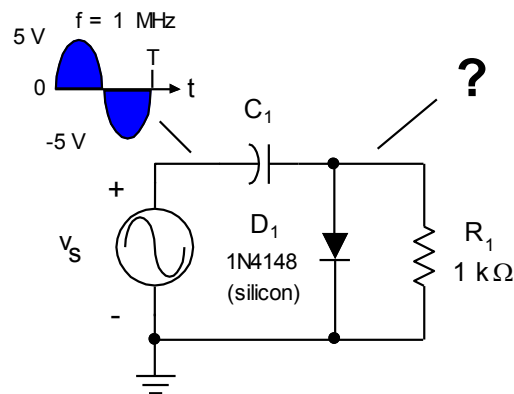


Figure 3-57.

- 3-14. The reverse saturation current through a diode demonstrates a _____ (positive, negative, zero) temperature coefficient (tempco).
- 3-15. A silicon diode has a reverse saturation current of 2 nA at 25°C. Determine its reverse saturation current at 55°C and at 5°C.
- 3-16. A silicon diode has a reverse saturation current of 10 nA at 25°C. Determine its reverse saturation current at 65°C and at 10°C.

Section 3-4

- 3-17. A true *zener* diode (as discussed in Section 2-6) has a breakdown voltage _____ (above, below) 5 volts, and a _____ (positive, negative) temperature coefficient.
- 3-18. A true *avalanche-breakdown* diode (as discussed in Section 2-6) has a breakdown voltage _____ (above, below) 5 volts and a _____ (positive, negative) temperature coefficient.
- 3-19. *Thermistors* demonstrate a _____ (positive, negative) temperature coefficient of resistance.
- 3-20. As the temperature of a thermistor is *raised*, its resistance will _____ (increase, decrease) in a _____ (linear, nonlinear) fashion.
- 3-21. The data for a Raychem Corp. RUE PolySwitch PTC resistor is given in Table 3-2. Find the maximum voltage drop across the device if 50 mA flows through it. Find current-limit value (I_{LIMIT}) for the device if it drops 24 V while it is protecting a circuit. Also determine PTC's tripped resistance R_T .

Table 3-2.

The RUE400 PTC Resistor Characteristics

I_H = Hold Current = 4.00 A	R_{UT} = Untripped Resistance = 0.01 to 0.03 Ω
I_T = Trip Current = 8.00 A	R_T = Tripped Resistance = V^2/P_d
P_d = 2.5 W	(where V is the applied voltage)
Maximum Voltage = 30 V	Operating Temperature Range = 0 to 60°C
Maximum Interrupt I = 40 A	

Section 3-5

- 3-22. A *varistor* behaves like a (an) _____ (open, short) until its breakdown voltage is exceeded.
- 3-23. A varistor acts like two back-to-back _____ (rectifier diodes, zener diodes, thermistors) in series.

Section 3-6

- 3-24. An infrared (GaAs) LED is used in the circuit shown in Fig. 3-34(a). Find the forward current (I_D) through it. Assume the knee voltage is 1.2 V.

- 3-25. A green (GaP) LED is used in the circuit shown in Fig. 3-34(a). Find the forward current (I_D) through it. Assume the knee voltage is 2.4 V.
- 3-26. What is a *p-n heterojunction*?
- 3-27. The laser diode in Fig. 3-58 is being pulsed. Using the knee-voltage model, determine the peak forward current through the diode.

The Semiconductor Laser Circuit for Prob. 3-27.

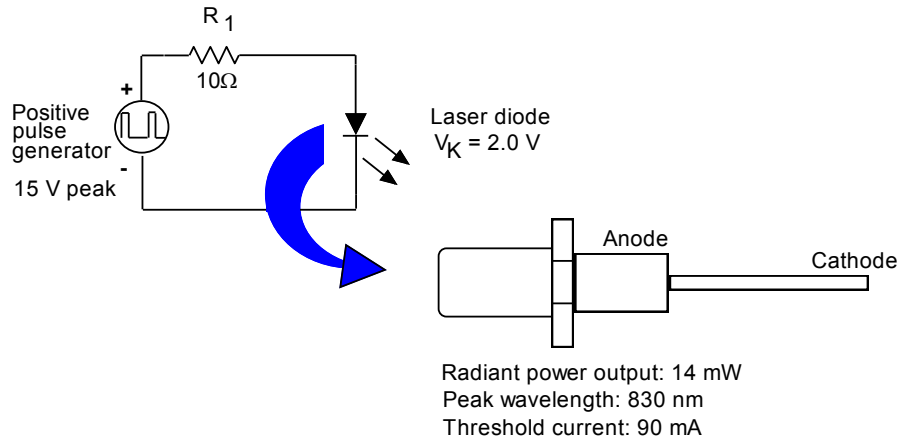


Figure 3-58.

- 3-28. A partial schematic of an amplifier circuit is given in Fig. 3-59. In this case the amplifier's input signal is applied via input jacks *J2-A* and *J2-B* located on the rear panel. LEDs *DS1* and *DS2* are located on the front panel. The amplifier and resistor *R101* are located on the main printed circuit board (PCB) assembly. *J1* is the connector (receptacle) mounted to the printed circuit board. *P1* is the mating plug. The pin numbers (e.g., *J1-3* and *J1-4*) are also indicated. Explain the purpose of the LEDs and the operation of the circuit.

The Circuit for Problem 3-28.

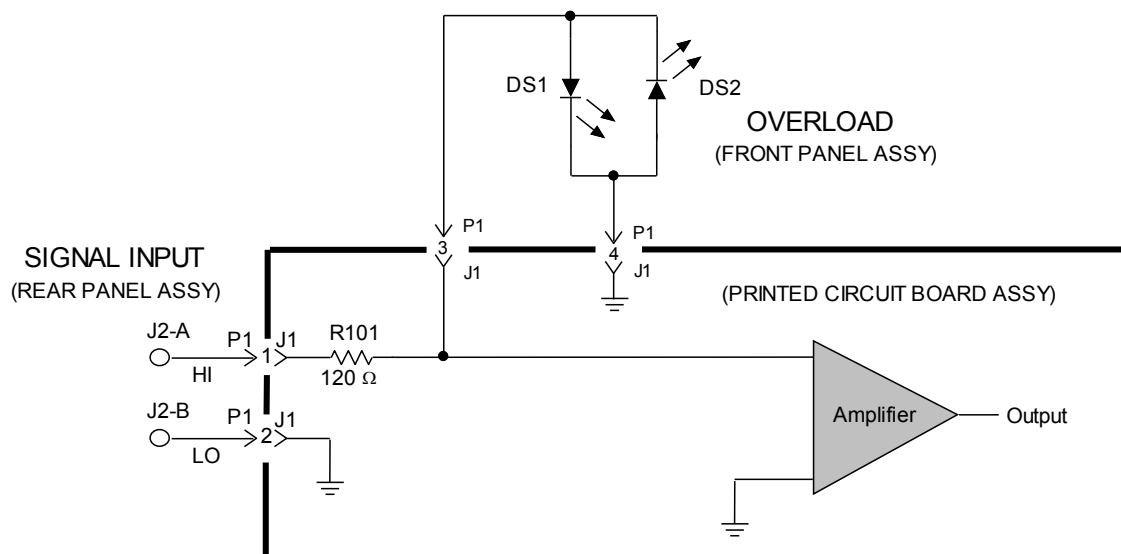


Figure 3-59.

Section 3-7

- 3-29. A *photoconductive cell* has a terminal resistance that _____ (increases, decreases) as the light intensity increases.
- 3-30. A photodiode's reverse current _____ (increases, decreases) as the light intensity increases.
- 3-31. The three photodiodes indicated in Fig. 3-43(b) are exposed to a light intensity of $20,000 \text{ lm/m}^2$. Using the V - I characteristic in Fig. 3-42(a), find the voltage (V) across R_L . R_L has been changed to 300Ω .
- 3-32. Basically, *solar cell* is simply a _____ (photodiode, photoconductive cell, laser diode) that is being operated in its photovoltaic mode of operation.

Section 3-8

- 3-33. Sketch the voltage waveform that will be developed across R_L in Fig. 3-59. Be sure to label its peak value.
- 3-34. Sketch the voltage waveform that will be developed across R_L in Fig. 3-59. Assume that the peak source voltage has been reduced to 5 V. Be sure to label its peak value.

The Circuit for Probs. 3-33 and 3-34.

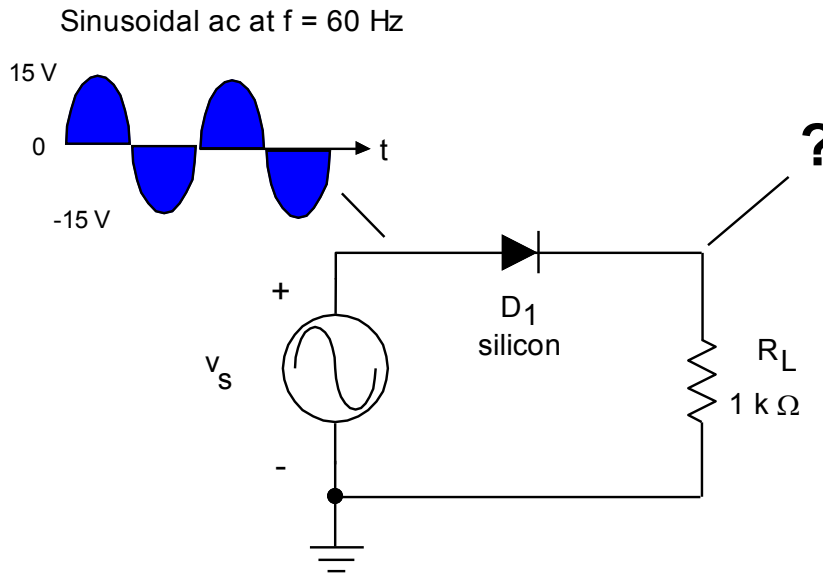


Figure 3-59.

- 3-35. The reverse recovery time (t_{rr}) of a diode is a measure of how long it takes for a diode _____ (turn on, turn off).
- 3-36. Reverse recovery time is caused by _____ (minority, majority) carrier storage at the p - n junction.
- 3-37. Reverse recovery time may be modeled by using a _____ (dynamic resistance, diffusion capacitance, an ideal current source).

Section 3-9

- 3-38. When a *heavily doped* n -type (n^+) semiconductor is placed next to metal a (an) _____ (Schottky barrier, ohmic connection) is formed.
- 3-39. When *lightly doped* n -type (n^-) semiconductor is placed next to metal a (an) _____ (Schottky barrier, ohmic connection) is formed.
- 3-40. A Schottky barrier diode is used in Fig. 3-60. Find the diode's forward current by using the knee-voltage diode model.
- 3-41. A Schottky barrier diode is used in Fig. 3-60. Find the diode's forward current by using the knee-voltage diode model. Assume that V_S is reduced to 3.3 V.

The Circuit for Probs. 3-40 and 3-41.

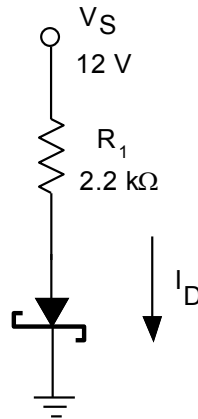


Figure 3-60.

Section 3-10

- 3-42. *Junction* capacitance tends to be _____ (larger, smaller) than *diffusion* capacitance.
- 3-43. Diffusion capacitance tends to _____ (increase, decrease) as the forward bias is increased.
- 3-44. Junction capacitance tends to _____ (increase, decrease) as the reverse bias is increased.
- 3-45. Varactor diodes are normally used in their _____ (forward-, reverse-) biased condition.
- 3-46. Match the schematic symbols in Fig. 3-61 with their names. Some answers may be used more than once.

The Symbols for Prob. 3-46.

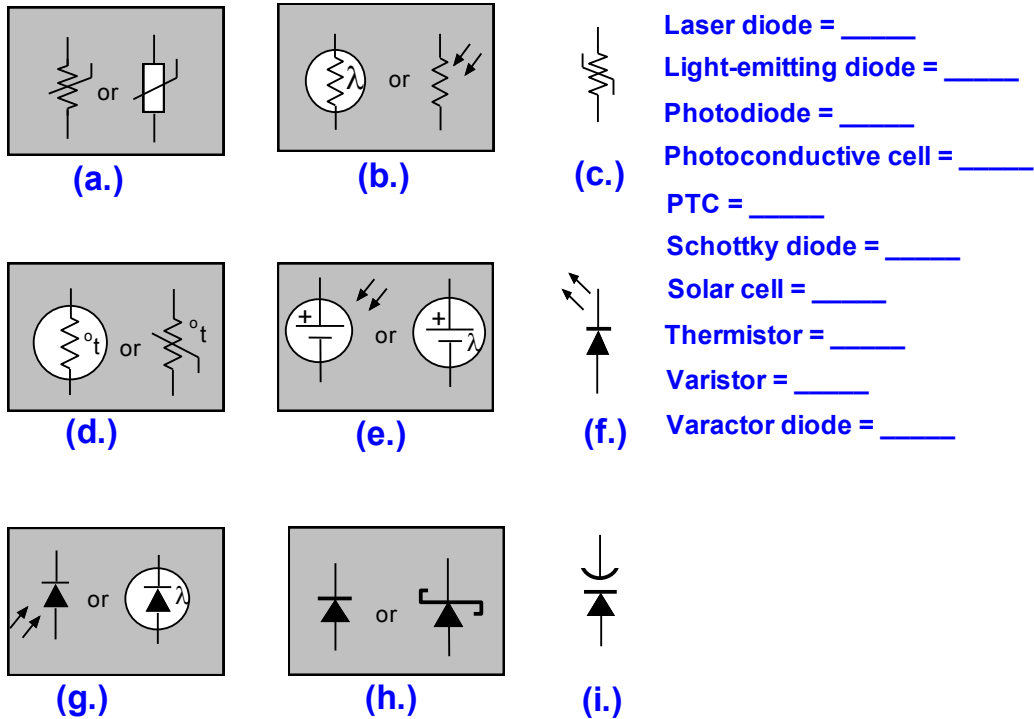


Figure 3-61.

EDA Problems

Section 3-2

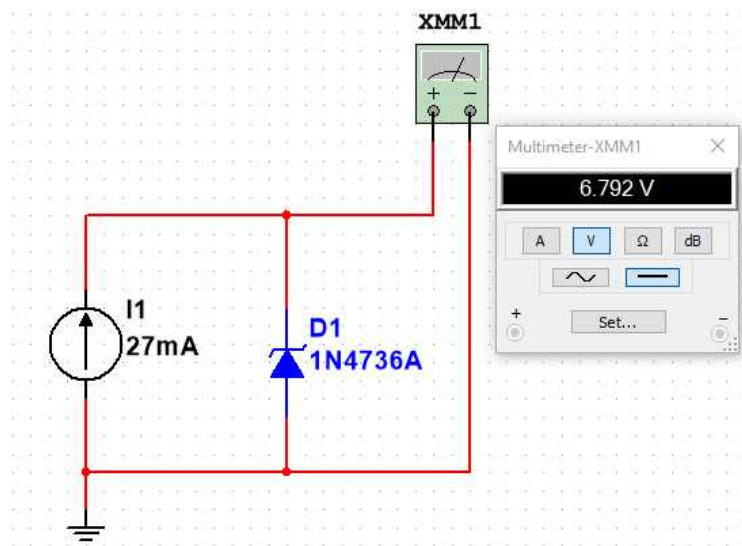
- 3-47. Repeat the analysis of the clamper circuit shown in Fig. 3-6 using Multisim but *reverse the diode*. Drag down an oscilloscope from the **Instruments** menu and connect it across R_L . Use the expanded oscilloscope display to observe the circuit's output. Obtain a hard copy of the output waveform.
- 3-48. Repeat the analysis of the clamper circuit shown in Fig. 3-6 using Multisim but increase the source voltage to 15 V peak (10.6 Vrms). Use the expanded oscilloscope display to observe the circuit's output. Obtain a hard copy of the output waveform.

Section 3-3

- 3-49. Develop the forward V - I characteristic of the 1N4148 diode at -65°C , 25°C , and at 125°C using Multisim. (Note the temperature range from -65°C to 125°C is the standard military temperature range for product specification.) Refer to Figs. 3-13 through 3-16. Obtain a hard copy of the V - I characteristic in each case.
- 3-50. Develop the forward V - I characteristic of the 1N4002 diode at -65°C , 25°C , and at 125°C using Multisim. Refer to Figs. 3-13 through 3-16. Obtain a hard copy of the V - I characteristic in each case.

Section 3-4

- 3-51. In Section 2-6 we examined zener and avalanche diodes and learned about their temperature coefficients. **Your challenge in Prob. 3-52 is to look at the temperature effects on these breakdown diodes.** Figure 3-62 shows a test circuit and a partial diode data sheet. We have an example of the setup for a 1N4736A zener diode. We are driving the zener with a constant-current source (set to the zener test current) and measuring the resultant zener voltage with a DMM. The DMM displays the zener voltage and is *not* at the nominal 6.8-V value. Perform a similar analysis for the 1N4741A zener diode. You should obtain a hard copy of the results.

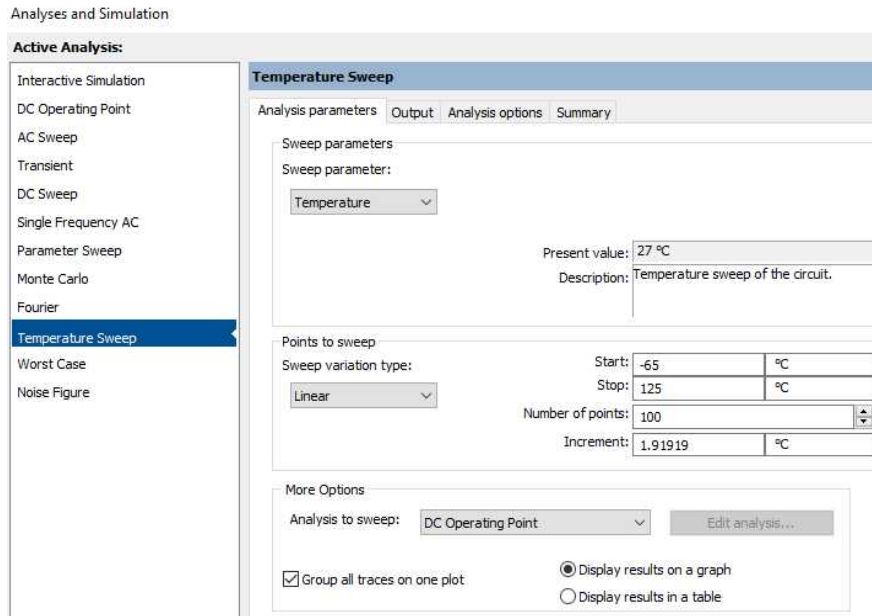


Electrical Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

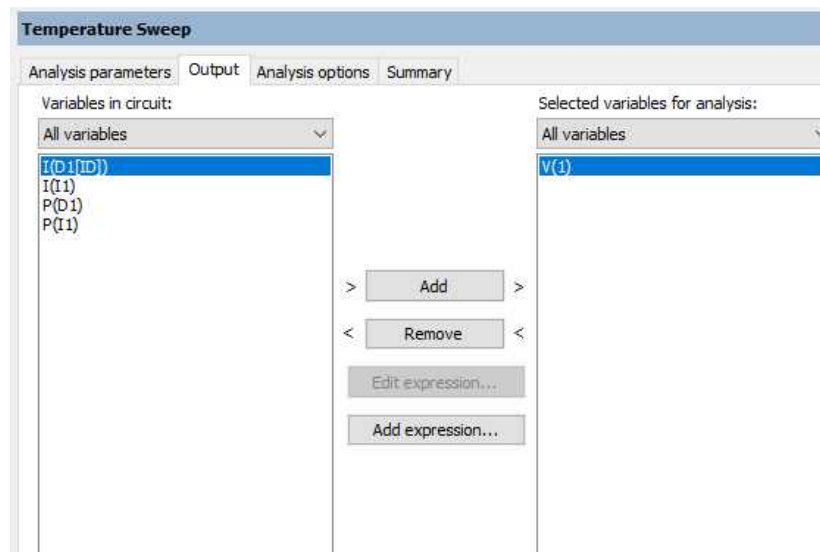
Device	V_Z (V) @ I_Z (Note 1)			Test Current I_Z (mA)	Max. Zener Impedance			Leakage Current		Non-Repetitive Peak Reverse Current I_{ZSM} (mA) (Note 2)
	Min.	Typ.	Max.		Z_Z @ I_Z (Ω)	Z_{ZK} @ I_{ZK} (Ω)	I_{ZK} (mA)	I_R (μA)	V_R (V)	
1N4728A	3.135	3.3	3.465	76	10	400	1	100	1	1380
1N4729A	3.42	3.6	3.78	69	10	400	1	100	1	1260
1N4730A	3.705	3.9	4.095	64	9	400	1	50	1	1190
1N4731A	4.085	4.3	4.515	58	9	400	1	10	1	1070
1N4732A	4.465	4.7	4.935	53	8	500	1	10	1	970
1N4733A	4.845	5.1	5.355	49	7	550	1	10	1	890
1N4734A	5.32	5.6	5.88	45	5	600	1	10	2	810
1N4735A	5.89	6.2	6.51	41	2	700	1	10	3	730
1N4736A	6.46	6.8	7.14	37	3.5	700	1	10	4	660
1N4737A	7.125	7.5	7.875	34	4	700	0.5	10	5	605
1N4738A	7.79	8.2	8.61	31	4.5	700	0.5	10	6	550
1N4739A	8.645	9.1	9.555	28	5	700	0.5	10	7	500
1N4740A	9.5	10	10.5	25	7	700	0.25	10	7.6	454
1N4741A	10.45	11	11.55	23	8	700	0.25	5	8.4	414
1N4742A	11.4	12	12.6	21	9	700	0.25	5	9.1	380

Figure 3-62.

- 3-52. You are to use Multisim to determine the effect of temperature on a 1N4741A zener diode and *obtain a plot* if the temperature runs through the standard military temperature range from -65°C to 125°C . The same circuit provided in 3-62 can be used to run a temperature sweep. Figure 3-63 provides guidance. Perform a **Temperature Sweep**. **Start** it from -65°C and **Stop** it at 125°C and use 100 data points. The sweep is **Linear** and sweeps the DC Operating Point. The **Output** is the voltage across the zener diode **V(1)**. The result for the 1N4736A is given in Fig. 3-64.



(a.)



(b.)

Figure 3-63.

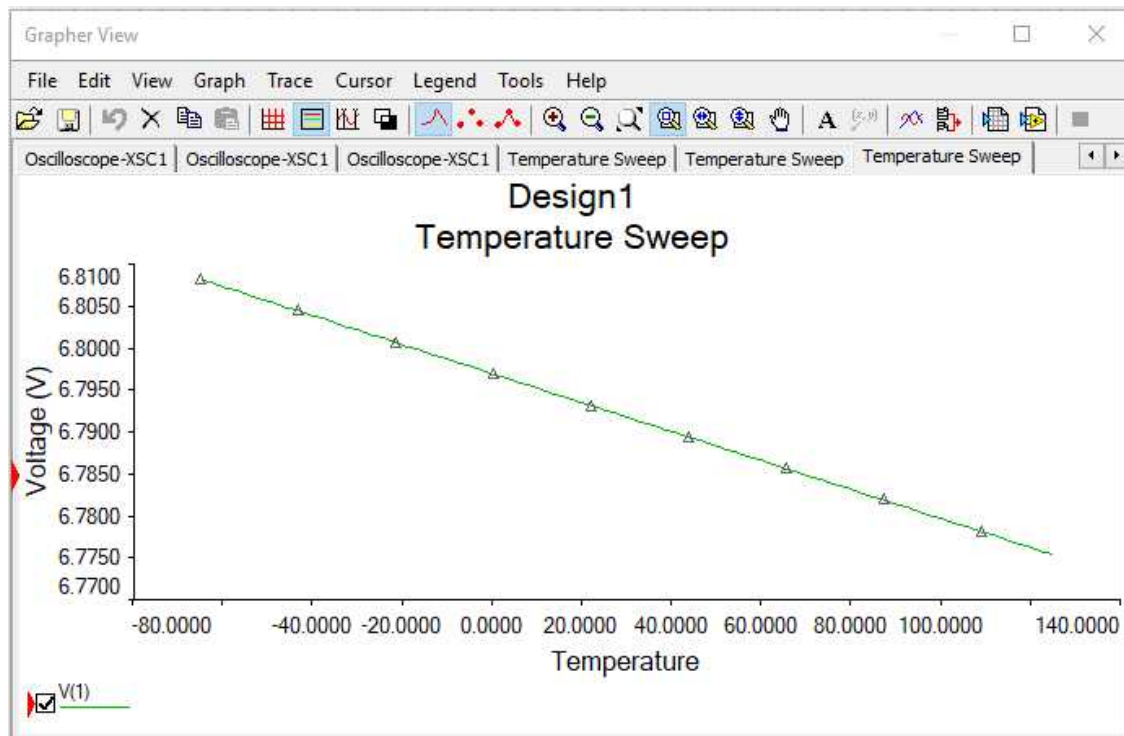


Figure 3-64.

Design Problems

- 3-53. The LED given in Fig. 3-65 is to have a forward current of 15 mA. Determine the required value for the current-limiting resistor R_1 . Use an internet search to select the nearest standard 5%-tolerance resistor value.
- 3-54. Repeat Prob. 3-53 if the DC supply voltage is increased to 15 V.

Circuit for Probs. 3-53 and 3-54

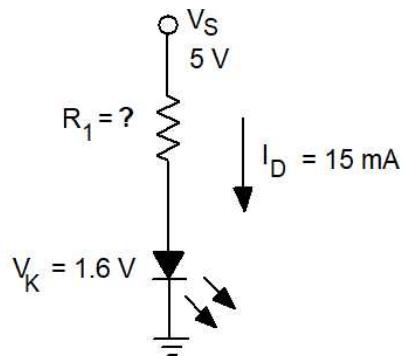


Figure 3-65.

Troubleshooting Problems

- 3-55. A common failure mode for an LED is for it to become a short circuit. What is the power dissipation in resistor R_I in Fig. 3-65 under *normal* operating conditions? Find the power dissipation in R_I if the LED becomes shorted.
- 3-56. Rectifier and Schottky diodes also tend to become short circuits when they fail catastrophically. Find the current through resistor R_I and its power dissipation if the Schottky diode in Fig. 3-60 becomes a short circuit.
- 3-57. A computer is being operated from a *surge-protected* AC power strip (refer to Fig. 3-66). After a thunderstorm, the circuit breaker keeps tripping. Both the computer and the printer are plugged into the power strip. Describe a troubleshooting procedure to isolate the faulty component. If the varistor is the problem, explain why it might have failed. The varistor is connected as depicted in Fig. 3-24 and is in the same position as the fuse.²⁹

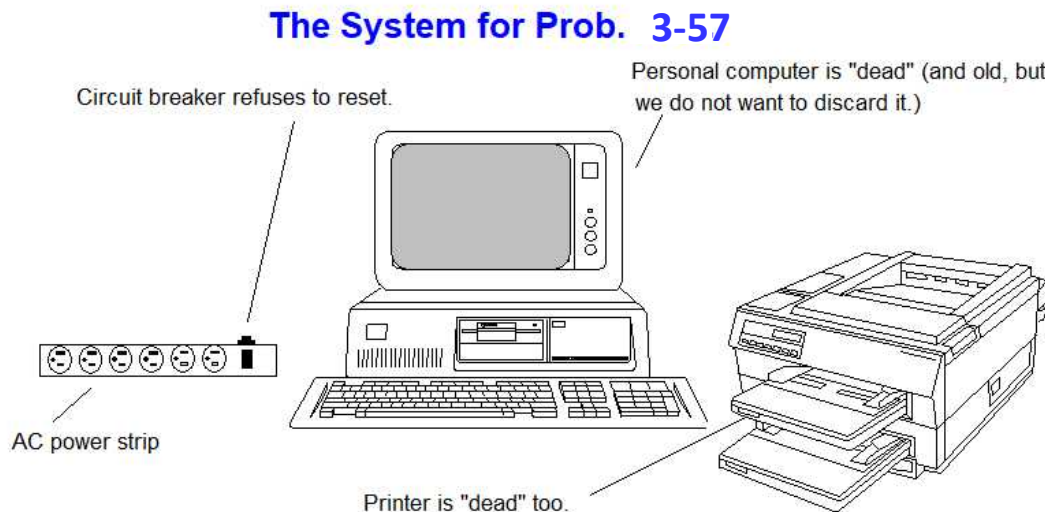


Figure 3-66.

²⁹ This system belongs to your great grandfather. You must fight the urge to say, "It wants to die – let it go." Solve the problem.

4

DC Power Supplies: Rectification and Filtering

Virtually all electronic systems require a source of DC power to operate properly. Consequently, DC power supplies are found in AC power-line-operated equipment like sound systems, desk-top computers, and laboratory bench-top equipment like DMMs (digital multimeters), oscilloscopes, function generators, and (of course) DC power supplies. There are two broad DC power supply classifications: linear and switching. In this chapter, we shall examine linear DC power supplies. The front end of a linear DC power supply includes its connection to the single-phase AC power distribution system, the transformer, rectifier, and filter. However, we shall also introduce an integrated circuit (IC) called a *three-terminal voltage regulator*. This easy-to-use device will permit us to construct a complete line-operated DC power supply. The specific topics covered in this chapter include:

- Linear Versus Switching DC Power Supplies
- The Load
- The Single-Phase AC Power Distribution System
- Average and RMS Values
- The Transformer
- The Half-Wave Rectifier
- Full-Wave Rectifiers Using a Center-Tapped Transformer
- Full-Wave Bridge Rectifiers
- Dual-Complementary Full-Wave Rectifiers
- Filter Capacitor Considerations
- Simple Capacitor Filter
- Ripple Factor
- Light-Loading Constraint
- Ripple Voltage Equation
- Rectifier Average and Peak Repetitive Currents
- Nonrepetitive Diode Surge Current
- Capacitor Ripple Current
- Transformer Secondary Current
- Diode Rectifier Specifications
- Three-Terminal IC Voltage Regulators

When we finish the chapter, *you* will be able to design a simple linear regulated DC power supply.

4-0 Study Objectives

After completing this chapter, you should be able to:

- Contrast the differences between linear and switching DC power supplies.
- Describe how the load drives the DC power supply requirements.
- Draw the fundamental block diagram of the line-operated linear DC power supply.
- Identify the hot, neutral, and ground connections in the single-phase AC power-distribution system and explain their functions.
- Explain the differences between average DC and AC root-mean-square (rms) values.
- Define the ideal transformer and calculate transformer voltage regulation.
- Analyze a half-wave rectifier circuit.
- Analyze full-wave rectifier circuits including the full-wave rectifier using a center-tapped transformer, the full-wave bridge rectifier, and the dual-complementary full-wave rectifier.
- Explain the role of the filter capacitor in the DC power supply.
- Analyze simple capacitor filter DC power supply circuits to determine the peak rectified voltage (V_{dc}), the peak-to-peak ripple voltage ($V_{r(p-p)}$) and its rms value ($V_{r(rms)}$), the average DC voltage (V_{DC}), and the minimum instantaneous DC voltage ($V_{dc(min)}$).
- Explain repetitive surge currents and their effect on the diode rectifiers and filter capacitors.
- Describe the application of the three-terminal integrated circuit (IC) voltage regulator and its features.
- Describe the basic approach to the design of a line-operated DC power supply.
- Interpret rectifier diode data sheets.

4-1 Linear Versus Switching DC Power Supplies

As mentioned previously, DC power supplies are available in either linear or switch-mode (also called switcher) designs. While both types supply DC power, the two methods used to produce this DC power are very different. Depending on the application, each type of power supply has advantages over the other one. Let us look at the differences between these two topologies as well as each design's respective advantages and disadvantages.

A linear power supply design applies the AC line voltage (e.g., 120 Vrms at a frequency of 60 Hz) to a power transformer to (usually) lower the voltage before being applied to the rectifier, filter and regulator circuitry [see Fig. 4-1]. The size and weight of a transformer is inversely proportional to the frequency of operation, at 60 Hz, this results in a larger, heavier DC power supply.

A switch-mode power supply [Fig. 4-2] converts the AC line power directly into a DC voltage *without* an input transformer, and this raw DC voltage is then converted into a *higher frequency* AC signal, which is used in the regulator circuit to produce the desired voltage and current.

This approach results in a much smaller, lighter transformer for raising or lowering the voltage than what would be necessary at an AC line frequency of 60 Hz.

These smaller transformers are also considerably more efficient than 60-Hz transformers. This means the losses are reduced. Do *not* let the block diagram of the switch-mode DC power supply in Fig. 4-2 intimidate you. We need to cover many more topics before we will be ready to make a detailed study.

Linear DC Power Supplies

Linear DC power supplies were the mainstay of AC-to-DC power conversion systems until the early 1980's. With the advancement of switching power supply technology, linear power supplies are less popular today but still find themselves indispensable in applications that require very low ripple and low electrical noise. A linear power supply typically uses a big transformer to drop voltage from AC line to much lower AC voltage, and then uses rectifier circuitry and filtering process to produce a very "clean" DC voltage. The filtered DC is then directed into the input of a voltage regulator, which can be a single integrated circuit.

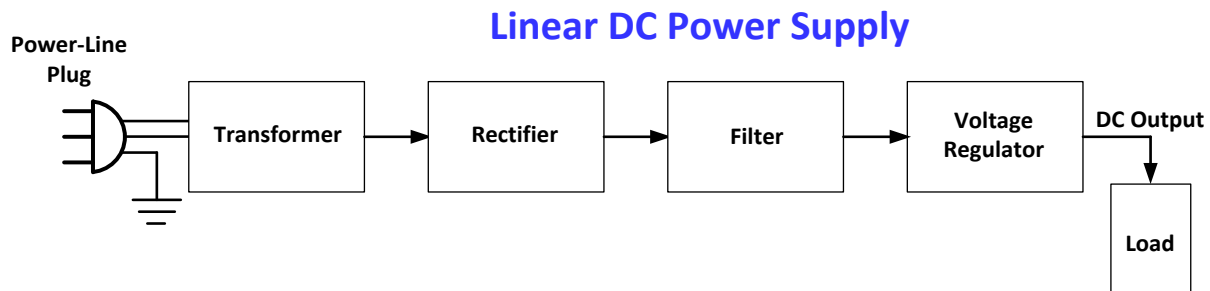


Figure 4-1.

Figure 4-1 provides the block diagram of a linear DC power supply. In this chapter we shall examine each of the functional blocks. Consider this discussion to be an overview, but the details will be provided throughout this chapter. The transformer usually reduces the sinusoidal power-line voltage. The rectifier distorts its sinewave input (with its average value of zero) to produce a pulsating waveform that has an average (DC) value. The filter smooths out the pulsating DC. The voltage regulator provides a constant DC voltage, reduces ripple, and provides protective functions.

Switching DC Power Supplies

Figure 4-2 shows the block diagram for a switching DC power supply³⁰. Switching DC power supplies were first introduced in the 1970's, today they are the most popular form of DC power supplies in the market due to their excellent power efficiency, light weight, minimal heatsinking requirements and exceptional overall performance.

³⁰ Important! *Figure 4-2 is included for comparison purposes only.* It also provides an indication of where our studies are headed ultimately, and not what we need to understand at this point.

A switching DC power supply (also known as switch-mode power supply) regulates the output voltage through a process called pulse width modulation (PWM). The PWM process generates some high-frequency electrical noise but enables the switching power supplies to be built with excellent power efficiency. A switching power supply can have exceptional load and (input AC power) line regulation.

Referring to Fig. 4-2, the input stage is an Electro-Magnetic Interference (EMI) filter. It prevents high-frequency noise from being placed on the power lines. The Rectifier stages use diodes and are discussed in this chapter. Active Power Factor Correction (PFC) adjusts the current drawn from the AC power line such that it is in phase with the voltage. The details of the design are covered in our later work.

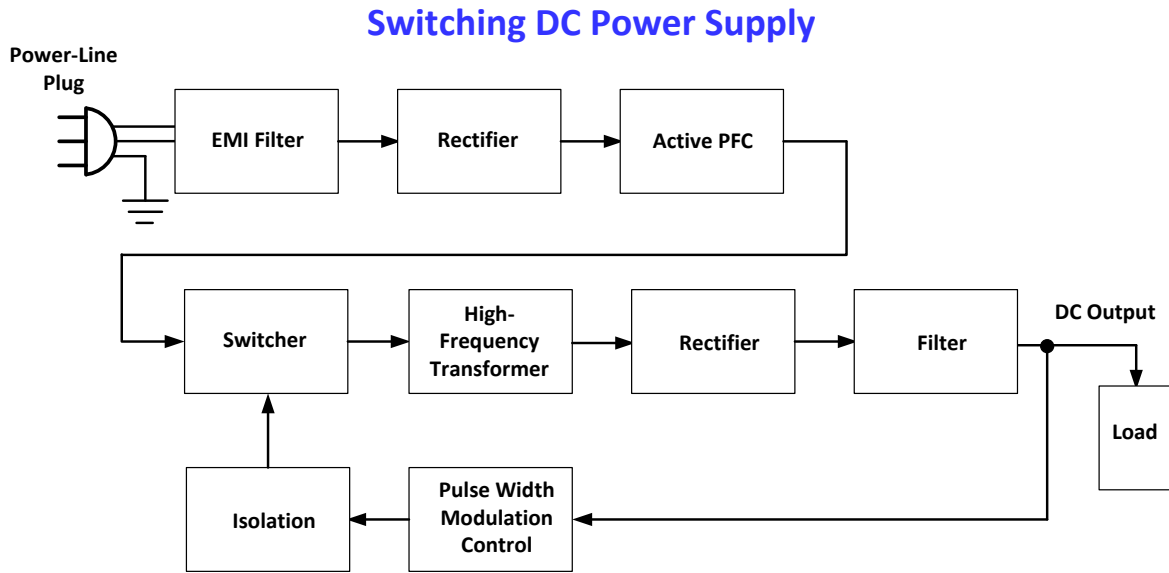


Figure 4-2.

4-2 The Load

Electronic equipment is designed to satisfy a purpose. Consider the desktop headphone amplifier illustrated in Fig. 4-3. In this instance, the consumer is provided with a small amplifier system to boost the amplitude of the audio signal monitored by a pair of headphones. The design also provides a Universal Serial Bus (USB) charging station. Each of these functional blocks includes electronic devices such as diodes, transistors, and integrated circuits. These devices require a DC power source to operate properly. (This will be explained completely in Chapter 5.) This is the purpose of the line-operated DC power supply. Because we have a low-power audio system a linear DC power supply is a good choice.

Since each of these blocks draws a current, the total load current (I_L) must be supplied by the DC power supply. Therefore, we arrive at Eq. 4-1 by Kirchhoff's Current Law (KCL).

$$I_L = I_1 + I_2 + I_3 + \bullet \bullet \bullet + I_{n-1} + I_n \quad (4-1)$$

When discussing and analyzing power supplies it is convenient to represent the load by its DC equivalent resistance (R_L). Hence, by Ohm's law we can state Eq. 4-2.

$$R_L = \frac{V_L}{I_L} \quad (4-2)$$

where V_L is the DC load voltage, I_L is DC load current, and R_L is the equivalent static (DC) load resistance. The reader should work through Example 4-1.

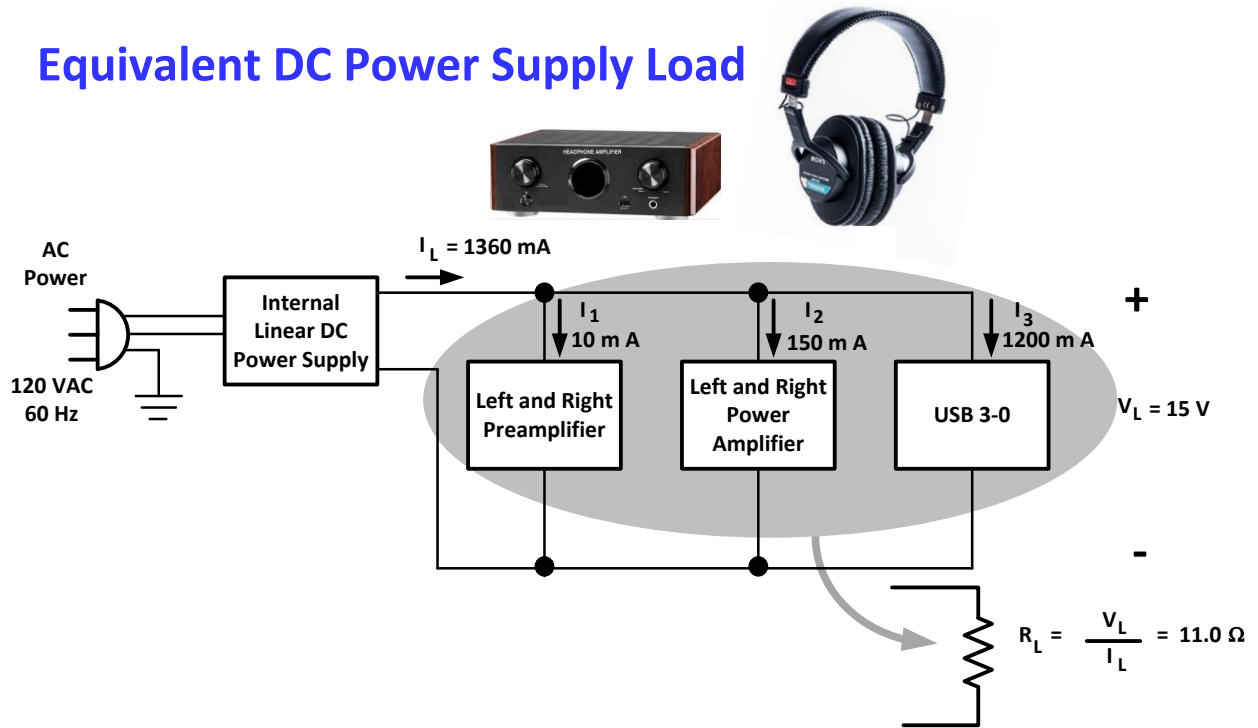


Figure 4-3. Headphone Amplifier DC Power Supply

Example 4-1. A headphone amplifier system is shown in Fig. 4-3. Determine the total load current (I_L), the equivalent load resistance (R_L), and the DC power (P_L) delivered to the load.

Solution: We apply Eq. 4-1 to determine the load current.

$$I_L = I_1 + I_2 + I_3 = 10 \text{ mA} + 150 \text{ mA} + 1200 \text{ mA} = 1360 \text{ mA}$$

Equation 4-2 is used to find the DC load resistance.

$$R_L = \frac{V_L}{I_L} = \frac{15 \text{ V}}{1.360 \text{ A}} = 11.0 \Omega$$

The DC power is calculated next.

$$P_L = V_L I_L = (15 \text{ V})(1.36 \text{ A}) = 20.4 \text{ W}$$

4-3 The Single-Phase AC Power Distribution System

Since a line-operated DC power supply must connect to the AC single-phase power distribution system, it is important that we understand how it is configured. ***Our safety as well as the safety of those who use the equipment we have designed and/or repaired depends on our knowledge.*** The important elements of the single-phase AC power distribution system have been illustrated in Fig. 4-4.

A standard duplex receptacle has been indicated. The AC input has been represented as a 115-Vrms, 60-Hz voltage source.³¹ (The line frequency could be 50 Hz in other installations outside of North America.) The National Electric Code (NEC) requires the neutral and earth ground connections be made at the service entrance. The normal AC load current flows through the hot wire and returns via the neutral wire. ***The ground conductor should not pass current unless a fault has occurred.***

The little slot on the duplex receptacle is the hot wire connection. The color code for the wire insulation has the hot wire black, the neutral wire white, and the ground wire green (or bare). *Expresso* can be used as a mnemonic aid. It's a hot, black, little drink, which helps us remember the *hot* wire is *black* and connects to the *little* slot. This is shown in Fig. 4-4.

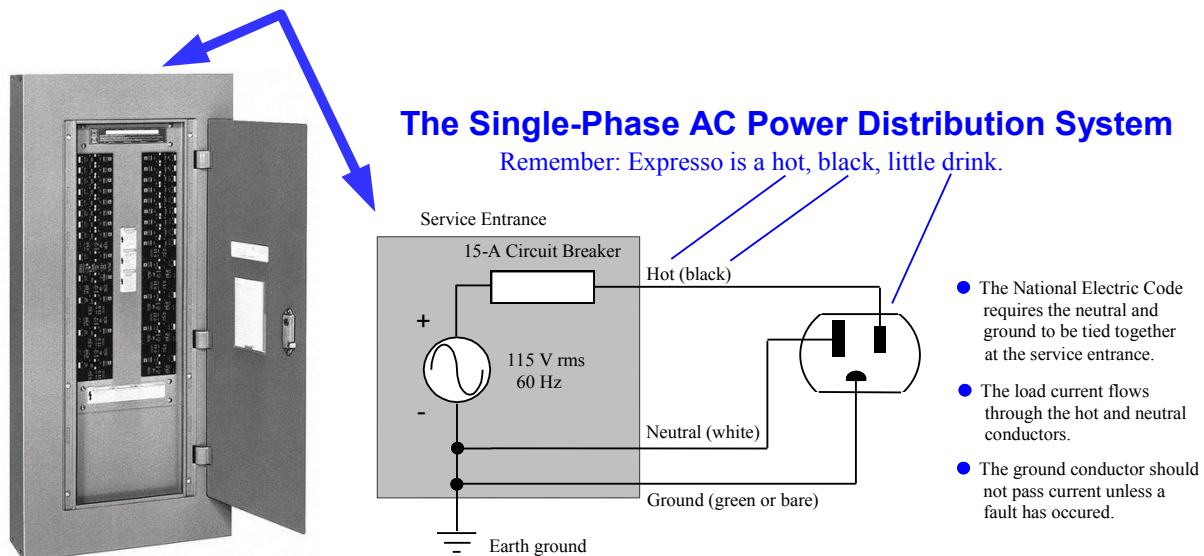


Figure 4-4.

Figure 4-5 shows how line-operated equipment should be connected to the power distribution system. The plug and receptacle connections have *not* been indicated in the figure. During normal operation, the AC load current flows through the hot and neutral wires. No current flows through the ground connection.

³¹ While you may be familiar with rms, it is reviewed in Section 4-4 and applied to the **nonsinusoidal** waveforms we encounter in the study of DC power supplies.

Normal Operation of the AC Power Distribution System

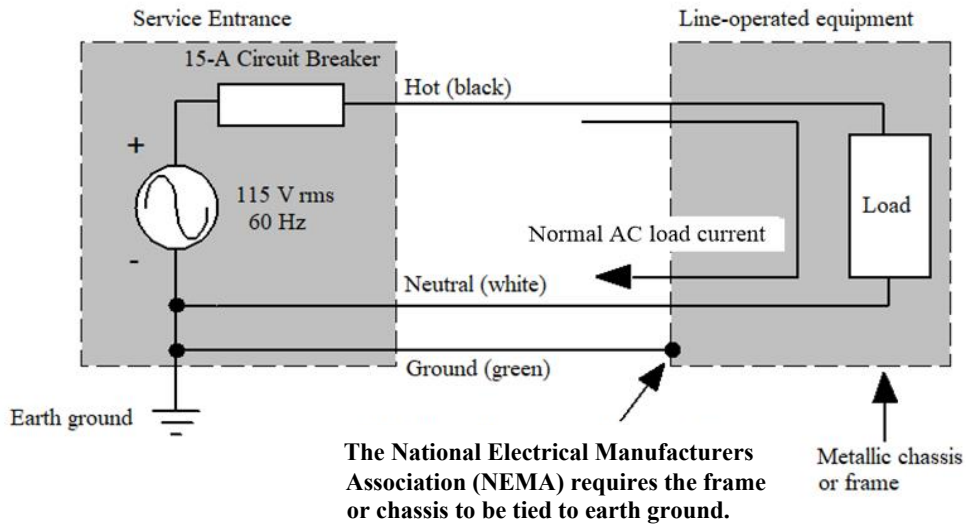


Figure 4-5.

A possible fault condition has been depicted in Fig. 4-6. The hot wire has contacted the metallic chassis. Without the ground connection, the metallic chassis could float up to 115 V rms. Obviously, a grounded person touching a 115-V chassis could be injured. However, because of the chassis ground connection, the hot wire will be shorted out. The large fault current will open the circuit breaker, which disconnects the faulty equipment. This prevents the chassis from being held at the 115-V potential.

If the chassis is double insulated, or nonconductive, the ground wire connection is *not* required. (A polarized plug is still used.) Electrical shock cannot occur. This approach is used for vacuum cleaners and many electric drills.

A Fault Condition

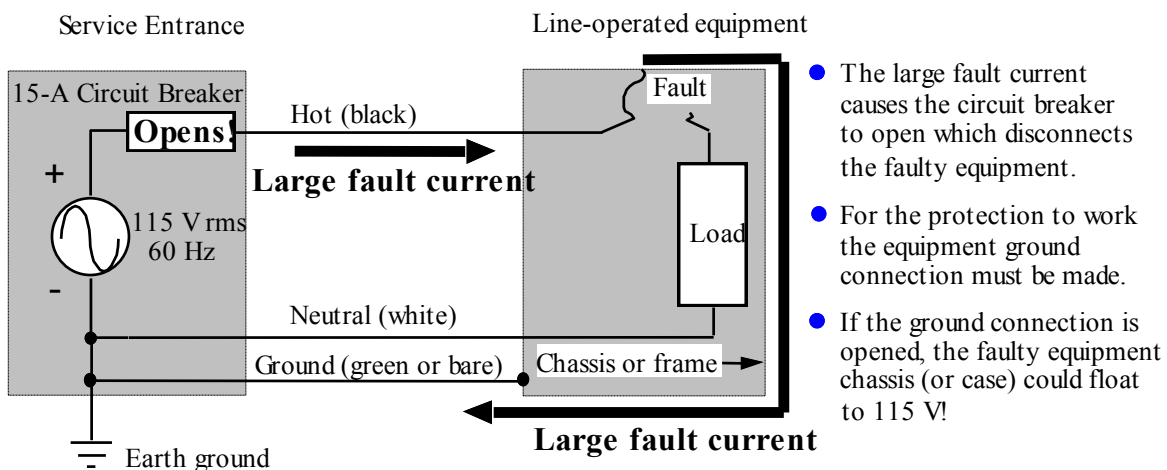


Figure 4-6.

4-4 Average and RMS Values

In your first circuits course, your studies most likely focused on DC problems. A second circuits course usually concentrates on AC circuit analysis. It is customary in the second course to define the basic sinusoidal values like peak, peak-to-peak, and rms values. Figure 4-7 provides a brief review. In Fig. 4-7(a) we are reminded DC flows in one direction only. Figure 4-7(b) indicates *pure* AC flows in one direction half of the time and then reverses its direction.

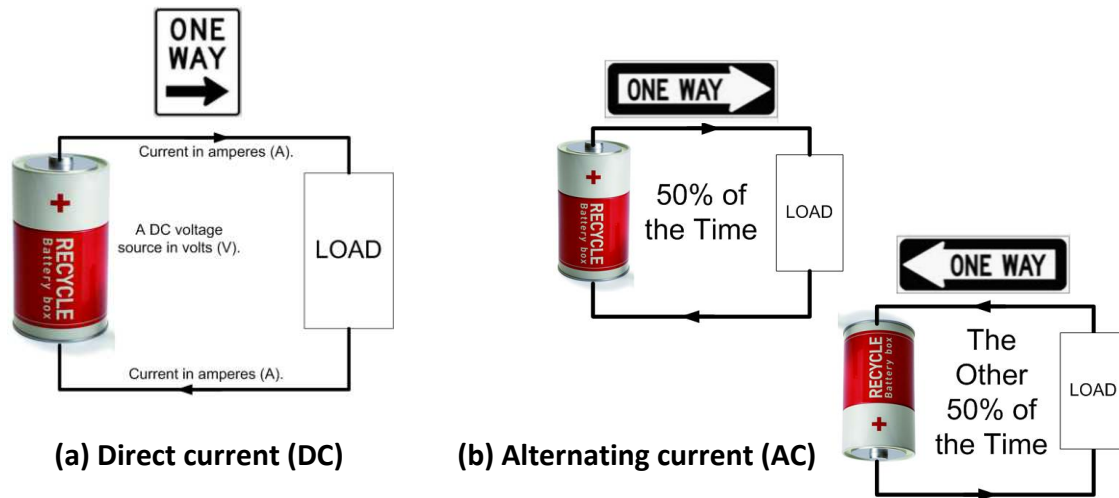


Figure 4-7.

Figure 4-7(c) illustrates a sine wave and the determination of its peak and peak-to-peak (p-p) values.

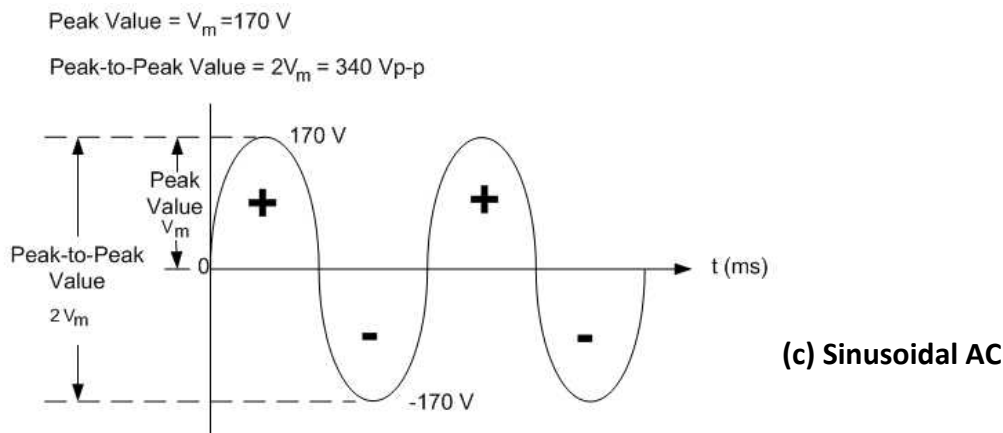


Figure 4-7 (continued).

Average Values

In Fig. 4-8(a) we see ***the average value of the sine wave is zero***. This means its average value is not a good way to describe it. Figure 4-8(b) shows the basic idea used to describe the root mean square (rms) value of a sine wave. ***The AC rms value produces the same power in a resistor as the same size DC. Power dissipation in a resistor results in a temperature rise. This means the rms value has the same effective value.***

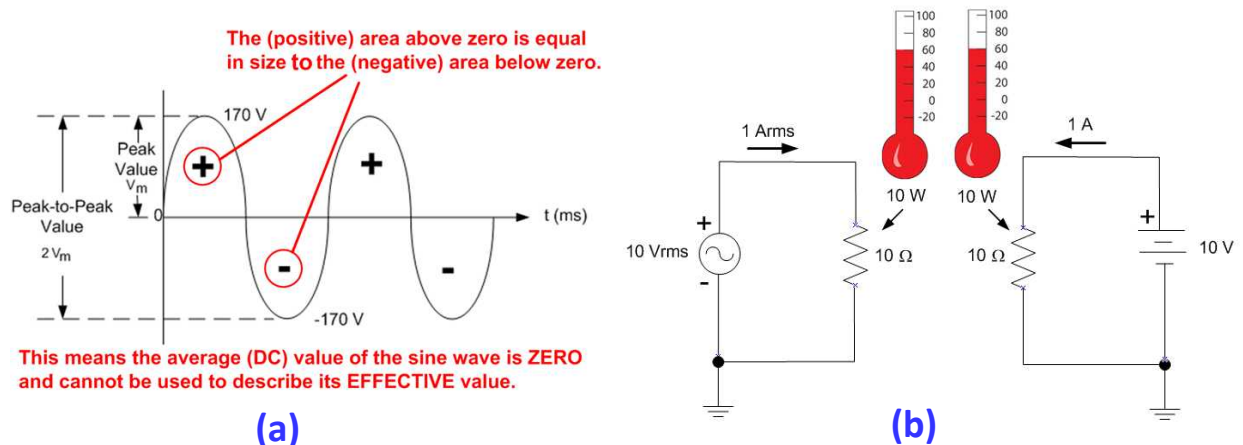


Figure 4-8.

The average value of a pure sine wave is given by Eq. 4-3.

$$V_{DC} = 0\text{ V} \quad (4-3)$$

The rms or effective value of sine wave can be determined by using Eq. 4-4.

$$V_{RMS} = \frac{V_m}{\sqrt{2}} \cong 0.707V_m \quad (4-4)$$

The reason for this review is that it will help us understand the various ***nonsinusoidal*** waveforms we encounter in the study of DC power supplies. For instance, in Fig. 4-9 we see the block diagram of a line-operated (linear) DC power supply and some typical waveforms. (We will see how these waveforms are produced as we work through Chapter 4.)

Linear DC Power Supply

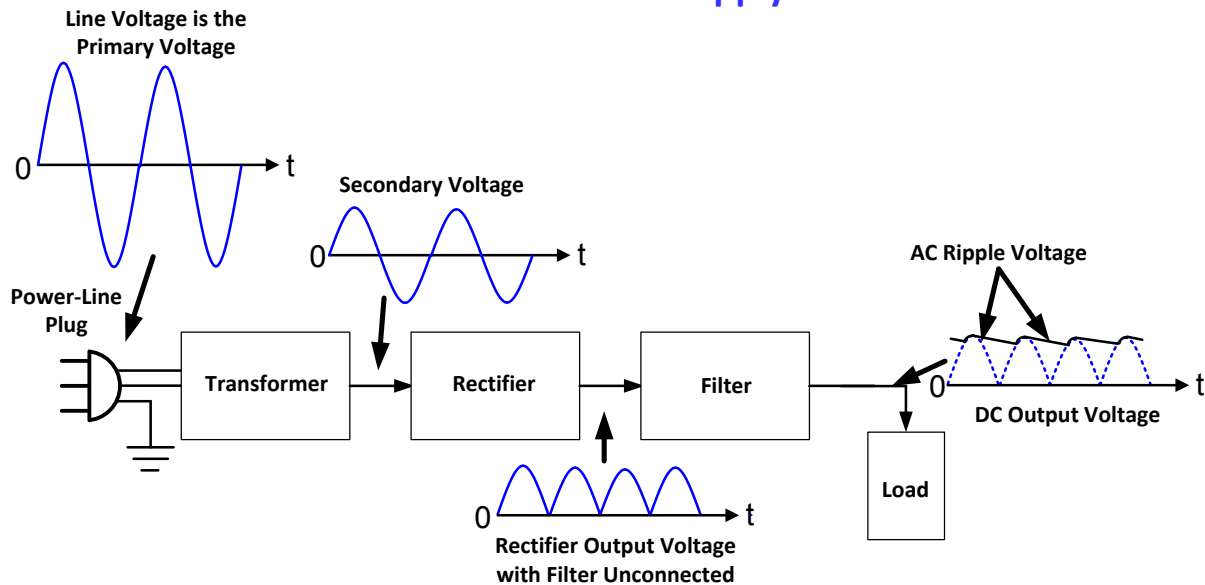


Figure 4-9.

Figure 4-9 shows the large sinusoidal voltage delivered by the power line plug to the primary winding of the transformer³². The transformer is evidently a step-down unit since the secondary voltage is sinusoidal with a smaller peak amplitude. Notice the output of the rectifier is always above the zero axis. Since its polarity is always positive it has a positive average. It is described as **pulsating DC**. (In general, that will be the waveform that will be developed if the output of the rectifier is *not* connected to the input of the filter.) The output of the filter is connected to the load. The DC output voltage will again have a positive average value. *The pulsating DC is shown in dashed lines for reference only.* The triangular-like variation is called the **(AC) ripple voltage**.

We have familiarity with sine waves, we know their average value is zero, and we know how find their rms or effective values by applying Eq. 4-4. To describe sinusoidal and nonsinusoidal waveforms we can refer to their instantaneous values [i.e., $v(t)$] or we can lump their characteristics into average and/or rms values. In the study of DC power supplies, as well as many other electronic circuits, the average and rms descriptions are extremely useful.

Let's define the DC or average value of a periodic waveform.

The DC or average value of a periodic waveform is given by the algebraic sum of its (positive) area above zero and its (negative) area below zero, divided by the period of the waveform.

This is summarized by Eq. 4-5.

$$V_{DC} = \frac{\text{Area}}{T}$$

(4-5)

³² Transformers are discussed in Section 4-5.

V_{DC} is the DC average value of a periodic voltage waveform. *Area* is the algebraic sum of the area above and below zero for one cycle and is divided by the period (T), which is the time for one cycle.

In Fig. 4-9 we indicated the filter's output has an AC ripple. Exactly how and why this occurs will be explained later. For now, we turn to Fig. 4-10(a). The period (T) of the pulsating DC is 8.33 ms. (This will be explained thoroughly in Section 4-7). The ripple waveform has been expanded to view it more clearly. We also see a triangular approximation of the ripple waveform.³³

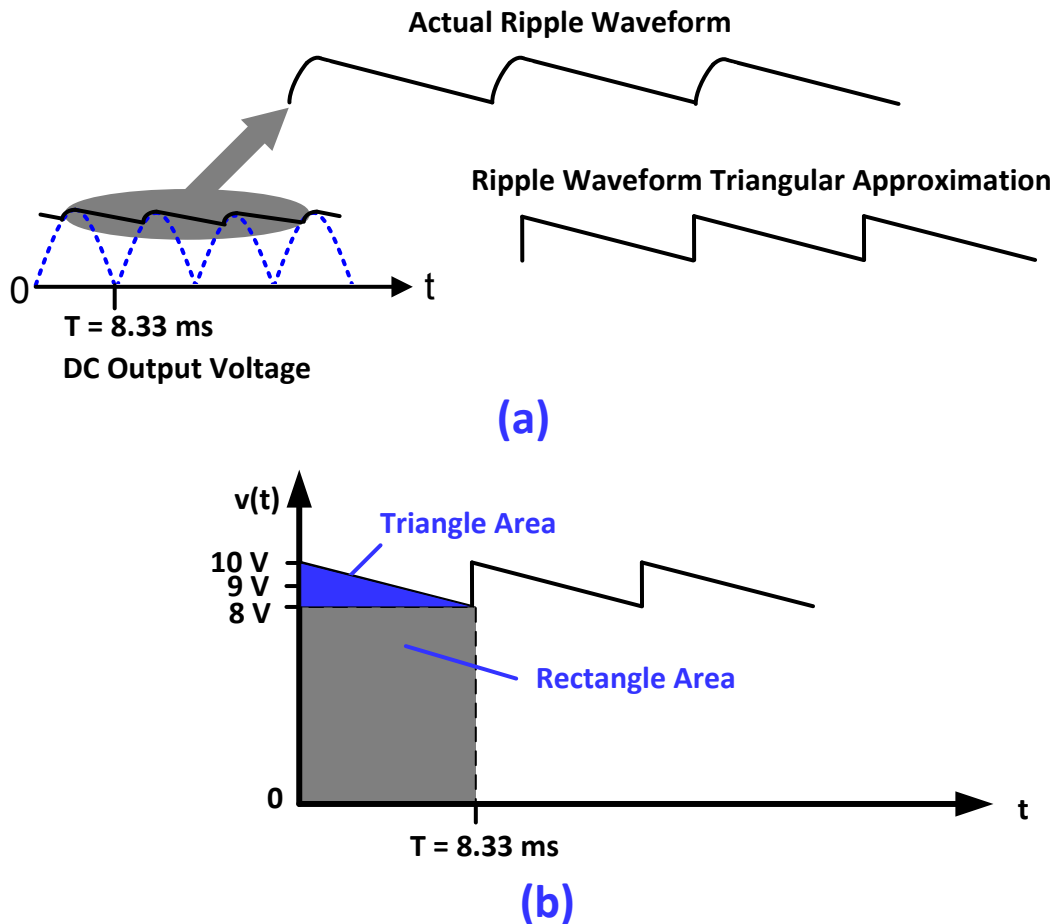


Figure 4-10.

In Fig. 4-10(b) we see the period is also 8.33 ms. Compare Fig. 4-10(a) with Fig. 4-10(b) and remember the period is taken between any two successive like points. Let's see how to determine the DC average value of the triangular waveform when it rides on a DC level as shown in Fig. 4-10(b). Consider Example 4-2.

³³ The triangular approximation simplifies analysis greatly. Consequently, its use is widely accepted.

Example 4-2. Find the DC value of the triangular waveform riding on a DC level as shown in Fig. 4-10(b).

Solution: In Fig. 4-10(b) we identify the period (T) to be 8.33 ms. The area under one cycle can be found easily by finding the area of the rectangle and adding it to the area of the triangle. Hence,

$$\text{rectangle area} = \text{base} \times \text{height} = (8.33 \text{ ms})(8 \text{ V}) = 66.64 \text{ mV} \cdot \text{s}$$

$$\text{triangle area} = \frac{1}{2} \times \text{base} \times \text{height} = \frac{1}{2} (8.33 \text{ ms})(2 \text{ V}) = 8.33 \text{ mV} \cdot \text{s}$$

$$\text{area} = \text{rectangle area} + \text{triangle area} = 66.64 \text{ mV} \cdot \text{s} + 8.33 \text{ mV} \cdot \text{s} = 74.97 \text{ mV} \cdot \text{s}$$

The DC value is given by applying Eq. 4-5.

$$V_{DC} = \frac{\text{area}}{T} = \frac{74.97 \text{ mV} \cdot \text{s}}{8.33 \text{ ms}} = 9 \text{ V}$$

The average DC value (V_{DC}) of the total waveform in Fig. 4-10(b) is 9 V. Figure 4-11(a) demonstrates the DC value runs through the triangular waveform such that area above it is equal to the area below it. If the waveform is drawn as shown in Fig. 4-11(b), it is clear it is an AC waveform. *Again, since a pure AC waveform (like the sine wave and triangle wave) has an average value of zero, it contributes nothing to the overall average of the total waveform* like Fig. 4-10(b).

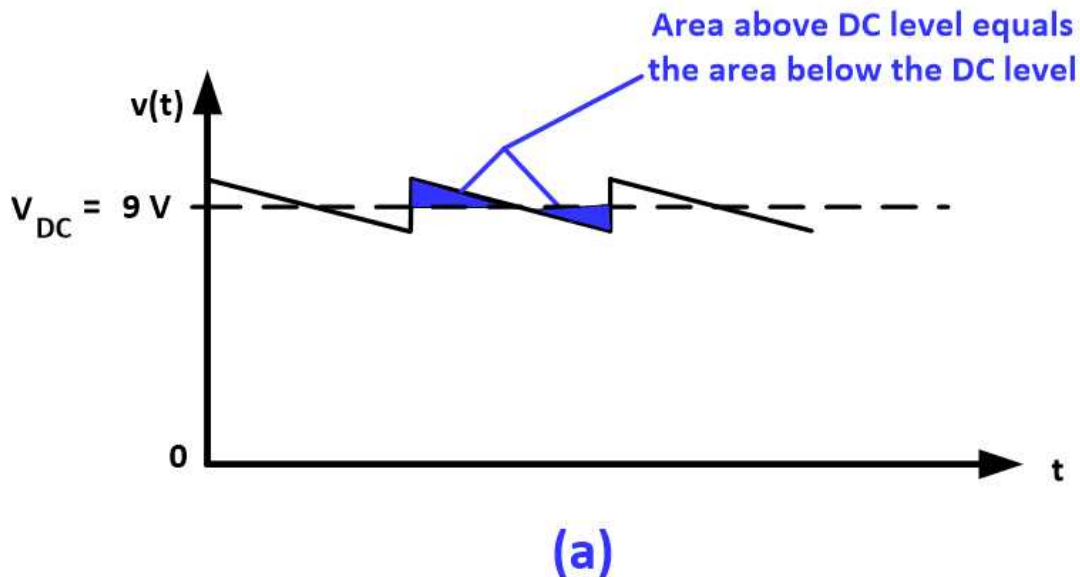


Figure 4-11.

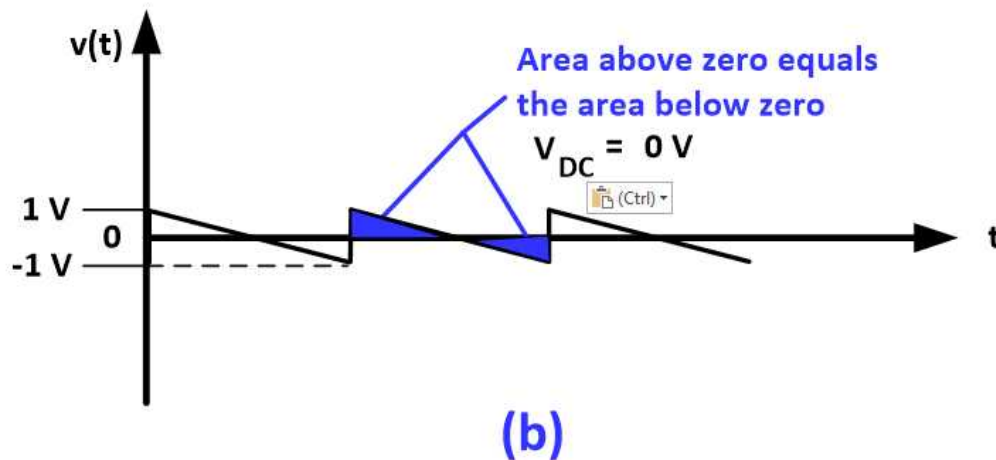


Figure 4-11 (continued).

The triangle wave zero reference in Fig. 4-11(b) is obtained by subtracting the DC value of 9 V from each of the three voltage values indicated in Fig. 4-10(a).

$$\begin{aligned} 10 \text{ V} - 9 \text{ V} &= 1 \text{ V} \\ 9 \text{ V} - 9 \text{ V} &= 0 \text{ V} \\ 8 \text{ V} - 9 \text{ V} &= -1 \text{ V} \end{aligned}$$

The average values of square, rectangular, and triangle waves are all relatively easy to find. That is because we have simple formulas for finding their areas. However, for other waveforms (e.g., the sinewave) we turn to **integral calculus**. Very simply, integral calculus is used arrive at the *equations* for finding the areas under waveforms. To familiarize the student with calculus notation, we provide Eq. 4-6.

$$\text{area} = \int_0^T v(t) dt \quad (4-6)$$

Where $\int$ = mathematical notation used to denote integration

0 and T = the limits of the integration

$v(t)$ = the (voltage) function to be integrated

dt = indicates the integration is with respect to time

By using Eq. 4-5 and substituting in Eq. 4-6, we obtain the calculus definition of V_{DC} .

$$V_{DC} = \frac{\text{area}}{T} = \frac{1}{T} \text{area} = \frac{1}{T} \int_0^T v(t) dt$$

$$V_{DC} = \frac{1}{T} \int_0^T v(t) dt \quad (4-7)$$

In general, we shall *not* use Eq. 4-7 to any large extent. If you are studying calculus, you may want to exercise it here.

In Fig. 4-12 we see the graph of a DC level. Since this voltage is constant, its DC average value for all time is 15 V. Applying either Eq. 4-5 or Eq. 4-7 will produce the same answer of 15 V. As we have seen, both the sine and the triangle (AC) waveforms have an average value of 0 V [see Fig. 4-8(a) and Fig. 4-11(b)]. If these waveforms ride on a DC level, such as 15 V, they will contribute *nothing* to the overall DC average. Consequently, the average value of the total waveform remains 15 V.

Total Waveform has an AC Ripple Riding on a DC Level OR is Varying DC

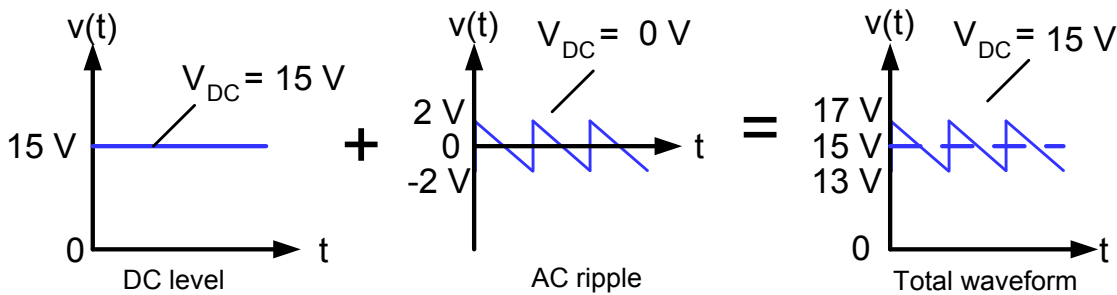


Figure 4-12.

As can be observed in Fig. 4-12, the total waveform can be described in two equal ways. We have an AC waveform riding on a DC level, or we have varying DC. For our purposes, we shall use the former description more often.

In Fig. 4-13 we see blocks that represent half- and full-wave rectifiers. Their input and output waveforms are indicated. The nonsinusoidal (pulsating DC) waveforms require the use of Eq. 4-7 to determine their DC values. The results are provided by Eqs. 4-8 and 4-9. Equation 4-8 yields the average value (V_{DC}) of the **half-wave rectifier**. V_{dcm} is the **peak value of the rectified waveform** in Fig. 4-13(a).

$$V_{DC} = \frac{V_{dcm}}{\pi} \cong 0.318V_{dcm} \quad (4-8)$$

Equation 4-9 gives the average value (V_{DC}) of the **full-wave rectifier**. Again, V_{dcm} is the peak value of the rectified waveform. The DC value of the full wave rectified waveform is twice that of the half-wave rectifier. This should make sense since we have twice as many pulses, we have twice the area, and that means twice the DC average value.

$$V_{DC} = 2 \frac{V_{dcm}}{\pi} \cong 0.637 V_{dcm} \quad (4-9)$$

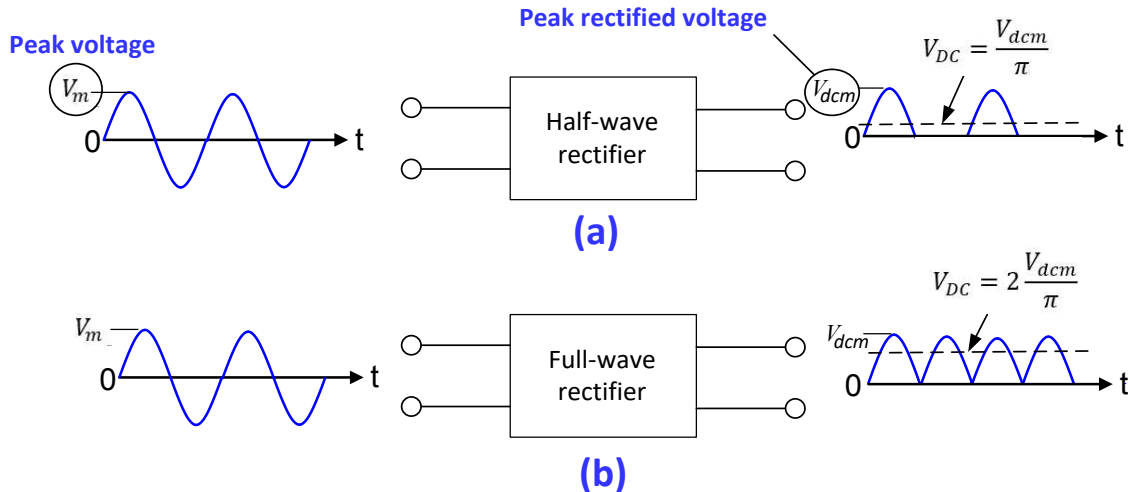


Figure 4-13.

With a little thought we can see that *rectifiers convert sine waves with an average value of zero into waveforms that have an average value. This is the sole function of rectifiers in a line-operated DC power supply.*

RMS Values

As mentioned previously, the root-mean-square (rms) or effective value is a useful way to characterize an AC waveform. Let us repeat its definition.

The rms or effective value of an AC waveform is equivalent to DC as far as power dissipated in a resistor is concerned.

To determine the rms value of *any* periodic AC (voltage or current) waveform, we may follow the procedure below.

1. Square the amplitude of the waveform.
2. Find the total area under the squared waveform.
3. Divide by the period.
4. Take the square root of the result.

Steps 2 and 3 produce an average value. *Another term for average is mean.* Consequently, the procedure provides us with the square root of the *mean* of the *squared* value or its rms value. The procedure is summarized by Eq. 4-10. Although voltage is indicated, *the same basic equation applies equally well for finding rms current.*

$$V_{rms} = \sqrt{\frac{(\text{area under the waveform})^2}{T}} \quad (4-10)$$

Let's find the rms value of the AC square wave indicated in Fig. 4-14(a). We note the positive area is the same size as the negative area, which means its DC value is zero. We begin the four-step procedure. In accordance with **step one**, the amplitude is squared and that provides the result shown in Fig. 4-17(b). Squaring the negative half cycle provides a positive result. **Step two** has us finding the resultant area of one cycle. Figure 4-17(b) shows the area is $V_m^2 T$.

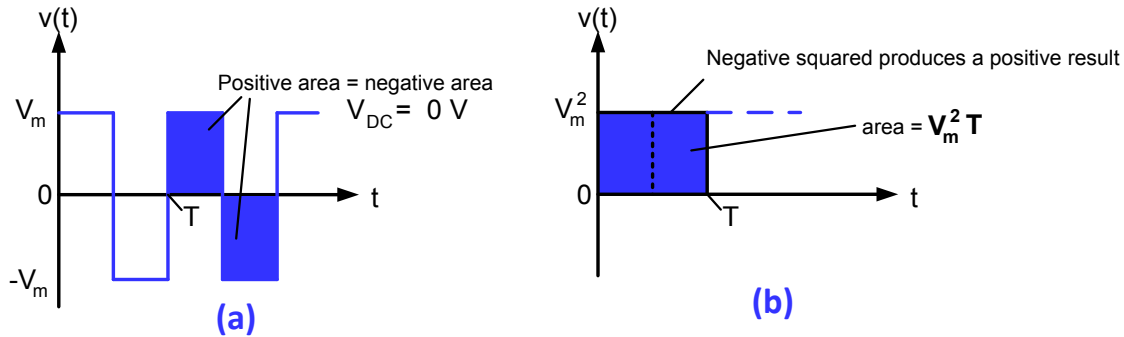


Figure 4-14.

We continue the procedure by finding the mean (or average) value (**step 3**).

$$\text{mean} = \frac{\text{area}}{T} = \frac{V_m^2 T}{T} = V_m^2$$

Step four requires that we take the square root.

$$V_{rms} = \sqrt{V_m^2} = V_m$$

Thus, we see ***the rms value of the AC square wave is equal to its peak value***. In general, finding the rms values of square and rectangular waves is straight forward. The is true because their squares produce rectangles and we know how to find the area of a rectangle (base X height). All other waveforms require the use of integral calculus. The calculus definition of the rms value is given by Eq. 4-11.

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt} \quad (4-11)$$

Where $\int$ = mathematical notation used to denote integration

0 and T = the limits of the integration

$v^2(t)$ = the squared (voltage) function to be integrated

dt = indicates the integration is with respect to time

Equation 4-11 looks very formidable. However, the goal here is to merely recognize it and understand it directs us to perform the same four steps detailed previously.

A key point to remember is **the rms or DC value of a DC or AC waveform depends upon its shape**. To illustrate this several waveforms are provided in Fig. 4-15 along with the equations for their DC and rms values.

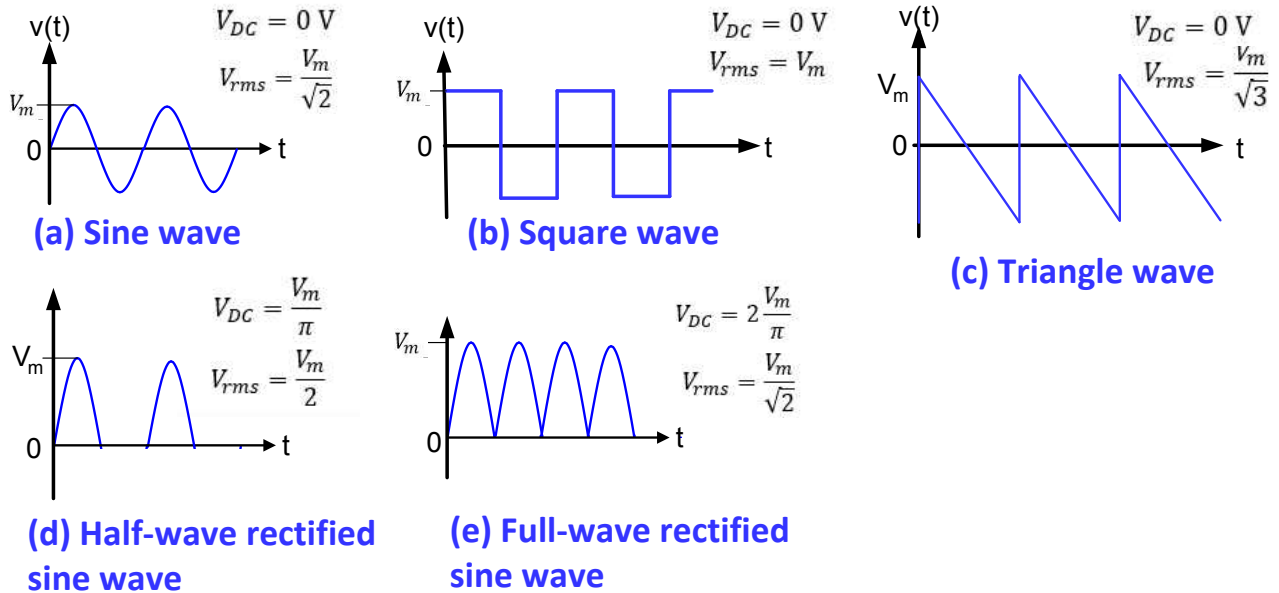


Figure 4-15.

Example 4-3. A triangle wave like the one shown in Fig. 4-15(c) has a peak value of 2 V. Find its rms value.

Solution: The equation used to determine the rms value is given in Fig. 4-15(c).

$$V_{rms} = \frac{V_m}{\sqrt{3}} = \frac{2 \text{ V}}{1.732} = 1.155 \text{ V}$$

4-5 The Transformer

Most line-operated linear DC power supplies will use a transformer at the front end where it connects to the AC power line. Typical transformers are shown in Fig. 4-16. Some transformers are designed to be mounted on a metallic chassis, while others can be mounted on printed circuit boards as through-hole components. Surface-mount components can be mounted on the top or the bottom of a printed circuit board. Toroidal transformers are very efficient and can operate at higher frequencies.



(a.) Chassis-mount



(b.) Through-hole printed circuit board mount



(c.) Surface Mount Technology (SMT)



(d.) Toroidal

Figure 4-16.

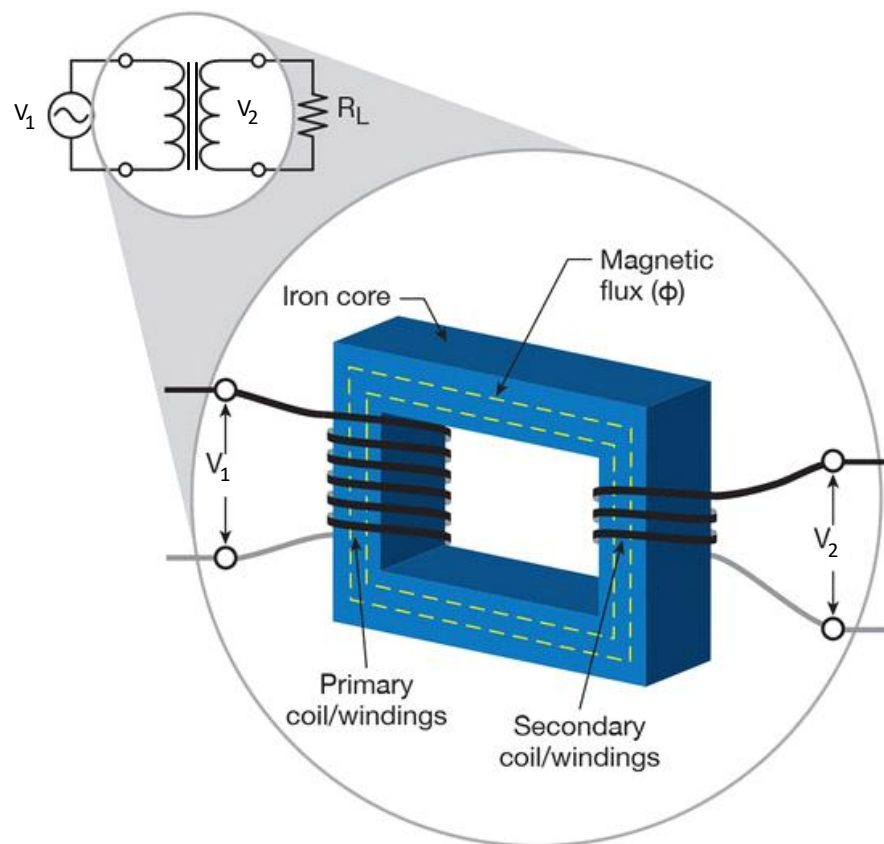


Figure 4-17.

A laminated iron core is used to improve the magnetic coupling between the primary and secondary windings. The structure shown in Fig. 4-17 is *conceptual*. In an actual transformer, the core design can have three parallel magnetic paths and the windings are usually wound on top of one another.

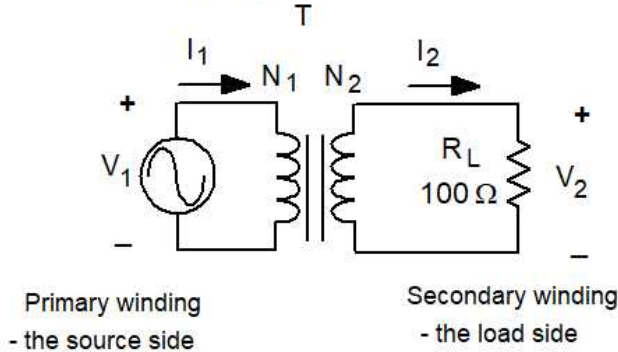
The transformer is typically incorporated to step down the AC line voltage and provide isolation from the power-line ground. The relationships between the excited (primary) side and the load (secondary) side are summarized in Fig. 4-18. Recall that when current flows through a wire, a magnetic field (Greek letter phi ϕ) is developed around the wire. The strength of the magnetic field is directly proportional to the magnitude of the current. The direction of the magnetic field depends on the direction of the current. Reversing the current direction will therefore reverse the direction of the magnetic field. Consequently, the sinusoidal AC voltage (V_1) applied to the primary winding (a coil) creates a sinusoidal magnetic field.

The changing magnetic field produced in the primary is used to induce a sinusoidal voltage in the secondary winding. No direct electrical connection exists between the primary side and the secondary side. This means the secondary is electrically isolated from the primary side. A transformer may be used to *step up* the primary voltage ($N_2 > N_1$), *step down* the primary voltage ($N_2 < N_1$), or simply provide isolation ($N_2 = N_1$). *Isolation transformers* are usually employed to isolate electronic instruments (typically oscilloscopes) from the power-line ground. ***Caution should be used when working with isolated instruments since their ground return is disabled. This can permit the case of an isolated instrument to rise to a dangerously large potential.***³⁴ Some transformers include an internal *electrostatic shield* to reduce the capacitive coupling between the primary and secondary windings. This is done to minimize any high-frequency, power-line noise from reaching the secondary winding(s).

³⁴ An unsuspecting (grounded) engineer or technician can have a really bad day if they touch the case. In fact, there was an incident at an unmentionable company where an unnamed mechanical engineer leaned against an isolated oscilloscope the instant an electrical engineer depressed a pushbutton to develop a series of 1000-volt pulses. The formerly friendly mechanical engineer was hurled into a nearby wall. To this day, the mechanical engineer has little use for electrical engineers. The electrical engineer was so remorseful he lost much of his hair and decided to go into management. True story.

The Ideal Transformer Relationships

- The secondary is coupled magnetically to the primary, but isolated electrically.
- Perfect coupling and no losses are assumed.



- T is the reference designator used for transformers.
- N_1 refers to the number of turns in the primary winding.
- V_1 represents the primary (rms) AC voltage and I_1 is the rms current.
- N_2 refers to the number of turns in the secondary winding.
- V_2 represents the secondary (rms) AC voltage and I_2 is the rms current.
- The ideal transformer voltage and current relationships are:

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} = \frac{I_1}{I_2}$$

Figure 4-18.

The *ideal* relationship between the rms values of the primary and secondary AC voltages is given by the turns ratio as shown in Fig. 4-18 and defined by Eq. 4-12.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} \quad (4-12)$$

This voltage relationship assumes perfect magnetic coupling exists between the primary and secondary windings. (In fact, the two vertical lines shown in the transformer schematic symbol represent the laminated iron core used to contain the magnetic flux to maximize the magnetic coupling.) The ideal transformer is also assumed to have *no energy losses*. ***This means all the power delivered to the transformer's primary is assumed to be transferred through the transformer to the load connected across the transformer's secondary.*** The power assumption leads us to the current relationship given by Eq. 4-13.

$$P_2 = P_1$$

$$V_2 I_2 = V_1 I_1$$

We solve for the voltage and current ratios to obtain Eq. 4-13

$$\frac{V_2}{V_1} = \frac{I_1}{I_2} \quad (4-13)$$

If we include the turns ratio, the entire ideal transformer voltage and current relationships are given by Eq. 4-14.

$$\frac{V_2}{V_1} = \frac{I_1}{I_2} = \frac{N_2}{N_1} \quad (4-14)$$

V_1 is the primary voltage, V_2 is the secondary voltage, I_1 is the primary current, I_2 is the secondary current, N_1 is the number of primary turns, and N_2 is the number of secondary turns.

Equivalently, the secondary acts like a voltage source to the load. The secondary current is determined by the size of the load resistance. The current, which flows through the primary, is dictated by the power delivered to the load resistance. The power delivered to the primary is equal to the load power (ideally).

Example 4-4. A step-down transformer is used in the circuit provided in Fig. 4-18. The primary voltage is 115 V rms while the secondary is rated at 12.6 V rms. Determine the transformer turns ratio (N_1/N_2). Calculate the resulting secondary current I_2 , and the corresponding primary current I_1 . Find the power delivered to the primary and the power absorbed by the load.

Solution: We apply Eq. 4-14 to determine the turns ratio.

$$\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{115 \text{ V}}{12.6 \text{ V}} = 9.126$$

This result means if we have 1000 turns on the secondary, the primary contains 9,126 turns. (The actual number of turns used by the manufacturer is not a big concern at this point.)

The secondary acts like an AC voltage source to the load. We find the secondary current by using Ohm's law.

$$I_2 = \frac{V_2}{R_L} = \frac{12.6 \text{ V}}{100 \Omega} = 126 \text{ mA rms}$$

We use Eq. 4-14 and our turns ratio calculation to find the primary current.

$$I_1 = \frac{N_2}{N_1} I_2 = \frac{V_2}{V_1} I_2 = \frac{12.6 \text{ V}}{115 \text{ V}} (126 \text{ mA}) = 13.8 \text{ mA rms}$$

The power delivered to the primary is equal to the power absorbed by the load. (P_{in} is P_1 while P_{out} is P_2 .)

$$P_{in} = V_1 I_1 = (115 \text{ V})(13.8 \text{ mA rms}) = 1.59 \text{ W}$$

Transformer Voltage Regulation

Transformer manufacturers will typically supply a transformer's nominal output voltage when it is providing its maximum rated load (secondary) current with a specified primary voltage. If the load current is reduced, the secondary voltage will increase. In fact, the secondary voltage will reach its maximum value if the load is removed entirely. For moderately sized transformers the no-load voltage can be as much as 20% greater than the full-load voltage. This is described as the transformer's **voltage regulation**. It is defined by Eq. 4-15.

$$\%VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% \quad (4-15)$$

$\%VR$ is the percent of voltage regulation, V_{NL} is the no-load voltage, and V_{FL} is the full-load voltage.

Example 4-5. A transformer provides a secondary voltage of 10 Vrms when the load current is at its maximum value of 1.5 Arms with a primary voltage of 115 V rms. Its no-load secondary voltage is 12 V rms. Determine its percent of voltage regulation ($\%VR$).

Solution: We use Eq. 4-15 to find the percent of voltage regulation.

$$\%VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{12 \text{ V} - 10 \text{ V}}{10 \text{ V}} \times 100\% = 20\%$$

The transformer data sheets provided by the manufacturers of commercial off-the-shelf transformers do *not* typically include the percent of voltage regulation. To provide general guidance, Table 4-1 is provided and shows typical values. ***Transformers have volt-ampere (VA) ratings which are the product of the maximum rms secondary current and the corresponding rms secondary voltage.*** We can determine the VA rating of the transformer given in Example 4-5.

$$\text{VA Rating} = V_2 I_2 = (10 \text{ Vrms})(1.5 \text{ Arms}) = 15 \text{ VA}$$

Table 4-1.

VA Ratings and Typical $\%VR$				
VA Ratings	6 VA	12 VA	50 VA	100 VA
$\%VR$	25%	12%	10%	10%

Since the transformer in Example 4-5 has a VA Rating of 15 VA, we should use the value for a VA Rating of 12 VA.

Some transformers have center-tapped windings while others may have multiple primary and/or secondary windings [see Fig. 4-19]. Figure 4-19(c) illustrates the ***transformer dot convention***. The dots indicate which transformer terminals will be instantaneously positive. It is possible to obtain 180° of phase shift across the transformer. This is usually *not* a major concern in linear power supply designs. We shall see additional examples of transformers throughout the chapter. In all cases, the transformer's load will "see" the secondary as its AC voltage source.

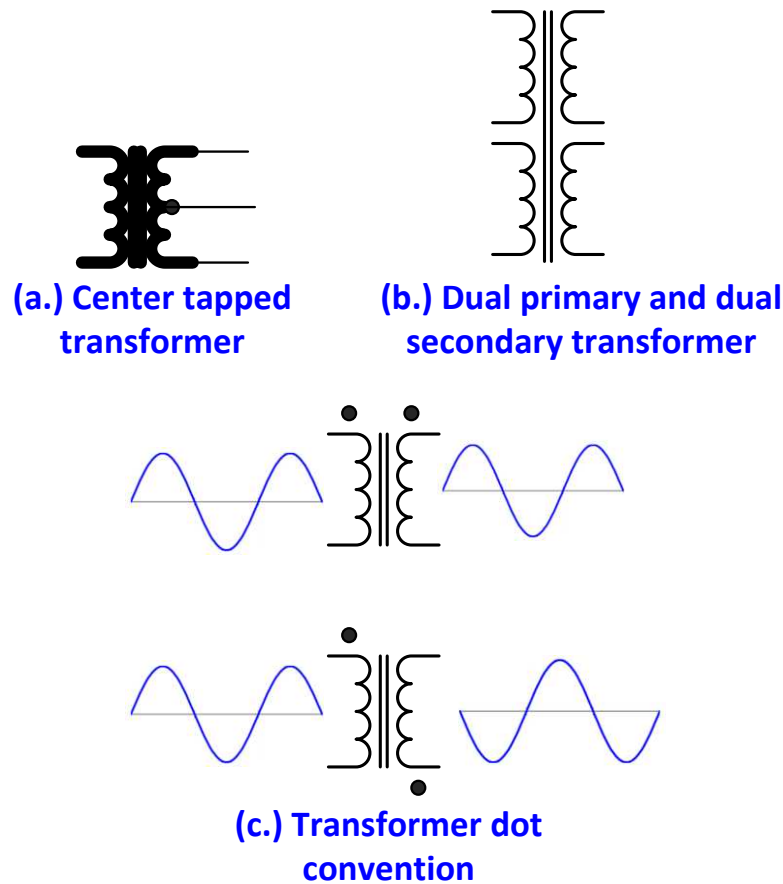


Figure 4-19.

4-6 The Half-Wave Rectifier

A rectifier circuit uses diodes to convert a sinusoidal waveform into a pulsating DC waveform. A pure sinusoidal waveform has an average value of zero. The purpose of a rectifier circuit is to distort a sinusoidal waveform such that it is always above or below the zero axis. This will produce a waveform with an average (DC) value. There are three fundamental rectifier circuits: the *half-wave rectifier*, the *full-wave rectifier using a center-tapped transformer*, and the *full-wave bridge rectifier*. A fourth configuration called a *dual complementary rectifier* employs a center-tapped transformer and a bridge rectifier. The purpose of the dual-complementary rectifier circuit is to generate both a positive and negative DC voltages of equal magnitude (e.g., ± 15 V or ± 40 V).

The operation of the half-wave rectifier was introduced in Section 3-8. However, in our circuit, we will be using a transformer. We shall investigate the transformers included in Multisim for simulation.

Multisim and Transformers

We will want to use Multisim to simulate our DC power supply circuits. We will need transformers. Multisim is started in the usual fashion. We can place a transformer by clicking on *Place Component*, place the Group in **<All Groups>**, and select **Transformer** [see Fig. 4-20]. We select **1P1S** - one primary and one secondary winding – transformer model.

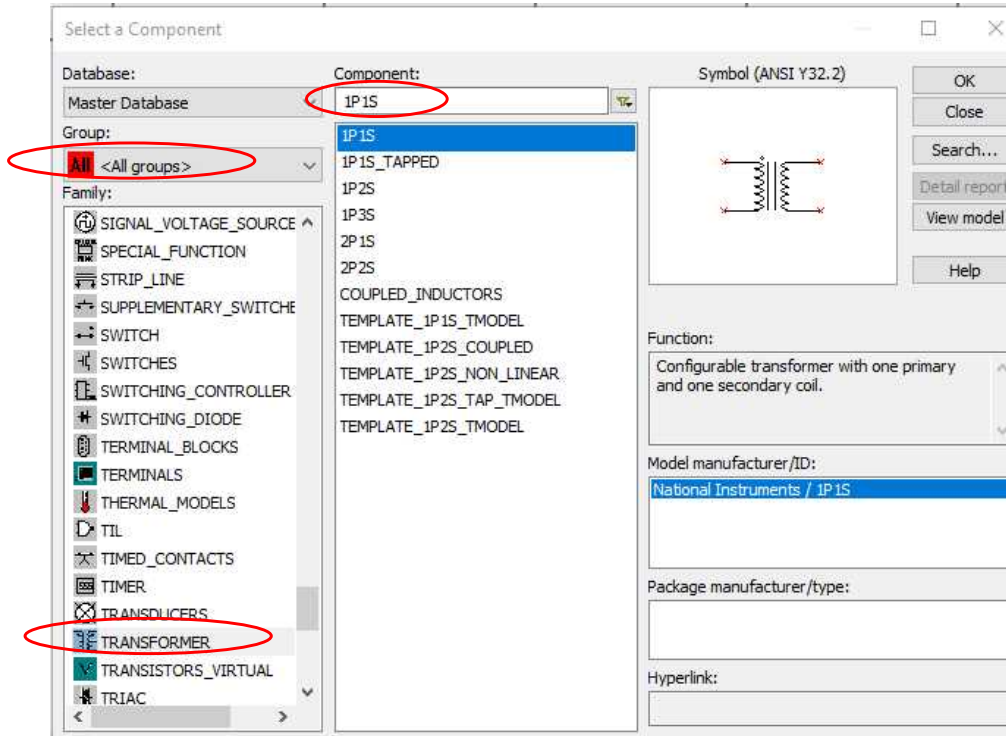


Figure 4-20.

The complete circuit is provided in Fig. 4-21. The 120-Vrms, 60-Hz voltage source simulates the power line. The default turns ratio is 10:1, which means the primary has ten times more windings than the secondary. Let's use the ideal transformer relationship to determine the secondary voltage.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} = \frac{1}{10}$$

$$V_2 = \frac{N_2}{N_1} V_1 = \left(\frac{1}{10} \right) (120 \text{ Vrms}) = 12 \text{ Vrms}$$

In a similar fashion, we can calculate the primary current. The secondary current can be determined by Ohm's law.

$$I_2 = \frac{V_2}{R_L} = \frac{12 \text{ Vrms}}{10 \, \Omega} = 1.2 \text{ Arms}$$

$$\frac{I_1}{I_2} = \frac{N_2}{N_1}$$

$$I_1 = \frac{N_2}{N_1} I_2 = \left(\frac{1}{10}\right) (1.2 \text{ Arms}) = 0.12 \text{ Arms} = 120 \text{ mA}$$

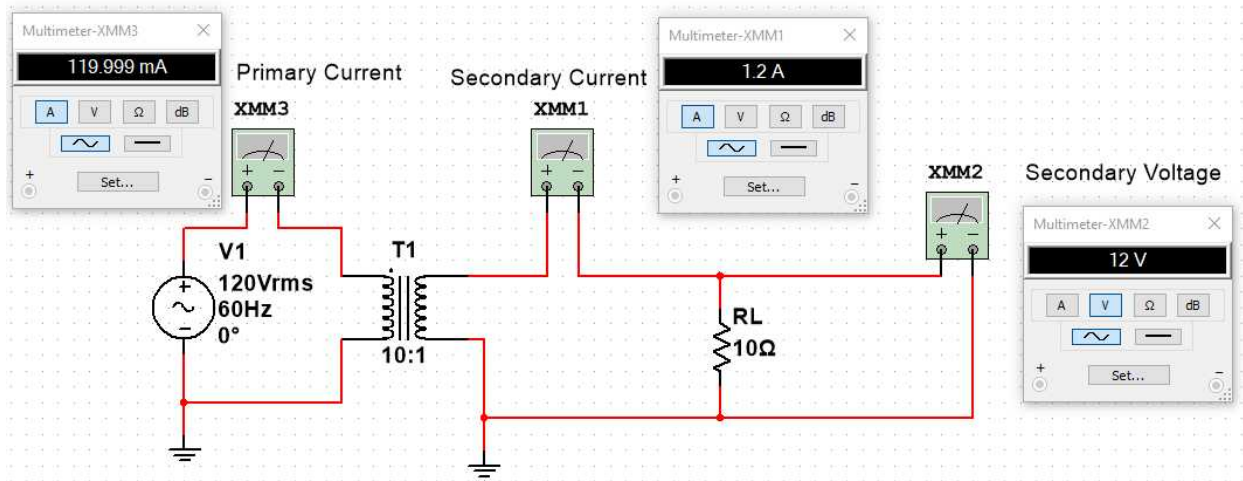


Figure 4-21.

The simulation verifies our calculations. Be sure to note the Digital Multimeters (DMMs) have been configured to measure AC. The ideal transformer used in the simulation has a percent of voltage regulation (%VR) of 0%. This is because the secondary voltage is constant, which means the no-load voltage (V_{NL}) is equal to the full-load voltage (V_{FL}). We use Eq. 4-15.

$$\%VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{12 \text{ Vrms} - 12 \text{ Vrms}}{12 \text{ Vrms}} \times 100\% = 0\%$$

Suppose we have a transformer with an open-circuit (no-load voltage) of 12 Vrms and a full-load voltage of 10 Vrms at a full-load current of 1 Arms. The problem is to take the ideal transformer and modify the transformer circuit to reflect the characteristics of the given “real” transformer. A resistor can be used to model the transformer losses. The equivalent circuit is provided in Fig. 4-22.

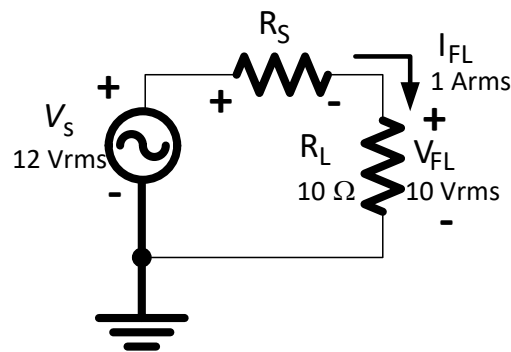


Figure 4-22.

In the equivalent circuit, the AC voltage source models the transformer’s secondary and R_L represents the external load. Resistor R_S models the transformer internal resistance. R_S is determined under full-load conditions. Kirchhoff’s Voltage Law (KVL) is used to find the voltage across R_S . Application of Ohm’s Law yields its value.

$$R_S = \frac{V_S - V_{FL}}{I_{FL}} = \frac{12 \text{ Vrms} - 10 \text{ Vrms}}{1 \text{ Arms}} = 2 \Omega$$

Resistor R_S is incorporated in the Multisim circuit as shown in Fig. 4-23.

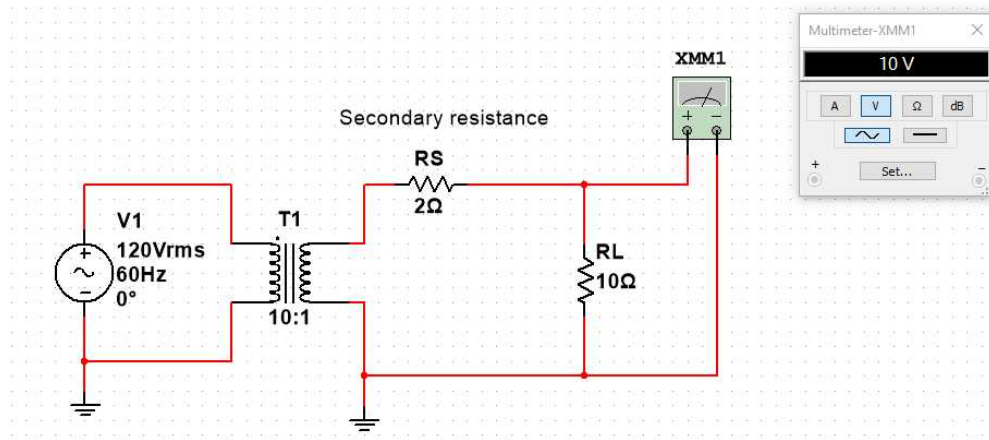


Figure 4-23.

If R_L is removed, the load current goes to zero. If the load current goes to zero, the voltage drop across R_S must also go to zero. By KVL, the voltage across the load position must be equal to the transformer secondary voltage. This is called the no-load voltage V_{NL} . Hence, $V_{NL} = V_2$ (or V_S in Fig. 4-22). This is demonstrated using Multisim by making R_L very large (i.e., gigohms) as indicated in Fig. 4-24.

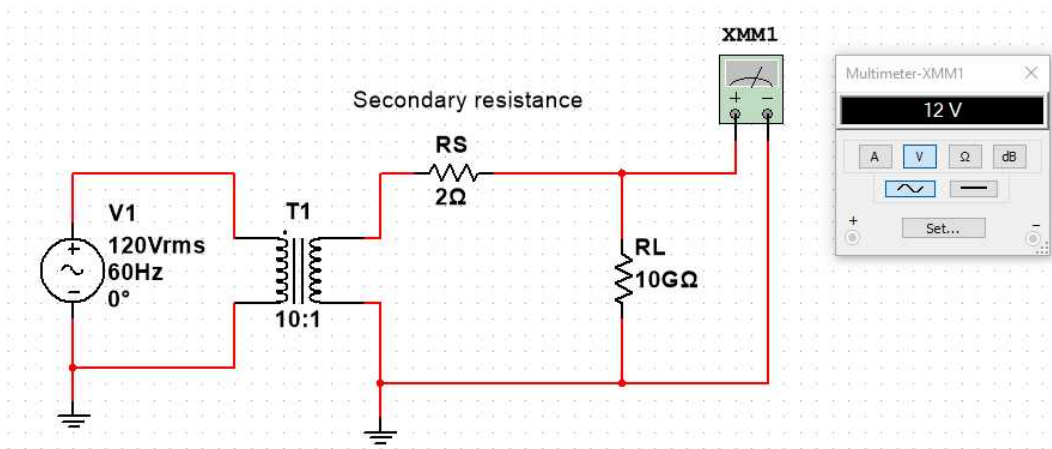


Figure 4-24.

Drawing on this result, leads us to Eq. 4-16.

$$R_S = \frac{V_{NL} - V_{FL}}{I_{FL}} \quad (4-16)$$

Half-Wave Rectifier Analysis

A half-wave rectifier circuit is given in Fig. 4-25(a). A Hammond 166JA12 chassis-mount transformer is used for transformer T_1 . It is specified to provide a secondary voltage of 12 Vrms at a full-load secondary current of 1 Arms with a primary voltage of 115 Vrms. We find the peak source (primary) voltage (V_m).

$$V_m = \sqrt{2}V_s = \sqrt{2}(115 \text{ Vrms}) = 163 \text{ V}$$

We use the indicated turns ratio to find V_2 .

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{1}{9.583} (115 \text{ Vrms}) = 12 \text{ Vrms}$$

Now we find the peak secondary voltage.

$$V_m = \sqrt{2}V_s = \sqrt{2}(12 \text{ Vrms}) = 17.0 \text{ V}$$

The frequency of the primary and secondary voltage is 60 Hz. The corresponding period (T) is found next.

$$T = \frac{1}{f} = \frac{1}{60 \text{ Hz}} = 16.7 \text{ ms}$$

In Fig. 4-25(b) we see that during the positive half-cycle of the secondary voltage, the (silicon) diode conducts. Using the knee-voltage diode model, we have indicated a diode voltage drop of 0.7 V. The **peak rectified voltage** (V_{dcm}) across the load is the peak secondary voltage minus the diode voltage drop. This is given by Eq. 4-17.

$V_{dcm} = V_m - 0.7\text{V}$

 (4-17)

Using Eq. 4-17 we find V_{dcm} .

$$V_{dcm} = V_m - 0.7 \text{ V} = 17.0 \text{ V} - 0.7 \text{ V} = 16.3 \text{ V}$$

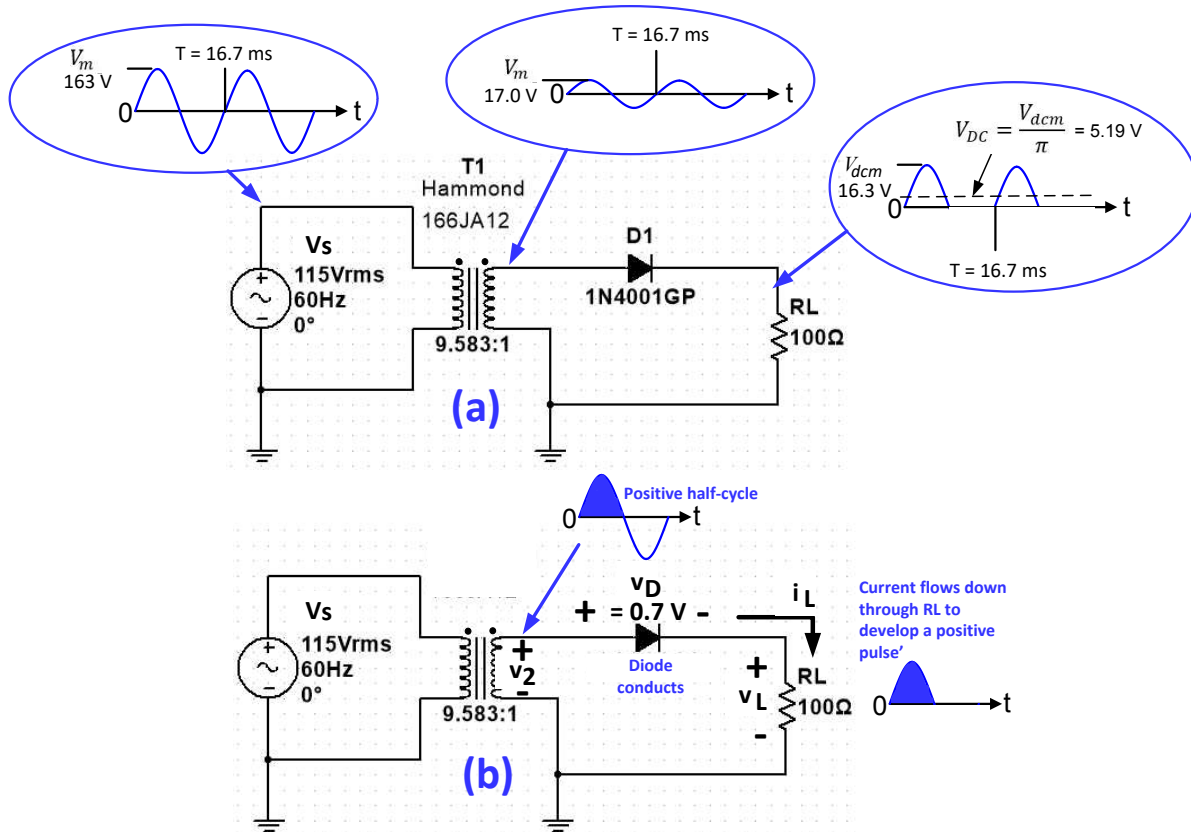


Figure 4-25.

Figure 4-26 shows the circuit condition when the AC secondary voltage is on its negative half-cycle. In this case, the diode is reverse biased and acts like an open switch. The current through the load is zero, which means the voltage drop across it is also zero. Putting these ideas together explains why the half-wave rectified voltage is developed across R_L . The waveform is given in Fig. 4-25(a). The DC average value is also indicated in Fig. 4-25(a). Equation 4-8 is used.

$$V_{DC} = \frac{V_{dcm}}{\pi} = \frac{16.3 V}{\pi} = 5.19 V$$

As can be seen in Fig. 4-26 (using KVL) the peak reverse bias (V_{RM}) across the diode is determined by Eq. 4-18.

$$V_{RM} = V_m$$

(4-18)

In our example we obtain the result below.

$$V_{RM} = V_m = 17.0 V$$

The diode's peak **repetitive reverse voltage rating** (V_{RRM}) must exceed this value. If it does not, the diode may experience avalanche breakdown.

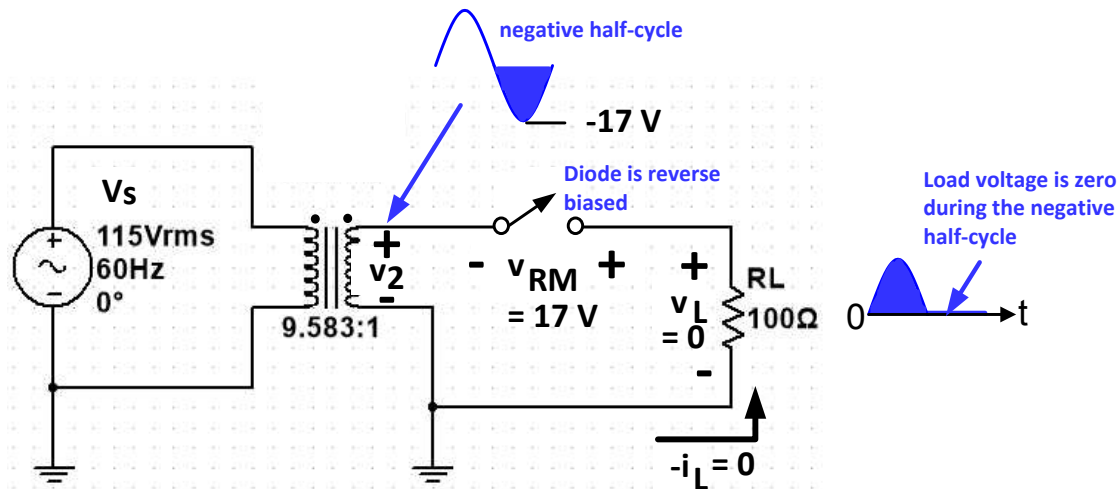


Figure 4-26.

The waveforms associated with the DC power supply are shown in Fig. 4-27. Be sure to note the definitions of v_2 , v_L , v_D , and i_L in Fig. 4-27. When voltages and the current agree with the definitions, they are taken as positive quantities. Conversely, when they are in the opposite direction, they are held to be negative. The secondary voltage waveform is shown in Fig. 4-27(b). Since the secondary voltage is 12 Vrms, its corresponding peak value is 17.0 V. Since its frequency (f) is 60 Hz, its period ($T = 1/f$) is 16.7 ms. (One half of the period is 8.33 ms.) The load voltage waveform is provided in Fig. 4-27(c). The peak rectified voltage (V_{dcm}) and the DC average value (V_{DC}) have been included. The diode voltage waveform (v_D) is given in Fig. 4-27(d). When the diode is forward biased, its voltage drop is 0.7 V. When the secondary voltage is negative, the diode drops all the voltage. In this case, our concern is the maximum reverse bias (V_{RM}). Again, it must not exceed the diode's reverse repetitive voltage rating (V_{RRM}). Figure 4-27(e) shows the load current. By Ohm's Law, it is proportional to the load voltage. Its average value is I_{DC} . Equations 4-19 and 4-20 are used in the analysis of the load current waveform. You should study Fig. 4-27 carefully.

$$I_m = \frac{V_{dcm}}{R_L} \quad (4-19)$$

$$I_{DC} = \frac{I_m}{\pi} \quad (4-20)$$

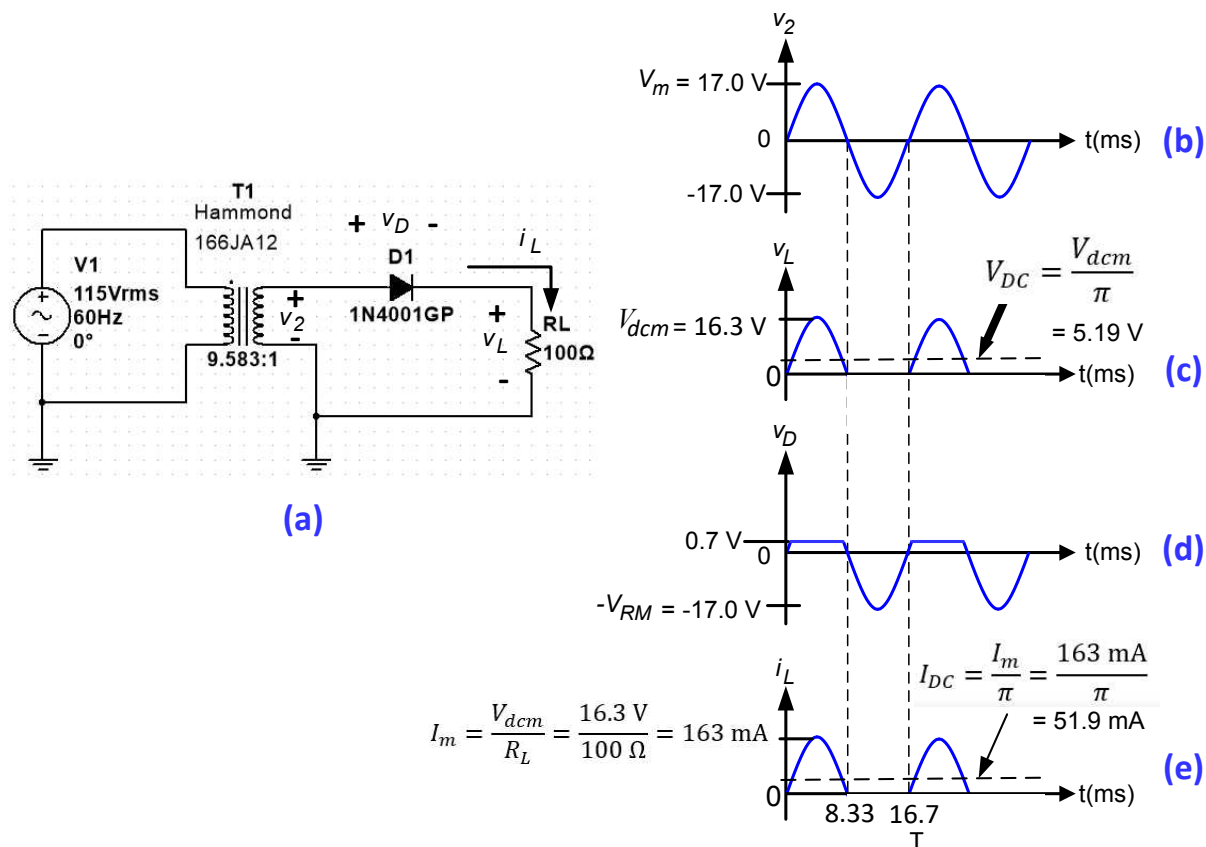


Figure 4-27.

Half-wave rectifiers are used rarely for line-operated DC power supplies. The relative simplicity of the half-wave rectifier does *not* compensate for its many disadvantages. A half-wave rectifier is difficult to filter, and the unidirectional current through the transformer's secondary tends to bias its iron core magnetically. The transformer bias reduces its efficiency and can distort the secondary waveform.

Example 4-6. The transformer secondary voltage in Fig. 4-27(a) has been increased to 24 Vrms. Determine the peak secondary voltage, the peak rectified voltage across the load, the DC load voltage, the diode's maximum reverse bias, the peak load current, and the DC load current.

Solution: The quantities will be determined using the order in which they were requested. First, we find the peak secondary voltage (V_m).

$$V_m = \sqrt{2}V_2 = \sqrt{2}(24 \text{ Vrms}) = 33.9 \text{ V}$$

The silicon diode is assumed to drop 0.7 V when it conducts. This assumption permits us to solve for the peak rectified voltage (V_{dcm}) across the load. We use Eq. 4-17.

$$V_{dcm} = V_m - 0.7 \text{ V} = 33.9 \text{ V} - 0.7 \text{ V} = 33.2 \text{ V}$$

Since we have a half-wave rectifier, we employ Eq. 4-8 to find V_{DC} .

$$V_{DC} = \frac{V_{dcm}}{\pi} = \frac{33.2 \text{ V}}{\pi} = 10.6 \text{ V}$$

The diode's maximum reverse bias (V_{RM}) is determined by using Eq. 4-18.

$$V_{RM} = V_m = 33.9 \text{ V}$$

The peak load current (I_m) is given by Eq. 4-19.

$$I_m = \frac{V_{dcm}}{R_L} = \frac{33.2 \text{ V}}{100 \Omega} = 332 \text{ mA}$$

The load current waveform is a half-wave rectified waveform, which means we can use Eq. 4-20. However, we shall use Ohm's Law instead.

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{10.6 \text{ V}}{100 \Omega} = 106 \text{ mA}$$

It should be noted the peak current through the diode is 332 mA, and its average forward current is 106 mA. The diode average forward current is designated $I_{D(AV)}$.

Multisim has been used to simulate the circuit [see Fig. 4-28]. It is recommended that you duplicate the simulation.

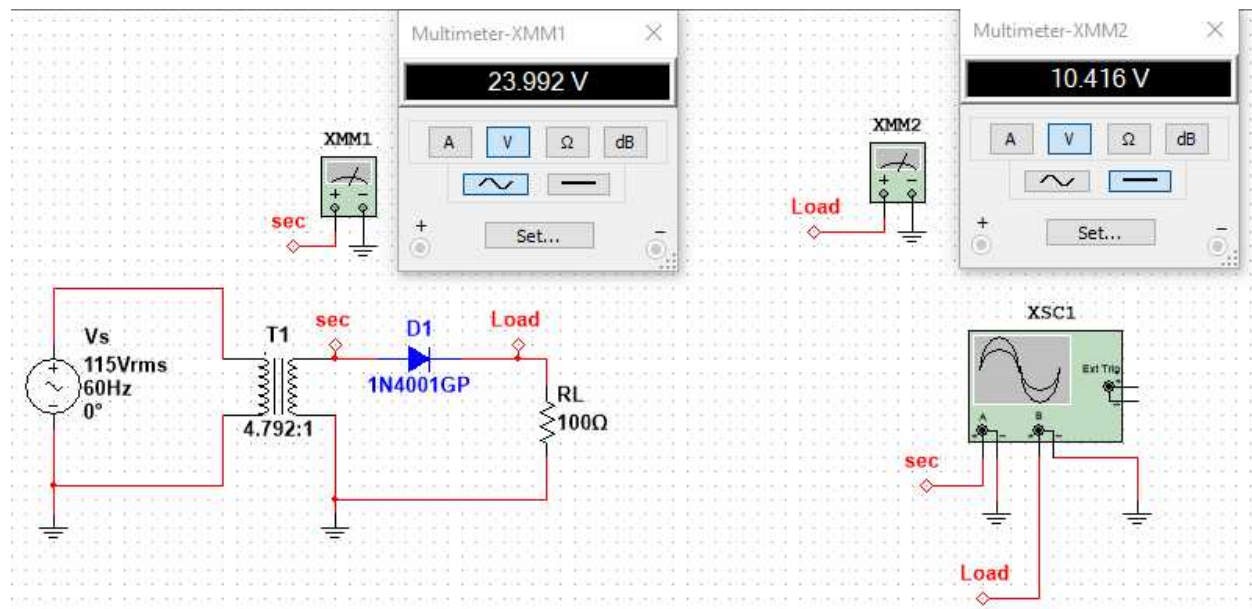


Figure 4-28.

On-page connectors are used to simplify the wiring. In Multisim click on **Place, Connectors**, and select **On-page connector**. Connectors that have the same label are connected. For example, the transformer secondary connector has been labeled “sec”. A connector with the same name is attached to DMM1 and the channel 1 input of the oscilloscope. In Fig. 4-28 we see the secondary voltage is very nearly 24 Vrms. The average voltage across the load is 10.416 V. This about 2% less than our predicted value of 10.6 V.

The oscilloscope display is shown in Fig. 4-29. Adjust the settings to match those in the figure. Click on the cursors on the left side of the screen and drag them into the position indicated.

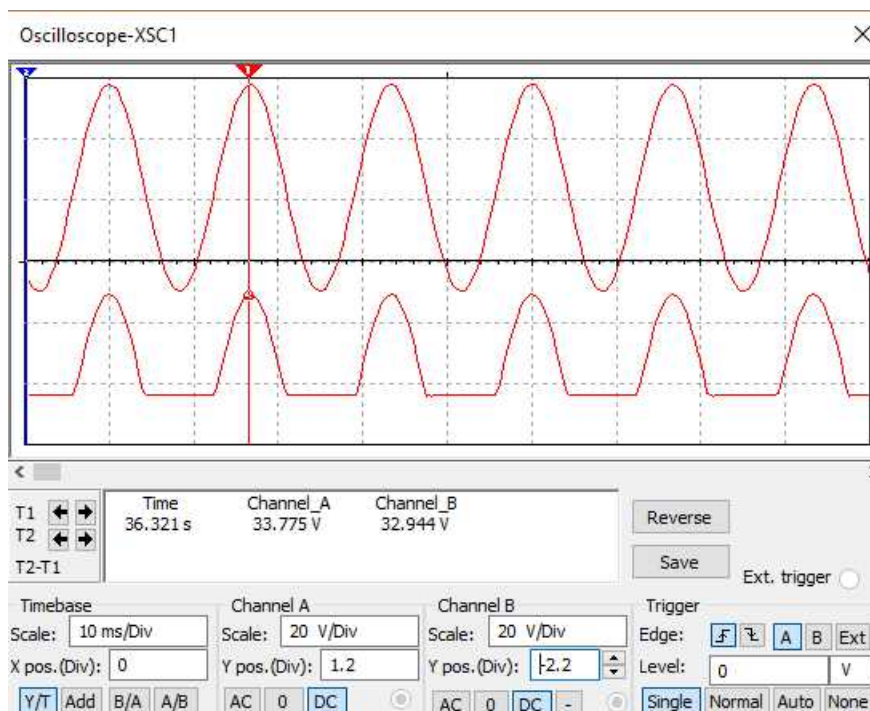


Figure 4-29.

The transformer secondary voltage is on Channel A and the load voltage is displayed on Channel B. Both channels are set to **20 V per division**. The waveforms will flicker and occasionally roll across the screen. The waveforms can be “frozen” by changing the trigger from **Auto Trigger** to **Single Trigger**. The two waveforms can be separated by adjusting the **Y position**. Two cursors are available and located at the left of the screen. Move the mouse to the left side of the screen. Hold the left mouse button down to drag Cursor 1 to the position shown. The instantaneous voltage of Channel A and Channel B appears in the table.

The peak secondary voltage (V_m) was calculated to be 33.9 V in Example 4-6. The oscilloscope indicates about 33.8 V. The peak rectified voltage (V_{dcm}) was determined to be 33.2 V in Example 4-6. The oscilloscope shows 32.9 V. The oscilloscope reading is approximately 0.9% lower. We have very close agreement between our calculations and the simulation.

4-7 Full-Wave Rectifiers Using a Center-Tapped Transformer

The operation of the half-wave rectifier can be extended to the full-wave rectifier circuit using a center-tapped transformer as shown in Fig. 4-30(a). In this circuit the transformer secondary voltage is 24 Vrms with a center tap. This means 12 Vrms is available between the upper lead and the center tap as well as between the lower lead and the center tap. This is illustrated in Fig. 4-30(b) along with the primary and secondary waveforms. Observe that when the upper terminal is positive, the lower terminal is negative. *If the center tap is taken as the ground reference, the two waveforms are 180° out of phase.*

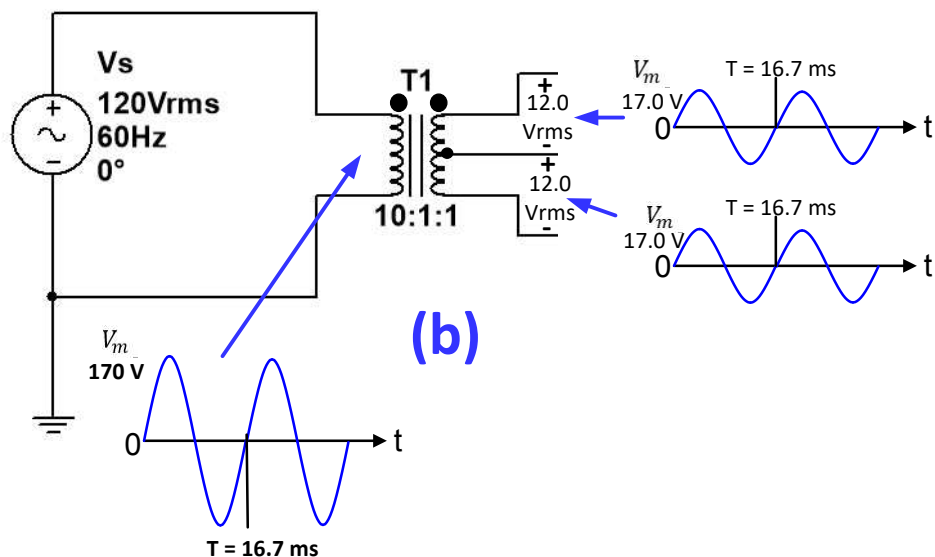
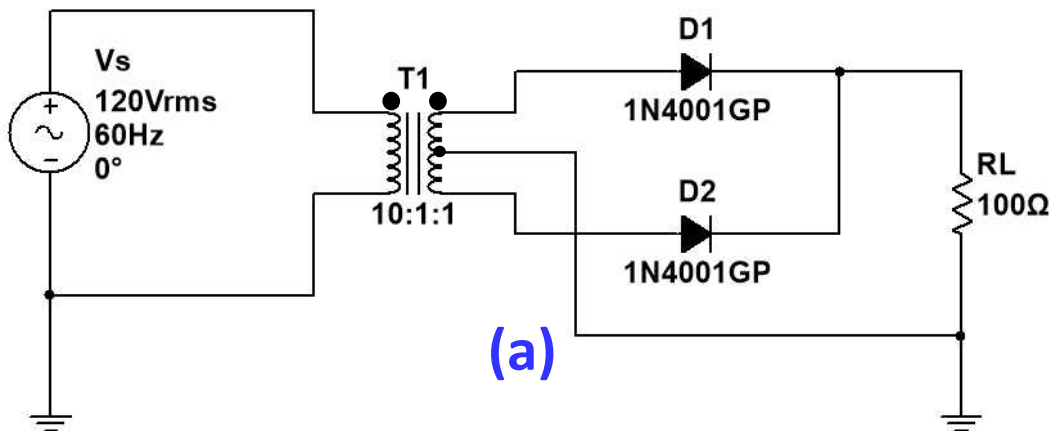


Figure 4-30.

Figure 4-31 illustrates the basic operation of the full-wave rectifier using a center-tapped transformer. In Fig. 4-31(a) we see the instantaneous polarities of the secondary waveforms during their positive half cycle. Diode D_1 is forward biased (positive to its anode) and diode D_2 is reverse biased (negative to its anode). The voltage drop across D_1 is held to be a constant 0.7 V (knee-voltage model) while diode D_2 behaves like an open switch. Since diode D_2 acts like an open, it and its circuitry have been removed to clarify the circuit operation as shown in Fig. 4-31(b). Current flows down through the load resistance R_L to develop a positive pulse of voltage across it.

During the negative half-cycle of the secondary voltage, the lower terminal of the transformer becomes positive relative to the center tap as shown in Fig. 4-31(c). As can be seen, diode D_2 is forward biased while diode D_1 is reverse biased. Diode D_2 has a voltage drop of 0.7 V and diode D_1 is an open switch. To simplify the discussion, the diode D_1 circuit has been removed to produce the equivalent circuit given in Fig. 4-31(d). Again, current flows down through the load and another positive pulse is produced. **Since both the positive and negative cycles are used to produce positive pulses across the load, the entire (full) wave is being used. Hence, we call this full-wave rectification.**

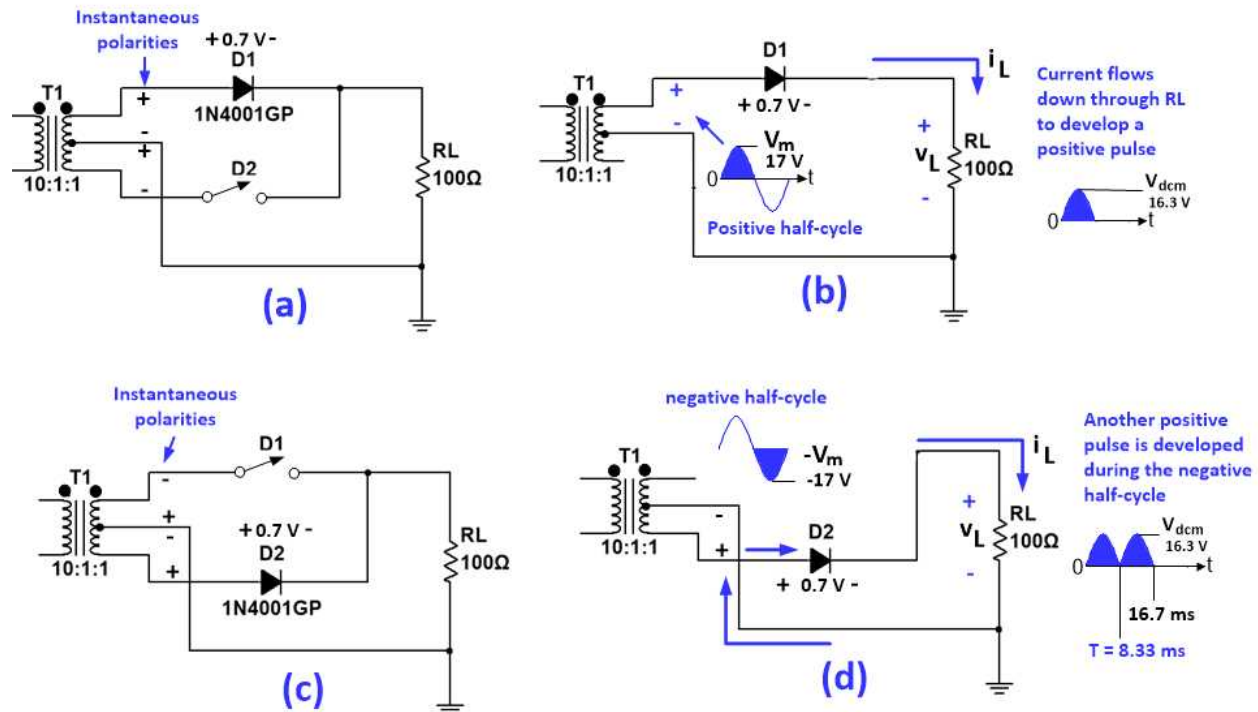


Figure 4-31.

Since we are using one half of the transformer secondary on each half-cycle, **the peak voltage (V_m) is the peak voltage across one half of the secondary.** Equation 4-21 is used to determine the peak rectified voltage across the load. Only one diode conducts at a time so KVL indicates we subtract the voltage drop of the diode in conduction.

$$V_{dcm} = V_m - 0.7V \quad (4-21)$$

In Fig. 4-31(d) we see the period (T) of the full wave rectified waveform is 8.33 ms. The corresponding frequency (f) can be determined.

$$f = \frac{1}{T} = \frac{1}{8.33 \text{ ms}} = 120 \text{ Hz}$$

The full-wave rectified waveform has a frequency that is twice the power-line frequency. Next, we shall determine the maximum reverse bias placed across the diodes. Consider Fig. 4-32.

We write a KVL equation starting at the “+” of V_{RM} for diode D_2 . We work our way around the closed loop (follow the arrows) and use the signs for the voltages as we encounter them as we proceed in the *same* direction. When we return to the “+” of V_{RM} for diode D_2 , we set the algebraic sum to zero.

$$V_{RM} - V_m - V_{dcm} = 0$$

We solve for V_{RM} and substitute in Eq. 4-21 for V_{dcm} .

$$V_{RM} = V_{dcm} + V_m = (V_m - 0.7V) + V_m = 2V_m - 0.7V$$

Equation 4-22 is used to calculate the maximum reverse bias (V_{RM}) across each of the diodes. If we repeat the analysis for diode D_1 , we will get the same result.³⁵

$$V_{RM} = 2V_m - 0.7V \quad (4-22)$$

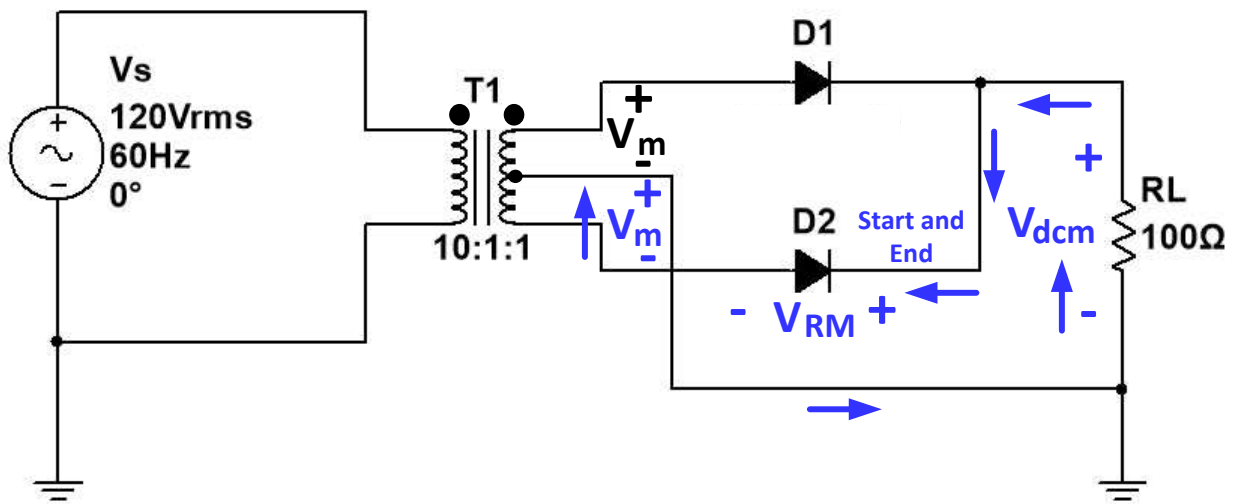


Figure 4-32.

³⁵ To use the phrase, they taught us to say in Professor School, “The proof is left as an exercise for the student.”

The waveforms associated with the full-wave rectifier using a center-tapped transformer are provided in Fig. 4-33. Figure 4-33(b) depicts the voltage across one half of the transformer's (upper) secondary winding. Figures 4-33(c) and 4-33(d) show the voltages across diodes D_1 and D_2 , respectively. It is important to note the diodes alternate in conduction. Each diode conducts half of the time. This means the average current $[I_{D(AV)}]$ through each of the diodes is equal to one half of the DC load current. This is given by Eq. 4-23. This observation is important because it tells us the required diode forward current rating.

$$I_{D(AV)} = \frac{I_{DC}}{2} \quad (4-23)$$

Figure 4-33(e) shows the full wave rectified waveform. Equation 4-9 is used to determine its average value.

$$V_{DC} = 2 \frac{V_{dcm}}{\pi} = 2 \frac{16.3 \text{ V}}{\pi} = 10.8 \text{ V}$$

Although not shown, the current waveform through the resistive load will look like the voltage waveform. The average DC load current here is:

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{10.8 \text{ V}}{100 \Omega} = 108 \text{ mA}$$

From Eq. 4-23 the average diode current ($I_{D(AV)}$) is 54 mA.

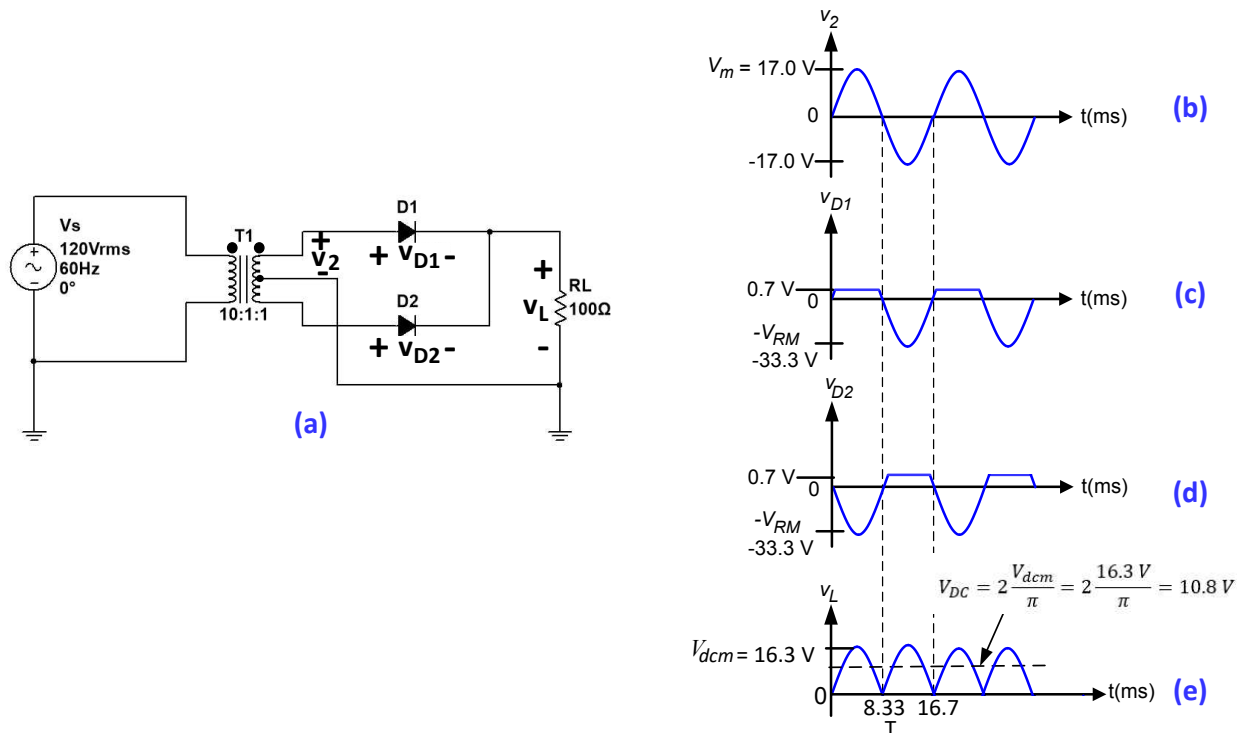


Figure 4-33.

Example 4-7. Analyze the full-wave rectifier circuit given in Fig. 4-34. A Signal Transformer (part number ST-7-48) transformer has been specified. This transformer is designed to be mounted on a printed-circuit board. The transformer has two separate secondary windings that can be connected as shown in Fig. 4-34 to form a center tap. The transformer is rated to be 48 VCT at a maximum secondary current of 0.7 Arms. Determine the peak secondary voltage (V_m) across one half of the secondary, the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$].

Solution: The quantities will be determined using the order in which they were requested. First, we find V_m .

$$V_m = \sqrt{2}V_2 = \sqrt{2}(24 \text{ Vrms}) = 33.9 \text{ V}$$

The silicon diode is assumed to drop 0.7 V when it conducts. This assumption permits us to solve for the peak rectified voltage (V_{dcm}) across the load. We use Eq. 4-21.

$$V_{dcm} = V_m - 0.7 \text{ V} = 33.9 \text{ V} - 0.7 \text{ V} = 33.2 \text{ V}$$

Since we have a full-wave rectifier, we employ Eq. 4-9 to find V_{DC} .

$$V_{DC} = 2 \frac{V_{dcm}}{\pi} = \frac{(2)(33.2\text{V})}{\pi} = 21.1 \text{ V}$$

The diode's maximum reverse bias (V_{RM}) is determined by using Eq. 4-22.

$$V_{RM} = 2V_m - 0.7\text{V} = (2)(33.9\text{V}) - 0.7\text{V} = 67.1\text{V}$$

The peak load current (I_m) is given by Eq. 4-19.

$$I_m = \frac{V_{dcm}}{R_L} = \frac{33.2 \text{ V}}{100 \Omega} = 332 \text{ mA}$$

The load current waveform is a full wave rectified waveform. We shall use Ohm's Law.

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{21.1 \text{ V}}{100 \Omega} = 211 \text{ mA}$$

It should be noted the peak current through the diode is 332 mA. The diode average forward current is designated $I_{D(AV)}$. We use Eq. 4-23.

$$I_{D(AV)} = \frac{I_{DC}}{2} = \frac{211 \text{ mA}}{2} = 105.5 \text{ mA}$$

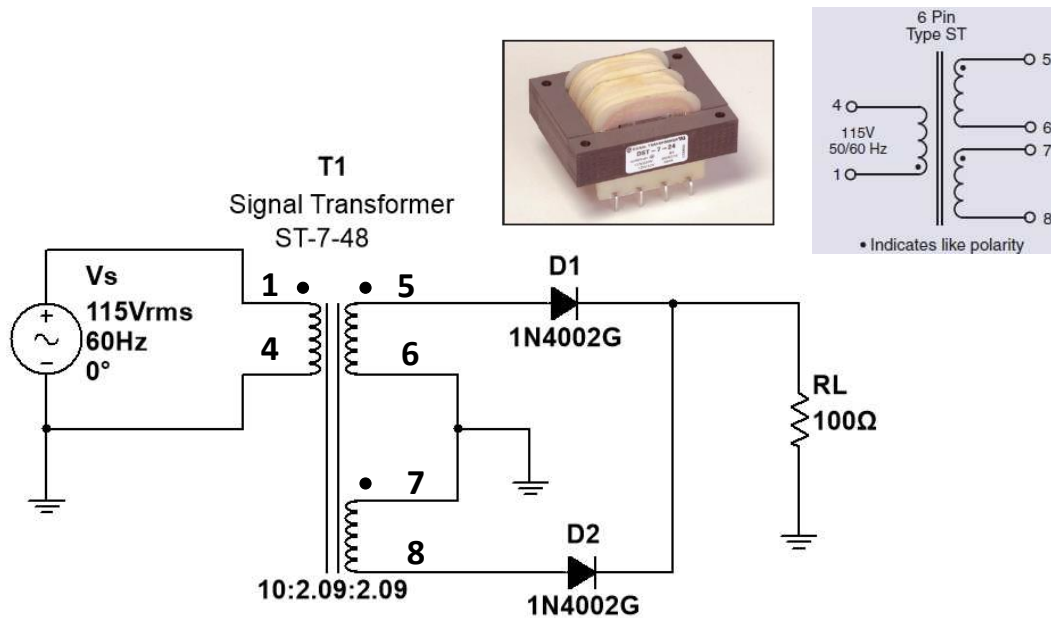


Figure 4-34.

While we have focused on power supplies that provide positive DC output voltages, *negative DC output voltages can be obtained by reversing both diodes* as shown in Fig. 4-35.

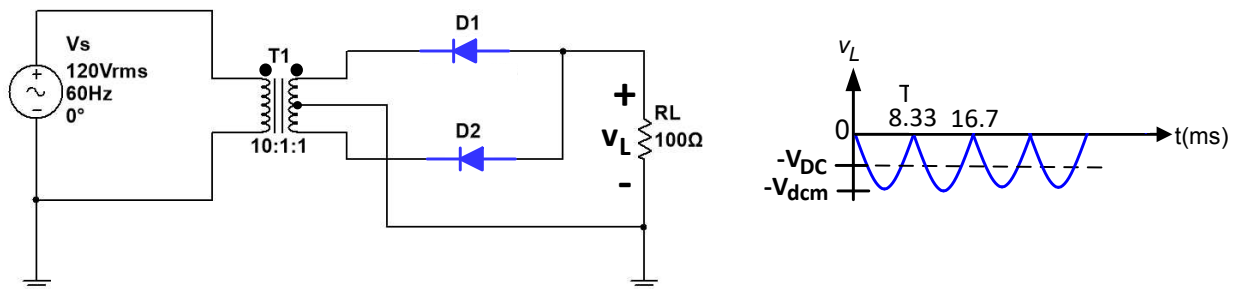


Figure 4-35.

4-8 Full-Wave Bridge Rectifiers

The full-wave bridge rectifier is a popular choice for DC power supply designs. It is the only choice if a center-tapped transformer is not available. Some typical circuits are shown in Fig. 4-36. You should verify the circuits are equivalent. As can be seen in Fig. 4-36, four (4) diodes are required to construct a full-wave bridge rectifier.

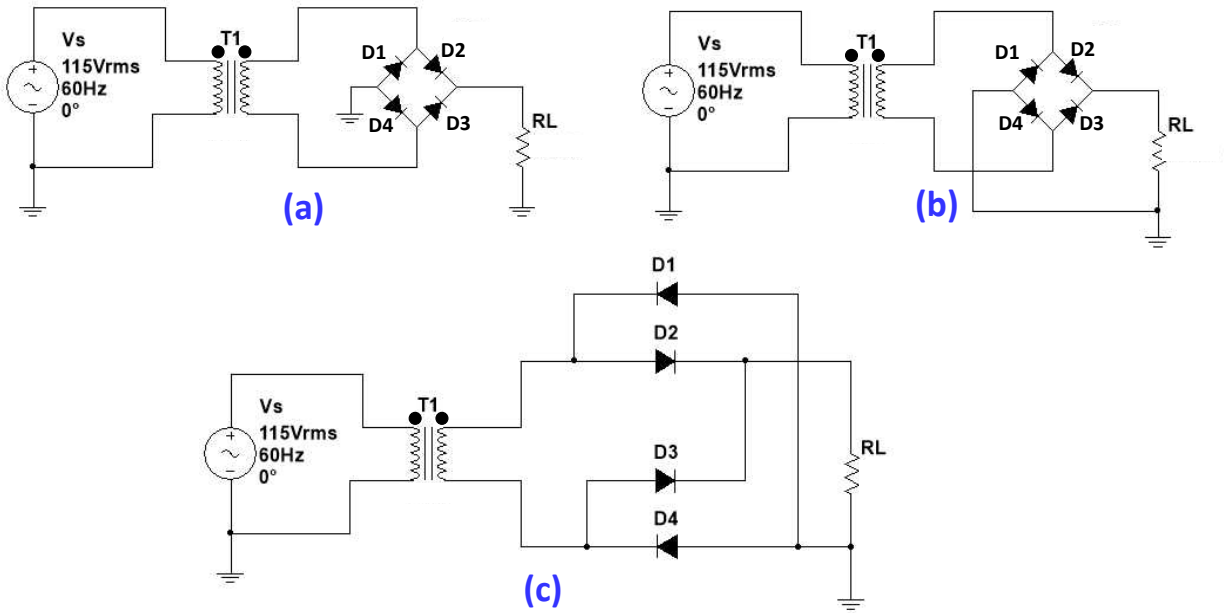


Figure 4-36.

The popularity of the full-wave bridge rectifier has prompted semiconductor manufacturers to offer four diodes configured as a bridge in a single package as shown in Fig. 4-37. We see packages for surface mount, through hole, and chassis mount. Required current and voltage ratings constrain the package choices.

Full-Wave Bridge Packages



Figure 4-37.

To illustrate the operation of the full wave bridge it has been redrawn in Fig. 4-38(a). When the upper terminal of the transformer becomes positive, diodes D_2 and D_4 will conduct as shown in Fig. 4-38(b). Diodes D_1 and D_3 are reverse biased. When the bottom terminal of the transformer is positive, diodes D_1 and D_3 will conduct as shown in Fig. 4-38(c). Diodes D_2 and D_4 are reverse biased.

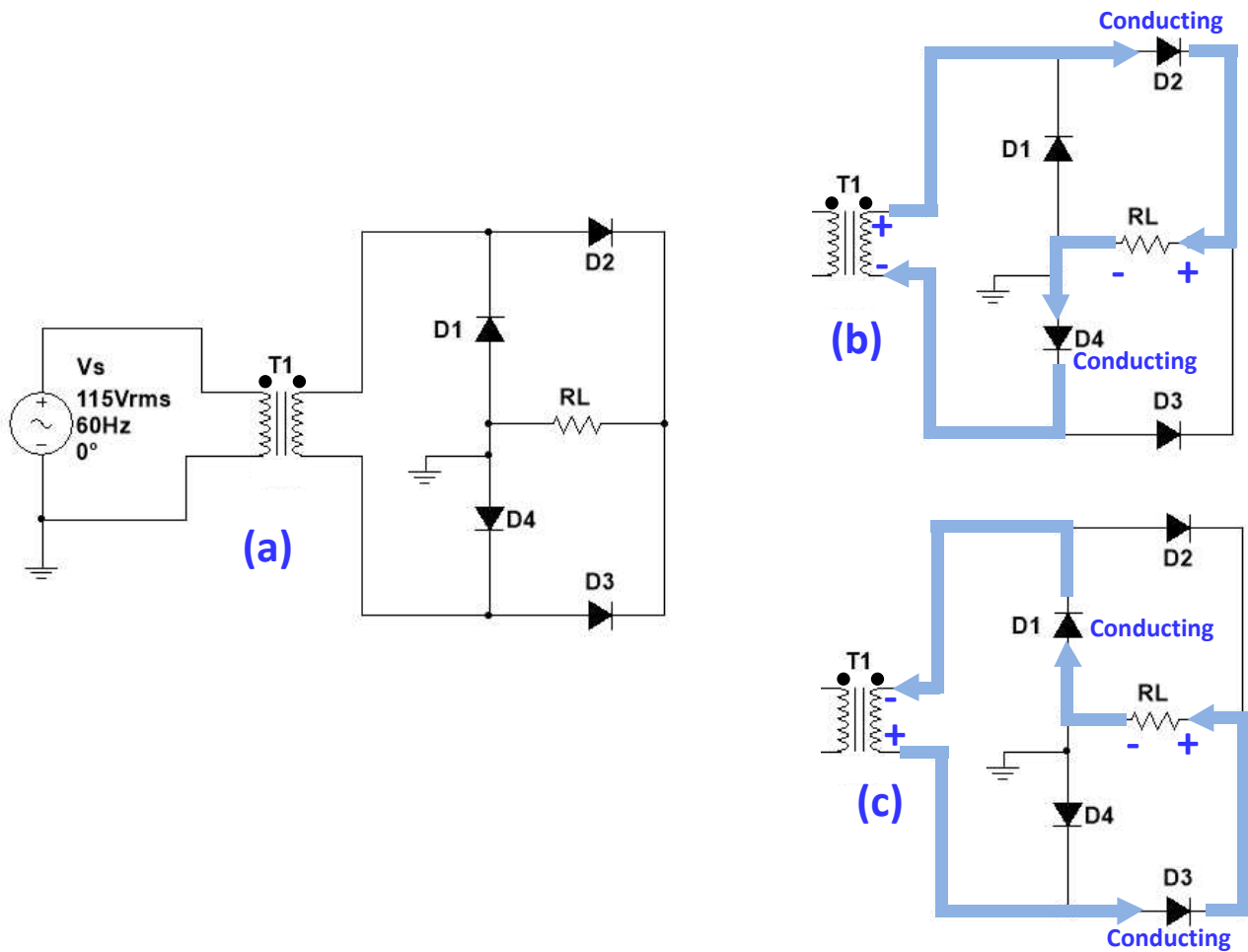


Figure 4-38.

In Fig. 4-39(a) we use KVL to determine the peak rectified voltage (V_{dcm}) across the load, diodes D_1 and D_3 act like open switches.

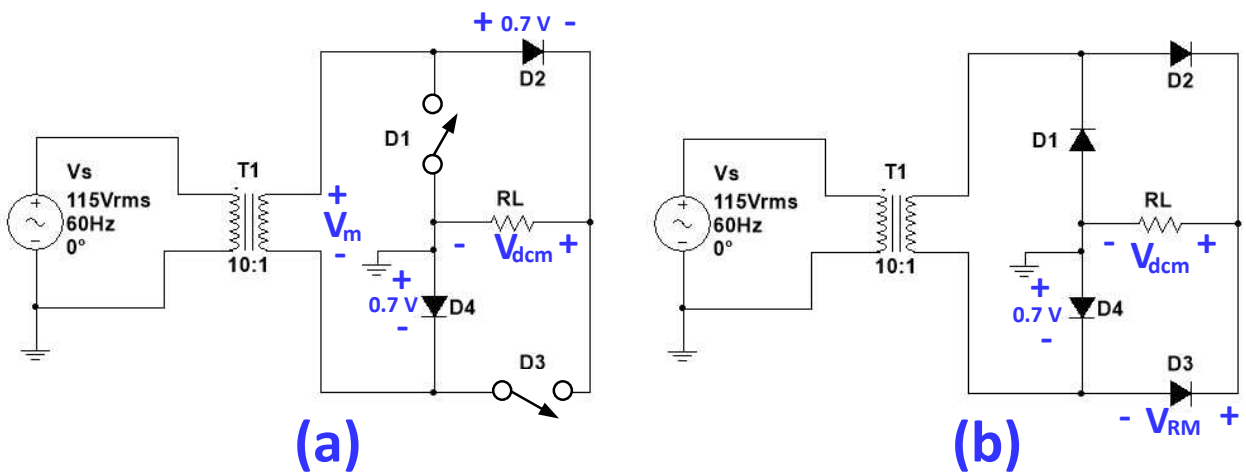


Figure 4-39.

We start at the negative terminal of the peak secondary voltage V_m and write around the loop. We then solve for V_{dcm} and obtain Eq. 4-24.

$$-V_m + 0.7\text{ V} + V_{dcm} + 0.7\text{ V} = 0$$

$$V_{dcm} = V_m - 0.7\text{ V} - 0.7\text{ V}$$

$$\boxed{V_{dcm} = V_m - 1.4\text{ V}} \quad (4-24)$$

To find the maximum reverse bias (V_{RM}) we employ Fig. 4-39(b) and use KVL. We start at the negative terminal of the load and write around the loop that includes diodes D_3 and D_4 . We solve for V_{RM} to reach Eq. 4-25.

$$-V_{dcm} + V_{RM} - 0.7\text{ V} = 0$$

$$V_{RM} = V_{dcm} + 0.7\text{ V} = (V_m - 1.4\text{ V}) + 0.7\text{ V} = V_m - 0.7\text{ V}$$

$$\boxed{V_{RM} = V_m - 0.7\text{ V}} \quad (4-25)$$

Example 4-8. Analyze the full-wave bridge rectifier circuit given in Fig. 4-38(a). The transformer has a secondary voltage of 25.2 Vrms with a maximum current rating of 2.8 Arms. The load resistor R_L is 50 Ω . Determine the peak secondary voltage (V_m), the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$]. Construct the circuit using Multisim. Obtain the waveform across R_L and use the cursor to find V_{dcm} . Use DMMs to measure I_{DC} and V_{DC} .

Solution: The quantities will be determined using the order in which they were requested. First, we find V_m .

$$V_m = \sqrt{2}V_2 = \sqrt{2}(25.2\text{ Vrms}) = 35.6\text{ V}$$

We use Eq. 4-24.

$$V_{dcm} = V_m - 1.4\text{ V} = 35.6\text{ V} - 1.4\text{ V} = 34.2\text{ V}$$

Since we have a full wave rectifier, we employ Eq. 4-13 to find V_{DC} .

$$V_{DC} = 2 \frac{V_{dcm}}{\pi} = \frac{(2)(34.2\text{ V})}{\pi} = 21.8\text{ V}$$

The diode's maximum reverse bias (V_{RM}) is determined by using Eq. 4-25.

$$V_{RM} = V_m - 0.7\text{ V} = (35.6\text{ V}) - 0.7\text{ V} = 34.9\text{ V}$$

The peak load current (I_m) is given by Eq. 4-19.

$$I_m = \frac{V_{dcm}}{R_L} = \frac{34.2 \text{ V}}{50 \Omega} = 684 \text{ mA}$$

The load current waveform is a full wave rectified waveform. We shall use Ohm's Law.

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{21.8 \text{ V}}{50 \Omega} = 436 \text{ mA}$$

It should be noted the peak current through a conducting diode is 684 mA. The diode average forward current is designated $I_{D(AV)}$. (Each pair of diodes only conduct one-half of the time.) We use Eq. 4-23.

$$I_{D(AV)} = \frac{I_{DC}}{2} = \frac{436 \text{ mA}}{2} = 218 \text{ mA}$$

To use Multisim, we need to determine the turns ratio for the transformer and find N_2 . Use $N_1 = 10$.

$$\frac{N_2}{N_1} = \frac{V_2}{V_1}$$

$$N_2 = \frac{V_2}{V_1} N_1 = \frac{25.2 \text{ V}}{115 \text{ V}} (10) = 2.191$$

These values are used to edit the transformer model as shown in Fig. 4-40.

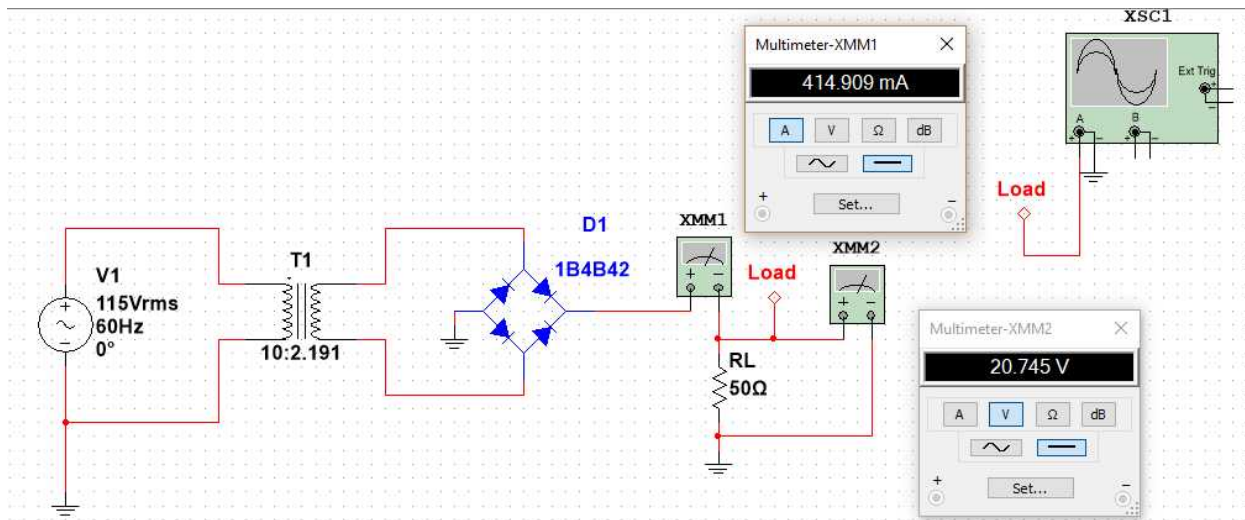


Figure 4-40.

The oscilloscope details are provided in Fig. 4-41. Our calculations gave a V_{dcm} of 34.2 V and the oscilloscope provided 33.3 V, which is about 2.6% low. V_{DC} was computed to be 21.8 V and Multisim yielded an answer of 20.7 V (about 5% low). The DC load current was calculated to be 436 mA while Multisim gave 415 mA, which is about 4.8% low. The calculations and the simulation results are reasonably close.

Note the circled settings in Fig. 4-41. The time base is adjusted to 10 ms per division to display the desired number of cycles. The vertical sensitivity is set to 20 V per division, so we can see the entire waveform. The default trigger mode is Auto. While the simulation is running the screen will appear to flicker. We fix that by adjusting the trigger to single sweep with a trigger level of three (3) volts. The controls of a physical oscilloscope will behave in a manner that is quite similar.³⁶

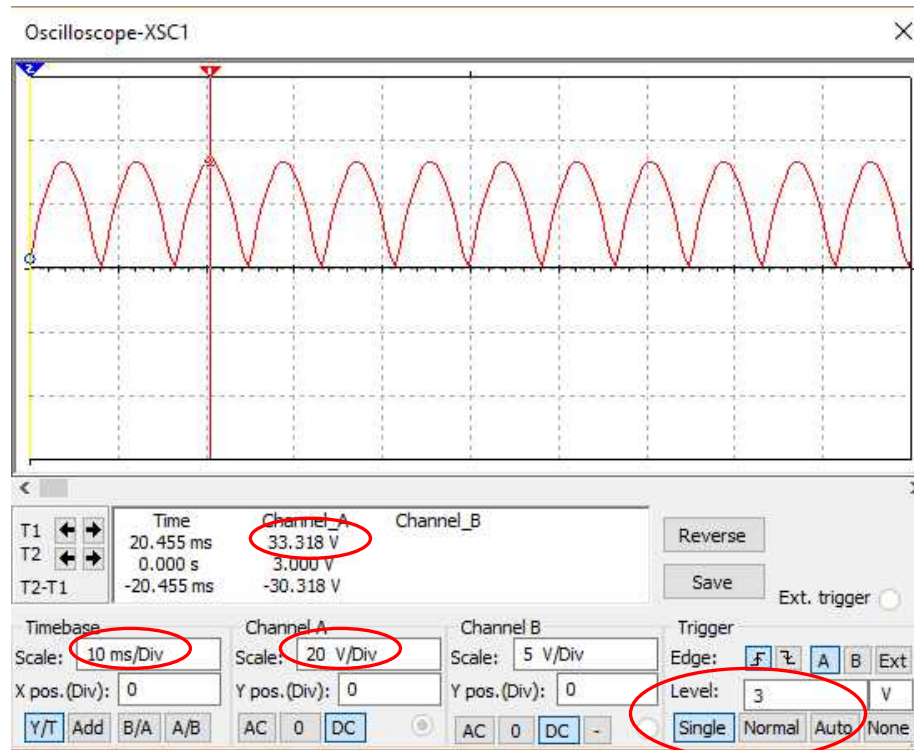


Figure 4-41.

To summarize the performance of the full-wave bridge rectifier, we illustrate the various waveforms associated with it in Fig. 4-42. Study them carefully. The values are determined in Example 4-8. The waveforms of the voltage across diodes D_2 and D_4 are identical, as are the voltage waveforms diodes D_1 and D_3 [see Fig. 4-42(c) and (d), respectively]. Since each *pair of diodes* (D_2 , D_4 and D_1 , D_3) conduct for only one-half of the secondary voltage waveform on alternate half-cycles, their current waveforms are as shown in Fig. 4-42(e) and (f). The voltage across R_L and the current through it are included in Fig. 4-42(g) and (h), respectively. Again, note the average current ($I_{D(AV)}$) through the diodes is one-half of the average DC load current I_{DC} .

³⁶ Feel free to play and explore. You cannot hurt Multisim and can gain a feel for the oscilloscope. This can minimize frustration and embarrassment in the laboratory.

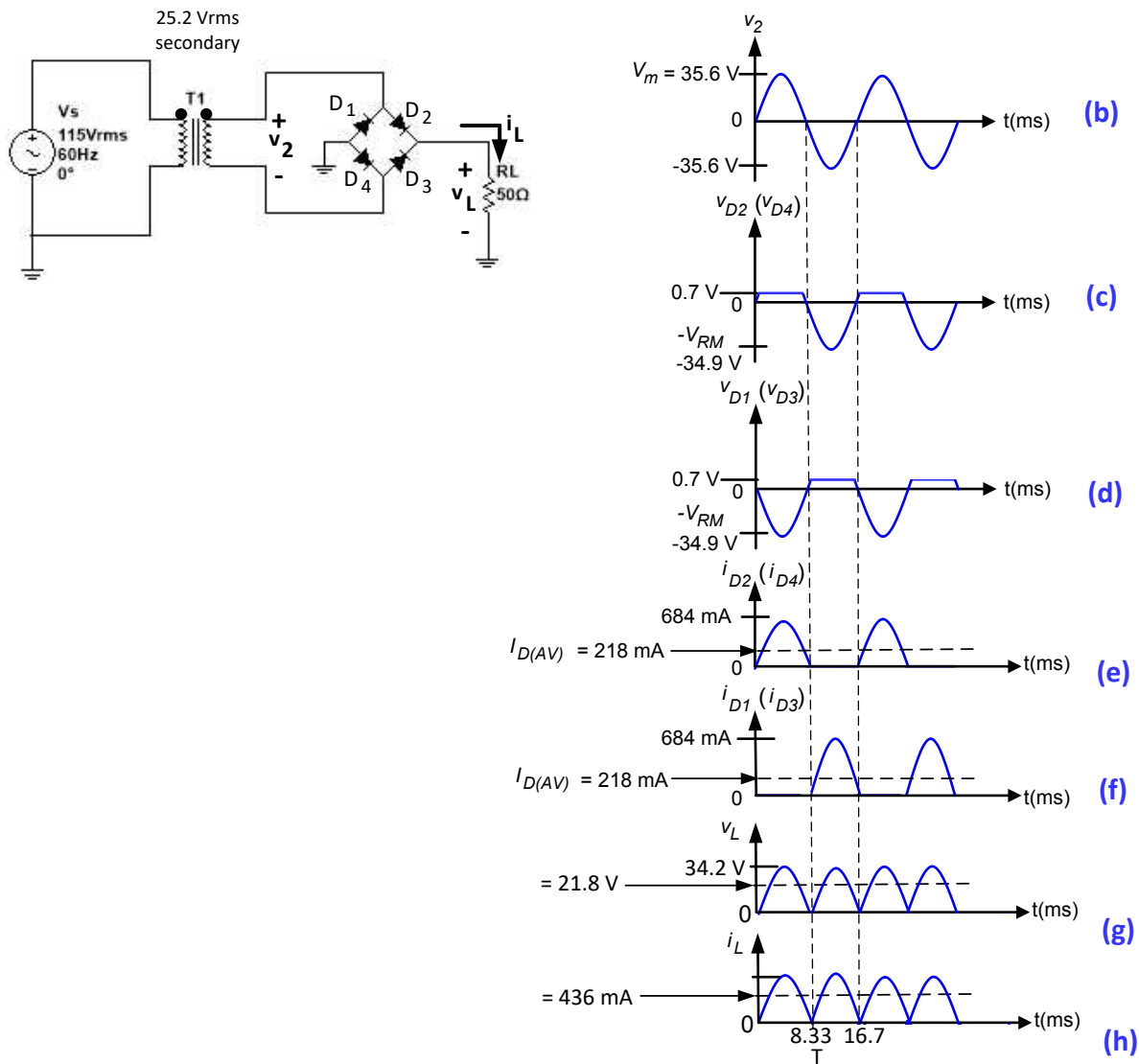


Figure 4-42.

4-9 Dual-Complementary Full-Wave Rectifiers

In many electronic circuits, a dual-polarity DC power supply is required. In Section 3-1 we examined the biased-diode clipper circuit [see Fig. 3-3(a)]. Basically, the DC power requirement involves two DC voltage sources. One produces a positive output voltage with respect to ground, while the other delivers a negative voltage with respect to ground. This can be modeled as illustrated in Fig. 4-43. We have two DC power supplies in series with the ground defined to be at the positive-to-negative connection point.

Dual-Complementary DC Power Supply

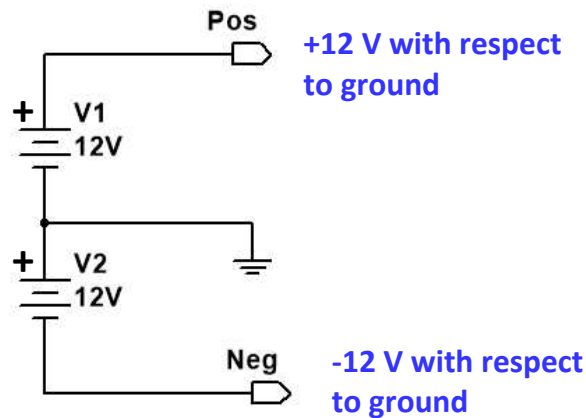


Figure 4-43.

The dual-complementary full-wave rectifier can serve as the front end of a dual-polarity DC power supply. In Fig. 4-44 we see we have two full-wave rectifier circuits that use center-tapped transformers. One provides a positive output while other produces a negative output. If the DC power supplies do *not* need to be isolated from one another, they can share the *same* center-tapped transformer.

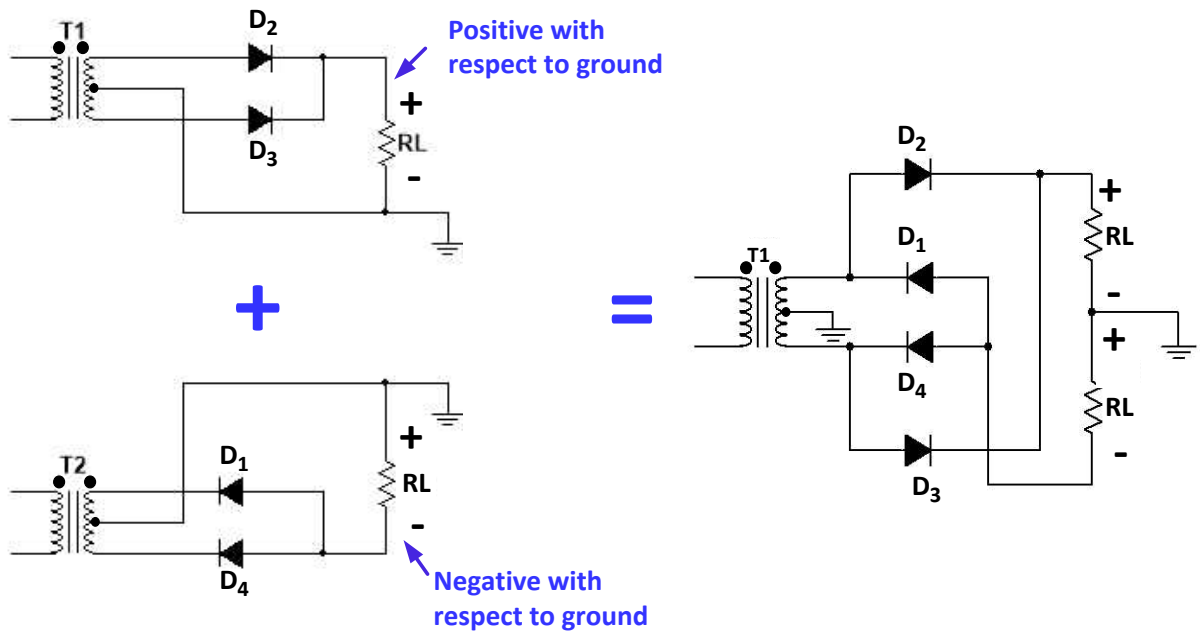


Figure 4-44.

It is possible to redraw the circuit in Fig. 4-44 [which has been repeated in Fig. 4-45(a)] to place the four rectifier diodes in the shape of a full-wave bridge as shown in Fig. 4-45. (You are encouraged to verify this.) Placing the diodes in the shape of a bridge suggests the full-wave bridge packages shown in Fig. 4-37 can also be used here.

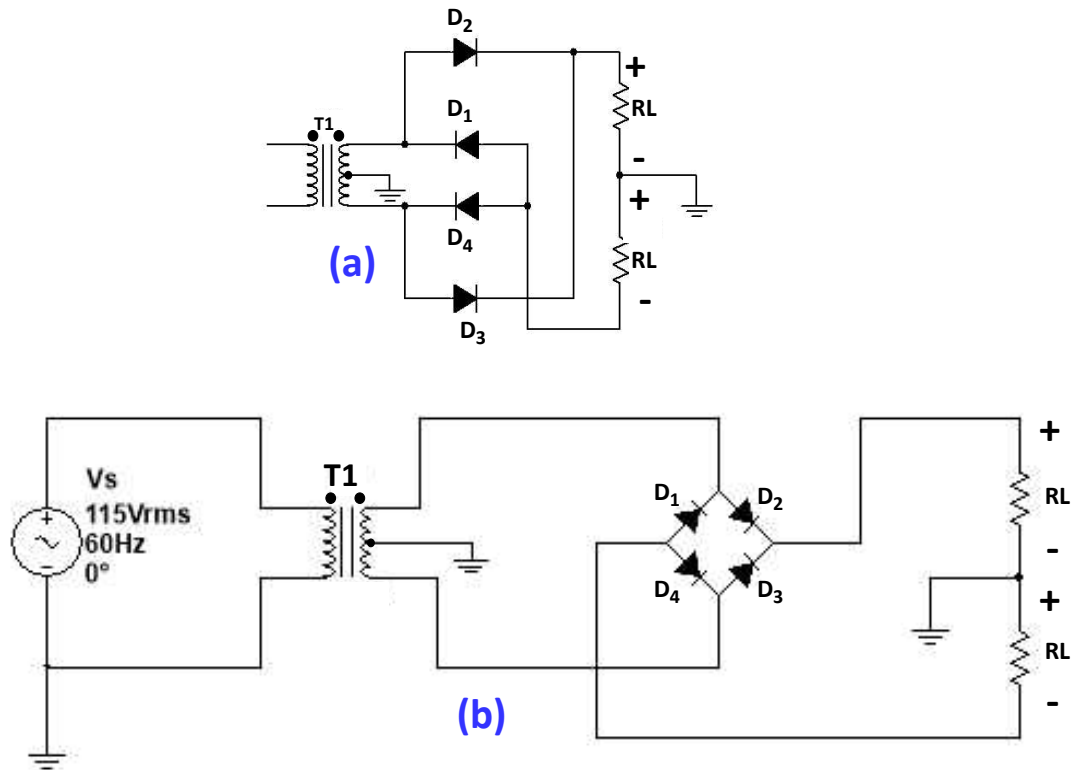


Figure 4-45.

4-10 Filter Capacitor Considerations

Pulsating DC is not suitable for most electronic systems. The problem is that even though we have an average value, the waveform amplitude varies and goes to *zero* instantaneously. For example, with a power-line frequency of 60 Hz and full-wave rectification, we have pulsating DC with a frequency of 120 Hz. If this were used to power an audio amplifier system, a very loud 120-Hz hum would be present at its output, and any audio input would be distorted severely. The DC must be relatively constant. Therefore, the output of the rectifier stage must be filtered or smoothed. The most elementary power supply filter consists of a single capacitor placed across the output of the rectifier in parallel with the load (see Fig. 4-46).

The strategy behind this scheme is based on two elementary circuit concepts. First, *capacitors oppose a change in their terminal voltage*, and second, *circuit elements in parallel experience the same voltage*. Subsequently, the capacitor will tend to smooth out the pulsating DC voltage delivered to the load.

Because this approach is very straight-forward, it is often called a *simple capacitor filter*. While other filter approaches using inductors, resistors, and additional capacitors are possible, their application is largely relegated to history books. They are too heavy and too expensive for modern applications.³⁷

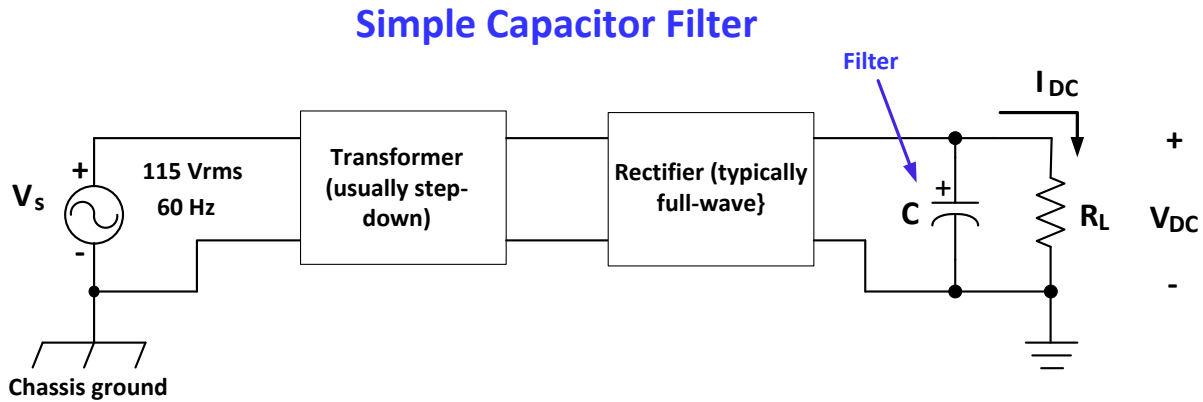


Figure 4-46.

The filter capacitor reduces the variation in the DC applied to the load. Any variation that remains is called “ripple”. To reduce the ripple, large values of filter capacitors are often required. (This will be explained further in Section 4-11.) Consequently, the filter capacitors incorporated in the design of DC power supplies are typically electrolytic capacitors. ***The key advantage provided by electrolytic capacitors is they offer large capacitance values for a relatively small physical size when compared to other types of capacitors.*** Two basic types of electrolytic capacitors are *aluminum* and *tantalum*. Let us examine some of the key attributes.

- Again, electrolytic capacitors offer large capacitance values for a relatively small physical size when compared to other types of capacitors.
- Electrolytic capacitors are *polarized*. [Note the plus (“+”) next to the capacitor symbol in Fig. 4-46]. This means one end must always be more positive than its other end. If the polarity is inadvertently reversed or if we place an AC voltage across them, the capacitor can be damaged severely, or even explode.
- Aluminum electrolytic capacitors are more common because they are available with voltage ratings that range from 2 to 700 V. Tantalum electrolytic capacitors offer superior characteristics, but have lower voltage ratings – typically, 4 to 50 V. (Tantalum capacitors also tend to be more expensive.)

³⁷ These other filters are called “L-input”, R-C Pi”, and “L-C Pi”. These filters tend to be bulky and heavy for DC power supplies operated from a 60 Hz power line.

- Equation 4-26 describes the physical construction of a capacitor.

$$C = \epsilon \frac{A}{d} \quad (4-26)$$

C is the capacitance in farads, ϵ (Greek letter epsilon) is the dielectric constant in farads per meter, A is the plate area in meters², and d is the distance between the plates in meters.

An aluminum electrolytic capacitor achieves a large capacitance by etching billions of tunnels in its aluminum plate to increase its surface area³⁸. The distance between the plates is made very small by using an electro-chemical reaction in its liquid electrolyte to form a very thin (e.g., 1 μm) oxide layer to serve as its dielectric. The liquid electrolyte has a very large dielectric constant and serves as the plate opposite the aluminum plate.

While tantalum electrolytic capacitors are available with liquid electrolytes, most are completely solid. In this case manganese dioxide is used as the dielectric. Because its solid dielectric is very thin and has a high-dielectric constant, solid tantalum capacitors offer large values of capacitance.

- Ideal insulators have infinite resistance and pass no current. However, the insulating material used as the dielectric in electrolytic capacitors is far from ideal and will permit a small **leakage current** to flow. The leakage current is on the order of microamperes for aluminum electrolytic capacitors and is even smaller for tantalum electrolytic capacitors. The leakage current is often modeled by using a large-valued (many megohms) **leakage resistance** in parallel with an ideal capacitor.

The maximum DC voltage that can be impressed across a capacitor without breaking down its dielectric, is called its **working voltage rating**. It is often denoted WVDC. The WVDC ratings of capacitors used in power supply filters must be greater than the peak rectified voltage (V_{dcm}) placed across them. To provide a 20% (minimum) safety margin, we offer the condition stated by Eq. 4-27.

$$\boxed{\text{WVDC} \geq 1.2V_{dcm}} \quad (4-27)$$

WVDC is the filter capacitor DC working voltage rating and V_{dcm} is the peak rectified voltage ($V_m - 0.7 \text{ V}$) for full-wave rectifiers using a center-tapped transformer (and dual-complementary full-wave rectifiers) and ($V_m - 1.4 \text{ V}$) for full-wave bridge rectifiers.

To conclude, we should also note that electrolytic capacitors also have a **ripple current rating**. This will be dealt with in Section 4-17. Some examples of electrolytic capacitors are given in Fig. 4-47.

³⁸ The insides of the tunnels have walls which add to the overall surface area of the plate.

Electrolytic Capacitor Case Styles

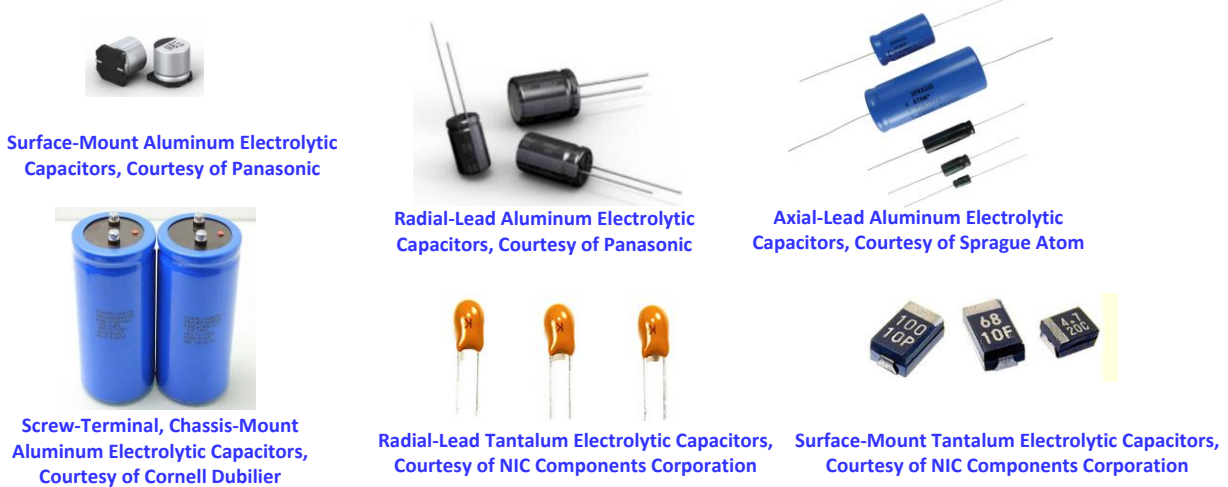


Figure 4-47.

4-11 Simple Capacitor Filters

To illustrate the effects of adding a filter capacitor, we study Fig. 4-48 carefully. In Fig. 4-48(a) have a full-wave rectifier using a center-tapped transformer driving a resistive load. As we saw in Section 4-7, a pulsating DC waveform will be developed across R_L , which has a peak rectified voltage V_{dcm} .

Recall that

$$V_{dcm} = V_m - 0.7 V$$

for this rectifier circuit. The average DC voltage across R_L has been shown to be

$$V_{DC} = 2 \frac{V_{dcm}}{\pi} \cong 0.637 V_{dcm}$$

and has been indicated in Fig. 4-48(a).

If we remove R_L temporarily and replace it with a filter capacitor C_1 , we have the situation shown in Fig. 4-48(b). From $t = 0$ to $t = T/4$, the capacitor will quickly charge to V_{dcm} . If the capacitor's leakage current is negligibly small, the capacitor will not discharge appreciably. Therefore, the voltage across it will remain at V_{dcm} . Note the rectified voltage has been shown in dashed lines for reference.

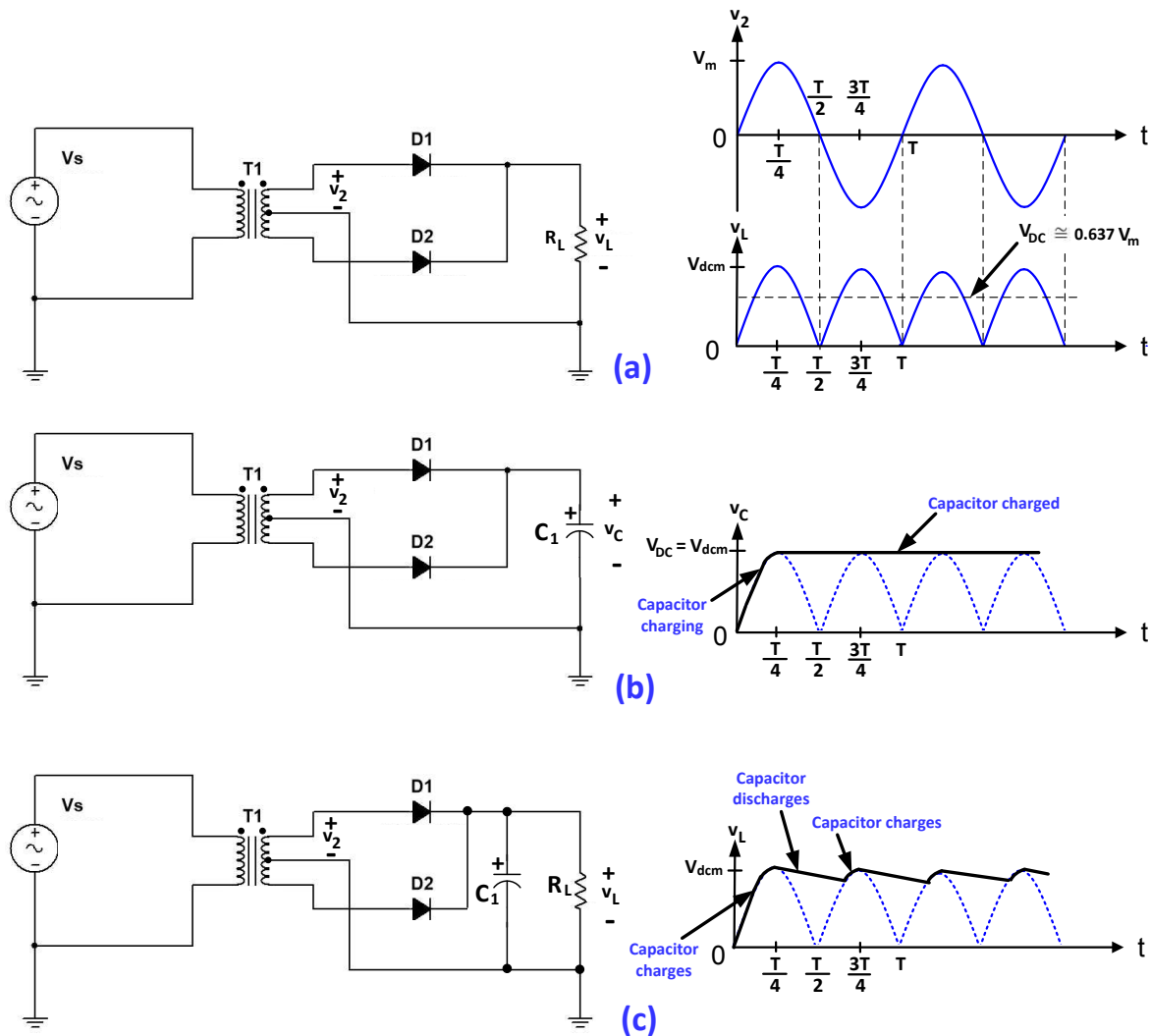


Figure 4-48.

The situation shown in Fig. 4-48(b) is *ideal*. The average DC voltage (V_{DC}) has been *increased* from $0.637V_{dcm}$ to V_{dcm} , and the pulsating DC has been converted to a perfectly smooth or constant DC level. However, this only happens when there is *no* load connected across the capacitor.

Figure 4-48(c) depicts a more realistic situation. The load is connected across the filter capacitor C_1 . As before, the capacitor will to the peak rectified voltage quickly. Once this occurs, ***the rectified voltage*** (again shown in dashed lines) ***will decrease and both rectifier diodes will be nonconducting***. Subsequently, the capacitor will start to discharge through R_L . The capacitor will continue to discharge until the rectified voltage becomes large enough to cause one of the diodes to conduct. When this occurs, the capacitor will again charge rapidly to the peak value of the pulsating DC.

The key to understanding the waveform in Fig. 4-48(c) is to note ***the cathode ends of both diodes D_1 and D_2 are held positive by the filter capacitor C_1*** . Consequently, ***the only time diode D_1 or diode D_2 can conduct is when their anodes are more positive (by about 0.7 V) than their cathodes***. When either of the two diodes conduct, the capacitor will be recharged.

In Fig. 4-49 we see the voltage waveform across the load and the filter capacitor. The peak-to-peak ripple voltage shall be designated as $V_{r(p-p)}$. By inspection of Fig. 4-49 we see the instantaneous minimum voltage $V_{dc(min)}$ is given by Eq. 4-28.

$$V_{dc(min)} = V_{dcm} - V_{r(p-p)} \quad (4-28)$$

From our work in Section 4-4 and Figs. 4-10, 4-11, and 4-12, it should be clear the DC average level in Fig. 4-49 is given by Eq. 4-29.

$$V_{DC} = V_{dcm} - \frac{V_{r(p-p)}}{2} \quad (4-29)$$

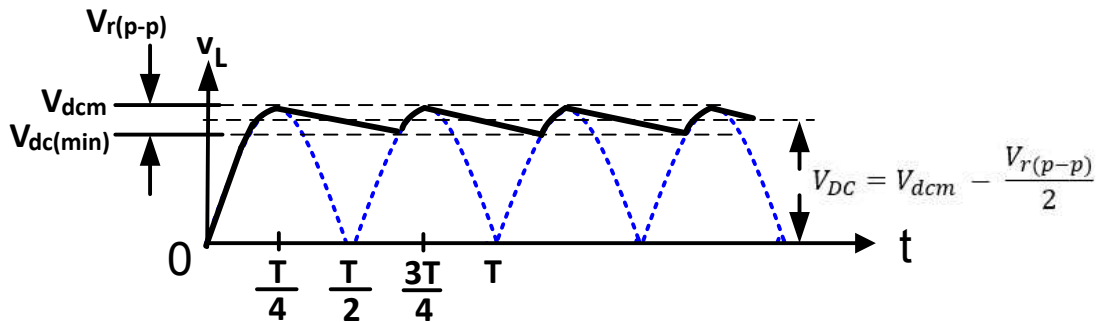


Figure 4-49.

Before we further quantify our analysis, let us first make some general observations (see Fig. 4-50).

- Generally, the *larger* the filter capacitor, the more charge it can hold and the less it will discharge. Hence, the peak-to-peak ripple will be *smaller*, and the DC level will be *closer* to V_{dcm} .
- The *smaller* the filter capacitor, the less charge it can hold and the more it will discharge. Consequently, the peak-to-peak ripple will be *larger*, and the DC level will decrease and *move toward the unfiltered DC level*.
- For a fixed value of filter capacitance, the peak-to-peak ripple will *decrease*, and the DC level will be *closer* to V_{dcm} , as the DC load current I_{DC} is *decreased*.
- For a fixed value of filter capacitance, the peak-to-peak ripple will *increase*, and the DC level will *move toward the unfiltered DC level*, as the DC load current I_{DC} is *increased*.

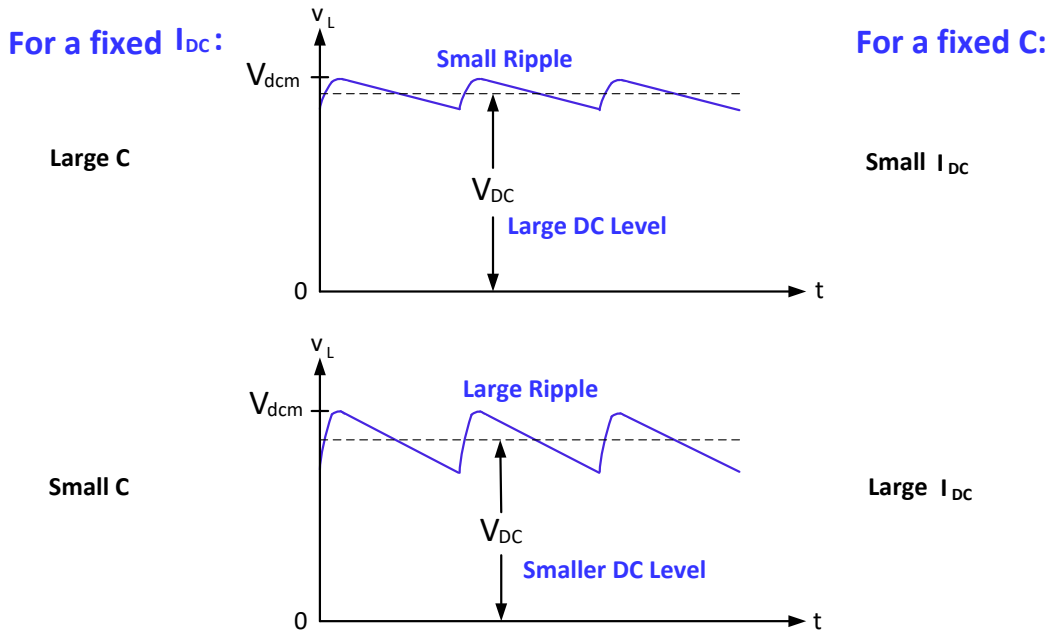
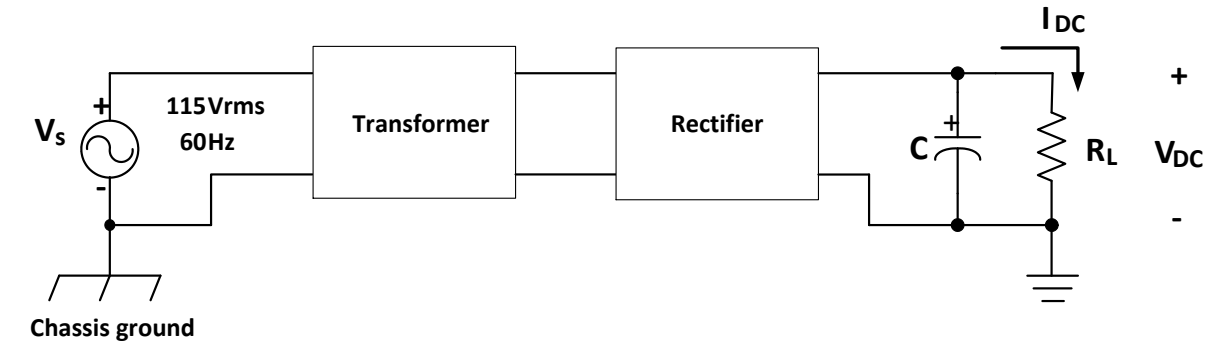


Figure 4-50.

4-12 Ripple Factor

The **ripple factor** (r) is a parameter often used to characterize DC power supply filter circuits. In Section 4-4 we examined average and rms values. A summary is provided in Fig. 4-51. Figure 4-51(a) reminds us the total waveform across the load can be decomposed into its DC component and its AC (ripple) component. Figure 4-51(b) shows the triangular approximation of the ripple voltage. This is done to simplify the mathematics.

The **period of the ripple waveform** has been denoted (T_r). By inspection we see that it is 8.33 ms (if we have a 60-Hz power-line frequency and full-wave rectification). The **ripple frequency** (f_r) is the reciprocal of its period.

$$f_r = \frac{1}{T_r} = \frac{1}{8.33 \text{ ms}} = 120 \text{ Hz}$$

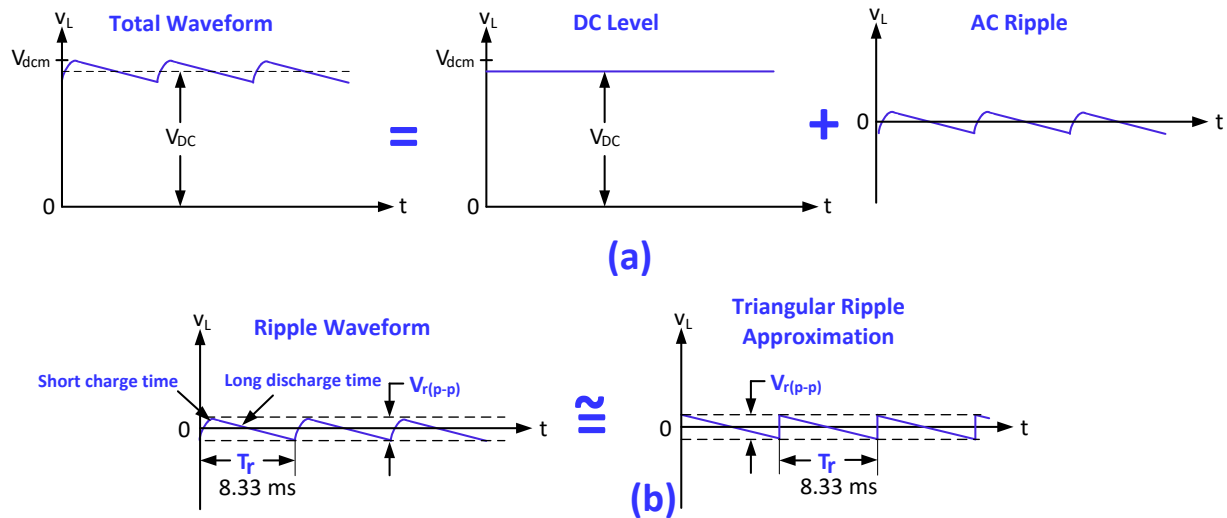


Figure 4-51.

The ripple factor (r) is defined by Eq. 4-30.

$$r = \frac{V_{r(rms)}}{V_{DC}} \quad (4-30)$$

From our work in Section 4-4, we recall the rms value of an AC waveform is equivalent to DC as far as power in a resistor is concerned. Our resistor is the load across the output of our DC power supply. Consequently, the ripple factor gives us a general idea as to the amount of AC power wasted as ripple compared to the useful DC power. Quite often, the ripple factor is expressed as a percentage as given by Eq. 4-31. A low value of $\%r$ is desired. In fact, **the ideal $\%r$ is 0%.**

$$\%r = \frac{V_{r(rms)}}{V_{DC}} \times 100\% \quad (4-31)$$

We can determine the **rms value of the ripple voltage** ($V_{r(rms)}$) by using the relationship provided in Fig. 4-15(c) for a triangle wave.

$$V_{rms} = \frac{V_m}{\sqrt{3}}$$

Applying this relationship to the triangle waveform in Fig. 4-51(b), leads us to Eq. 4-32.

$$V_{r(rms)} = \frac{V_m}{\sqrt{3}} = \frac{V_{r(p-p)}/2}{\sqrt{3}} = \frac{V_{r(p-p)}}{2\sqrt{3}} \quad (4-32)$$

Example 4-9. Analyze the rectifier circuit block diagram shown in Fig. 4-50. The total waveform across the load appears as shown in Fig. 4-51(a). The peak rectified voltage (V_{dcm}) across the load is 18 V. The peak-to-peak ripple voltage $V_{r(p-p)}$ is 2 V. Find $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the %r, and the required WVDC rating for the capacitor.

Solution: The quantities will be determined using the order in which they were requested. First, we find $V_{dc(min)}$ by using Eq. 4-28.

$$V_{dc(min)} = V_{dcm} - V_{r(p-p)} = 18 \text{ V} - 2 \text{ V} = 16 \text{ V}$$

We use Eq. 4-29 to determine V_{DC} .

$$V_{DC} = V_{dcm} - \frac{V_{r(p-p)}}{2} = 18 \text{ V} - \frac{2 \text{ V}}{2} = 17 \text{ V}$$

The rms value of the ripple voltage is determined by using Eq. 4-32.

$$V_{r(rms)} = \frac{V_{r(p-p)}}{2\sqrt{3}} = \frac{2 \text{ V}}{2\sqrt{3}} = 0.577 \text{ Vrms}$$

Equation 4-31 supplies us with the ripple factor percentage.

$$\%r = \frac{V_{r(rms)}}{V_{DC}} \times 100\% = \frac{0.577 \text{ Vrms}}{17 \text{ V}} \times 100\% = 3.39\%$$

The minimum working DC voltage rating for the filter capacitor is determined by Eq. 4-27.

$$\text{WVDC} \geq 1.2V_{dcm} = (1.2)(18\text{V}) = 21.6\text{V}$$

The capacitor's voltage rating should be at least 21.6 V. A standard value is 25 V, which is more than adequate.

4-13 Light-Loading Constraint

To analyze (and design) simple capacitor filters, we need to determine V_m , V_{dcm} , $V_{r(p-p)}$, and V_{DC} in terms of I_{DC} and C . We develop an equation for $V_{r(p-p)}$ in Section 4-14. To minimize ripple and keep the mathematics straightforward, we must ensure the filter is **lightly loaded**.

If a simple capacitor is lightly loaded, the average DC voltage will be very close to V_{dcm} , and the triangular ripple approximation will be valid.

If the filter is not lightly loaded, our approximations will degrade. The mathematics required to improve accuracy is very involved. Most engineers and technicians will then rely on computer simulation.

For light loading, the minimum value of V_{DC} is given by Eq. 4-33.

For light loading: $V_{DC} \geq 0.9V_{dcm}$

(4-33)

4-14 Ripple Voltage Equation

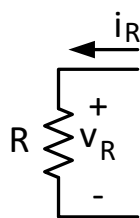
If we develop an equation for the peak-to-peak ripple voltage ($V_{r(p-p)}$) for a lightly loaded filter capacitor, the analysis of the filter capacitor becomes relatively simple. We remember a capacitor opposes a change in its terminal voltage with respect to time. Using calculus notation, we offer the mathematical definition provided by Eq. 4-34.

The capacitor current is i_C , the effective current through the capacitor, C is its capacitance, v_C is the voltage across the capacitor, and d/dt is calculus notation for a change in one quantity with respect to time.

$$\boxed{i_C = C \frac{dv_C}{dt}} \quad (4-34)$$

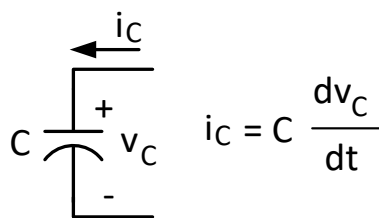
We will not use Eq. 4-34 directly. However, it is important that we are familiar with its meaning. In differential calculus statements like Eq. 4-34, the change in the voltage is taken to be infinitesimally small (approaching zero) with respect to an infinitesimally small change in time. Before we proceed further, consider Fig. 4-52. Figure 4-52(a) reminds us of the passive device convention. A resistor is a *passive* device so conventional current enters its positive terminal. We offer a simple definition: **Active devices are net suppliers of energy while passive devices are not.** Figure 4-52(b) shows us that when a capacitor is charging, conventional current enters its positive terminal just like a resistor. The capacitor stores electrical energy in an electric field. In Fig. 4-52(c) we see a capacitor that is discharging so conventional current (i) is leaving its positive terminal. It is supplying energy (temporarily). If we place a minus sign in front of the current i , its direction is reversed. So, a statement like $i_C = -i$ should make sense. **A capacitor is a passive device just like a resistor.** A capacitor can only return the energy it has received so it is *not* a net supplier of energy.

Passive Device Convention:
Current flows into the positive terminal.



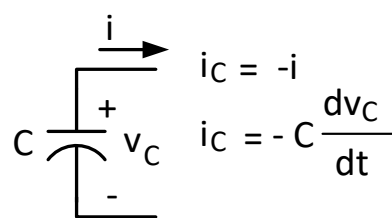
(a)

Capacitor charging



(b)

Capacitor discharging



(c)

Figure 4-52.

If we permit the change in voltage and current to be *small, but finitely large*, we may use the delta (Δ) notation as employed by Eq. 4-35.

$$\boxed{i_C \cong C \frac{\Delta v_C}{\Delta t}} \quad (4-35)$$

In Fig. 4-53 we see the filter capacitor is being discharged by a constant DC load current (I_{DC}). Since the current leaves the positive terminal of the capacitor, we must place a minus sign in front of Eq. 4-36.

$$\boxed{i_C \cong -C \frac{\Delta v_C}{\Delta t}} \quad (4-36)$$

If a capacitor is discharged by a constant current, its voltage decreases linearly. In Fig. 4-53 we see the voltage decreases linearly from the peak rectified voltage V_{dcm} to the minimum instantaneous voltage $V_{dc(min)}$. This is the change in the capacitor voltage Δv_C . This change in voltage occurs over a change in time Δt from t equals 0 until t reaches the period of the ripple waveform T_r . We substitute these observations into Eq. 4-36.

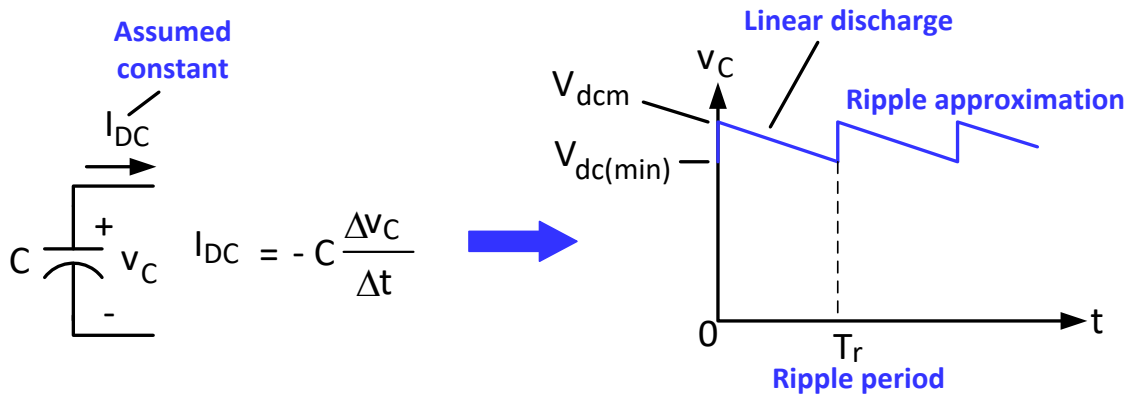


Figure 4-53.

$$I_{DC} = -C \frac{\Delta v_C}{\Delta t} = -C \frac{V_{dc(min)} - V_{dcm}}{T_r - 0}$$

Next, we distribute the minus sign.

$$I_{DC} = -C \frac{V_{dc(min)} - V_{dcm}}{T_r - 0} = C \frac{V_{dcm} - V_{dc(min)}}{T_r}$$

We factor out the reciprocal of the period of the ripple T_r and recall the reciprocal of the period produces the ripple frequency f_r .

$$I_{DC} = C(V_{dcm} - V_{dc(min)})(f_r)$$

If we look at Fig. 4-49, we can see the difference between V_{dcm} and $V_{dc(min)}$ is equal to the peak-to-peak ripple voltage $V_{r(p-p)}$. Substitution produces the result below:

$$I_{DC} = CV_{r(p-p)}f_r$$

Solving for the peak-to-peak ripple voltage produces Eq. 4-37.

$$\boxed{V_{r(p-p)} = \frac{I_{DC}}{f_r C}} \quad (4-37)$$

$V_{r(p-p)}$ is the peak-to-peak ripple voltage across a lightly loaded filter capacitor. I_{DC} is the load current, C is the filter capacitor, and f_r is the ripple frequency. Equation 4-37 gives us a lot of insight. The peak-to-peak ripple voltage is directly proportional to the DC load current. It is inversely proportional to the size of the filter capacitor. It is also inversely proportional to the ripple frequency, which explains why a full-wave rectifier with its ripple frequency of 120 Hz is twice as good as a half-wave rectifier with its ripple frequency of 60 Hz.

Example 4-10. Analyze the DC power supply shown in Fig. 4-54. The DC load current (I_{DC}) is 150 mA. Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the % r , and the required WVDC rating for the capacitor. Verify we have a lightly loaded filter.

Solution: The quantities will be determined using the order in which they were requested. Since we have a full-wave rectifier using a 36-Vrms center-tapped transformer, $V_2 = 36 \text{ Vrms}/2 = 18 \text{ Vrms}$.

$$V_m = \sqrt{2}V_2 = \sqrt{2}(18 \text{ Vrms}) = 25.5 \text{ V}$$

Since the diodes alternate in conduction, we only have one diode voltage drop with which to contend. Equation 4-21 gives us the peak rectified voltage.

$$V_{dcm} = V_m - 0.7 \text{ V} = 25.5 \text{ V} - 0.7 \text{ V} = 24.8 \text{ V}$$

We use Eq. 4-37 to determine the peak-to-peak ripple voltage.

$$V_{r(p-p)} = \frac{I_{DC}}{f_r C_1} = \frac{150 \text{ mA}}{(120 \text{ Hz})(470 \mu\text{F})} = 2.66 \text{ V p-p}$$

Equation 4-28 provides us with the minimum instantaneous voltage.

$$V_{dc(min)} = V_{dcm} - V_{r(p-p)} = 24.8 \text{ V} - 2.66 \text{ V} = 22.1 \text{ V}$$

We use Eq. 4-29 to find V_{DC} .

$$V_{DC} = V_{dcm} - \frac{V_{r(p-p)}}{2} = 24.8 \text{ V} - \frac{2.66 \text{ V}}{2} = 23.5 \text{ V}$$

The rms value of the ripple voltage is determined by using Eq. 4-32.

$$V_{r(rms)} = \frac{V_{r(p-p)}}{2\sqrt{3}} = \frac{2.66 \text{ V}}{2\sqrt{3}} = 0.768 \text{ Vrms}$$

Equation 4-31 supplies us with the ripple factor percentage.

$$\%r = \frac{V_{r(rms)}}{V_{DC}} \times 100\% = \frac{0.768 \text{ Vrms}}{23.5 \text{ V}} \times 100\% = 3.27\%$$

The minimum working DC voltage rating for the filter capacitor is determined by Eq. 4-27.

$$WVDC \geq 1.2V_{dcm} = (1.2)(24.8V) = 29.8V$$

The capacitor's voltage rating should be at least 29.8 V. A standard value is 35 V, which is more than adequate. We verify we have a lightly loaded filter capacitor by using Eq. 4-33.

$$V_{DC} \geq 0.9V_{dcm} = (0.9)(24.8V) = 22.3V$$

The DC voltage of 23.5 V exceeds the 22.3-V minimum requirement.

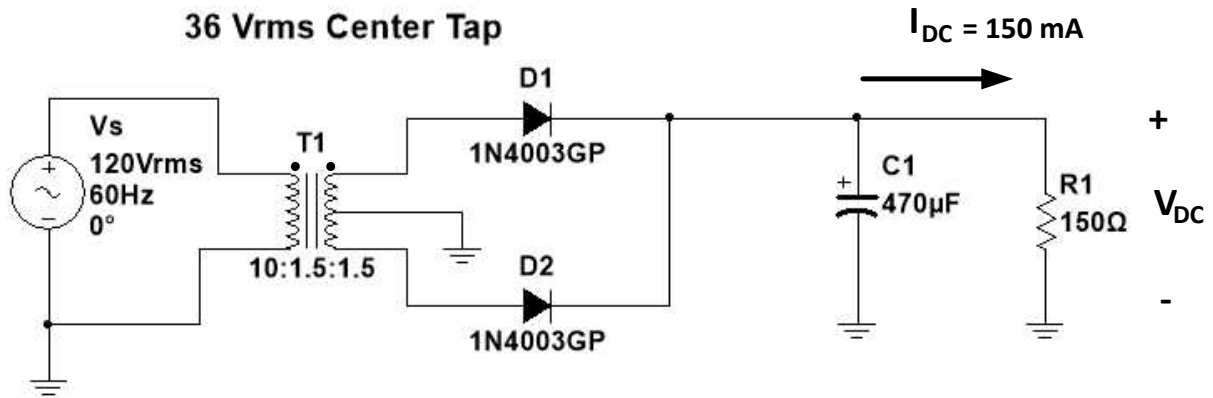


Figure 4-54.

Using Multisim to Analyze the DC Power Supply with a Simple Capacitor Filter

We shall use Multisim to verify the quantities we calculated in Example 4-10. Figure 4-55 indicates we are using two Multimeters (MM). One is being used to verify the DC voltage while the other is measuring the rms value of the AC ripple. *When a Multisim MM is configured to measure AC, it will ignore any DC level and display the true rms value of the AC component.*

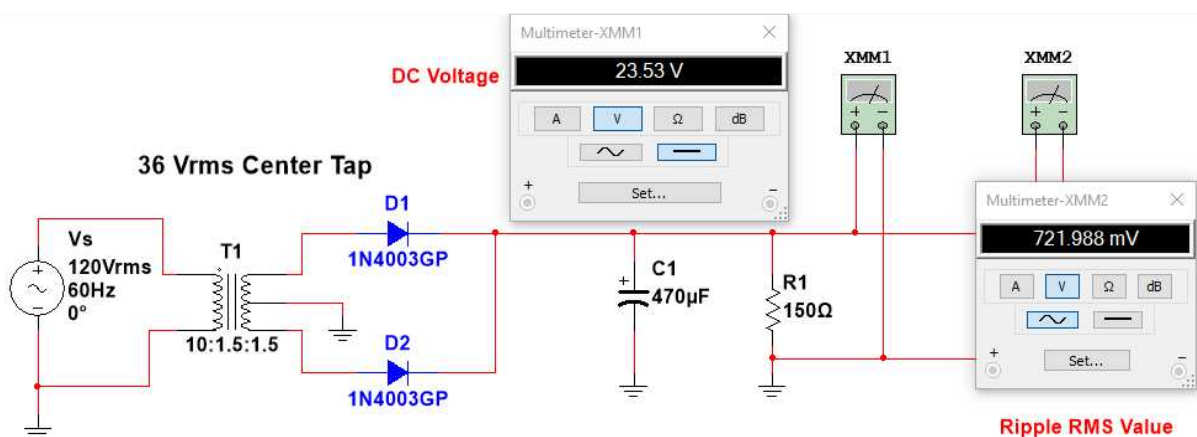


Figure 4-55.

The DC voltage agrees very closely with our calculated value. The rms value of 722 mVrms is about 6% lower than our calculated value of 768 mVrms. Next, we use a two-channel oscilloscope to examine the output voltage across the load. Note that we are using the voltage source to serve as an external trigger [see Fig. 4-56]. Observe we have AC ripple riding on the DC level. We drag the cursors from left and position them as shown in Fig. 4-57.

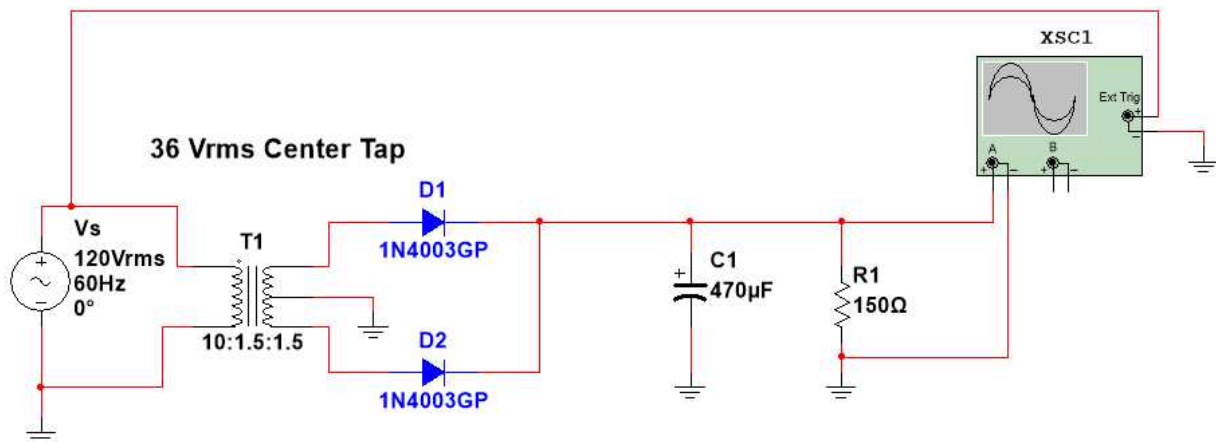


Figure 4-56.

Cursor 2 (blue) is being used to measure V_{dc} and indicates 24.6 V, which is about 0.8% lower than our calculation of 24.8 V. Cursor 1 (red) is positioned to measure $V_{dc(min)}$ and yields 22.4 V, which is approximately 1% higher than our calculated value of 22.1 V. Note the oscilloscope settings. We are calling for a single sweep.

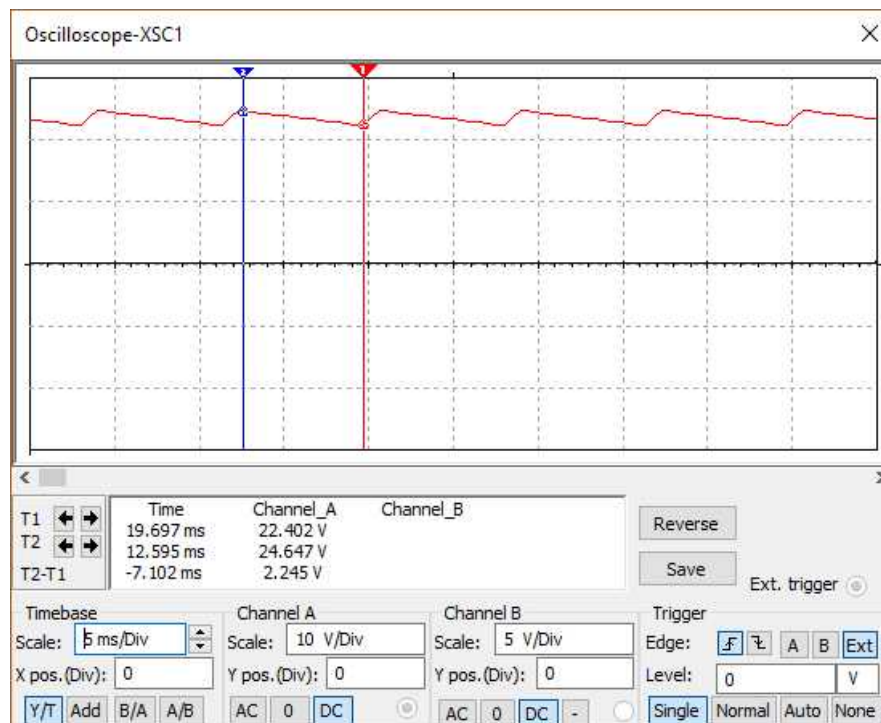


Figure 4-57.

To examine the AC ripple, *we AC couple the oscilloscope. This blocks the DC level.* This allows us to increase the vertical sensitivity, so we can examine the ripple closely [see Fig. 4-58].

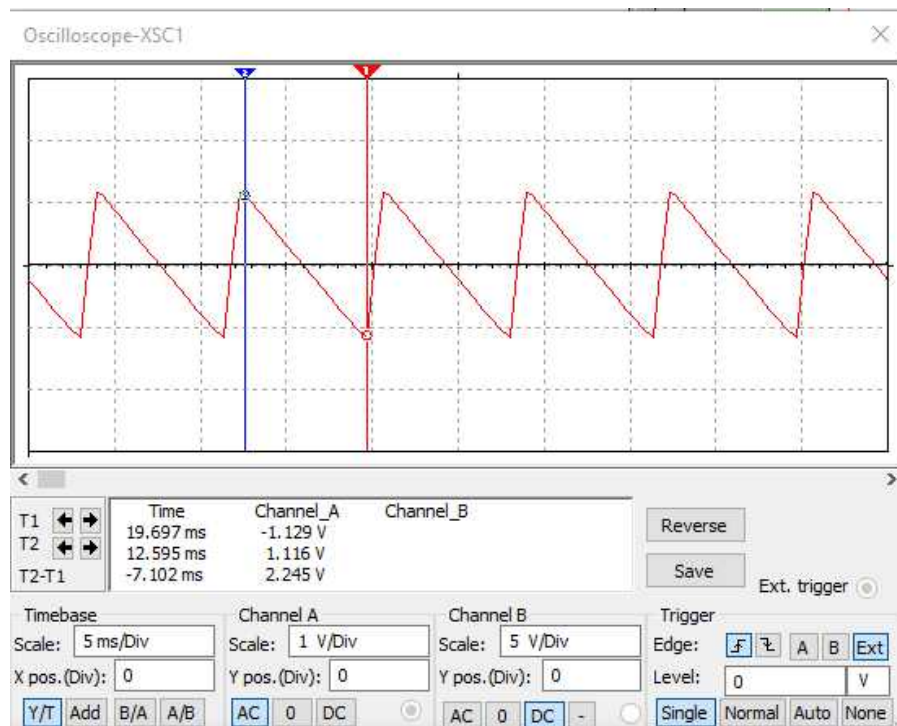


Figure 4-58.

We note the ripple waveform is triangular. Its peak-to-peak value is 2.25 Vp-p. This is about 15% lower than our calculated value of 2.66 Vp-p. Our calculations seem reasonably close to the simulation results.

4-15 Rectifier Average and Peak Repetitive Currents

Now that we have investigated simple capacitor filters, we need to consider their effect on the diode rectifiers. Specifically, we are concerned about the rectifier average currents $I_{D(AV)}$, and the rectifier peak currents $I_{D(PK)}$ that occur. This background will help us understand diode current ratings (and their derating), transformer secondary current ratings, and capacitor ripple current ratings.

As we saw previously, each diode in a full-wave rectifier using a center-tapped transformer, and each diode *pair* in a full-wave bridge rectifier must pass an average forward current equal to *one-half* of the DC load current (I_{DC}). The rectifier average current ($I_{D(AV)}$) is stated by Eq. 4-38.

$$I_{D(AV)} = 0.5I_{DC} \quad (4-38)$$

Manufacturers typically denote the rectifier diode average forward current *rating* as I_o or $I_{F(AV)}$. The average forward current rating I_o should be greater than the actual average forward current $I_{D(AV)}$ the diodes must pass.

To provide a 20% safety margin, we offer Eq. 4-39.

$$I_o \geq 1.2I_{D(AV)} = (1.2)(0.5)I_{DC} = 0.6I_{DC}$$

$$\boxed{I_o \geq 1.2I_{D(AV)} = 0.6I_{DC}} \quad (4-39)$$

In addition to the average forward current, rectifier diodes must also pass much larger peak repetitive surge currents $I_{D(PK)}$ which occur each time the filter capacitor is recharged. It is very important to be able to determine $I_{D(PK)}$. Manufacturers often reduce (derate) the I_o specification on the basis $I_{D(PK)}/I_{D(AV)}$ ratio.

In Fig. 4-59 we see the repetitive surge currents can be monitored by using a small, current-sensing resistor.

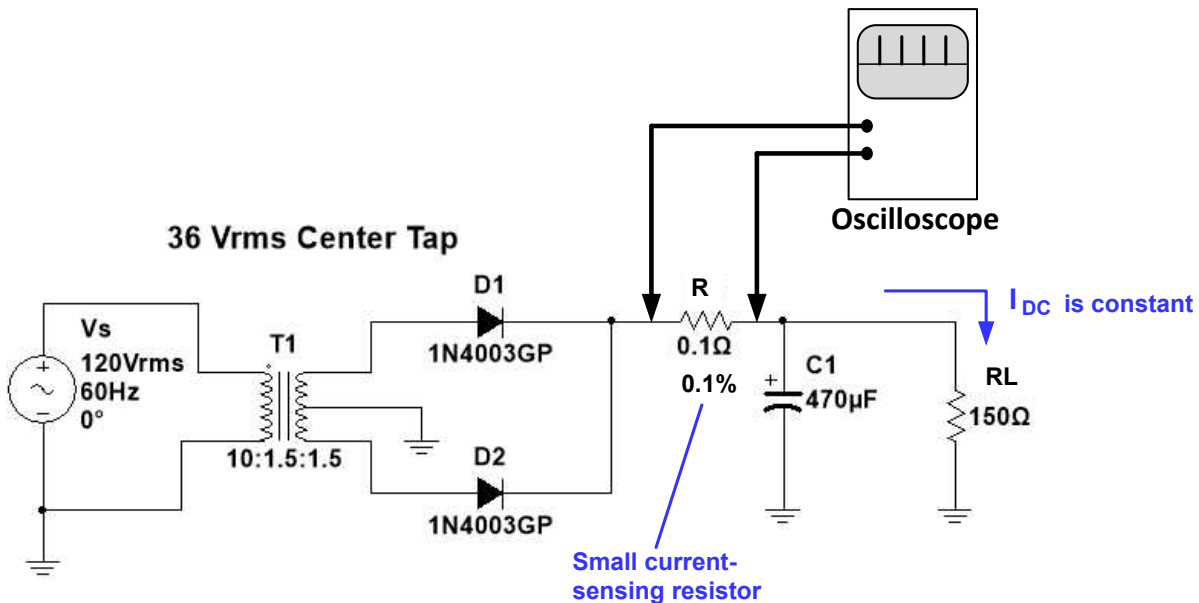
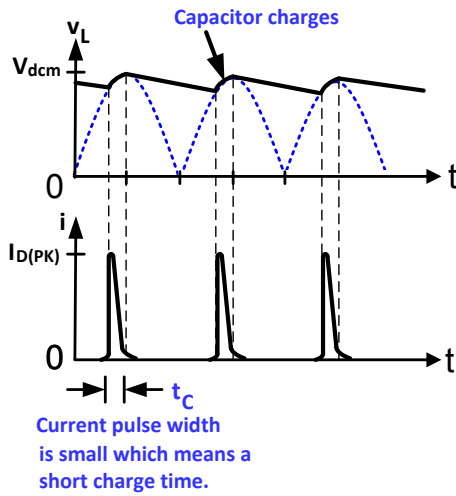


Figure 4-59.

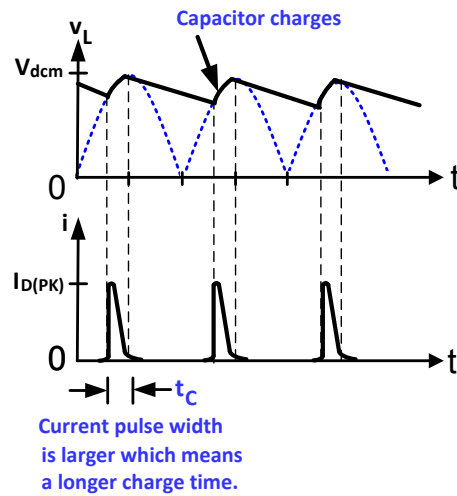
The larger the filter capacitor, the smaller the ripple, and the shorter the charge time. A short charge time will cause the peak repetitive current to be larger. (Since there is less time to recharge the filter capacitor, the current must be larger to replace the charge upon the capacitor.) This is shown in Fig. 4-60(a). If a smaller filter capacitor is used, the charge time will increase, the peak repetitive current will decrease, but the ripple will increase [see Fig. 4-60(b)].

Large C, Small Ripple, but Large Peak Current



(a)

Smaller C, Smaller Peak Current, but Larger Ripple

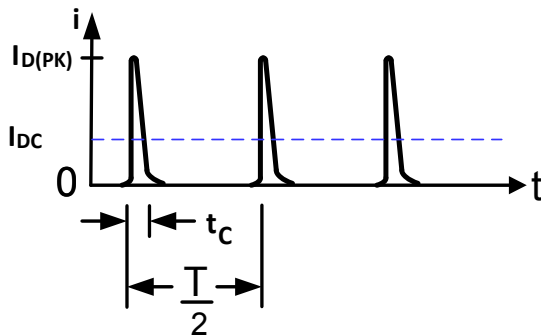


(b)

Figure 4-60.

In Fig. 4-61 we see the peak repetitive currents are highly nonlinear. To simplify our analysis, we shall assume their shape is approximately triangular (see Fig. 4-61). **If we assume the charge into the capacitor replaces the charge removed by the load, the average value of the current pulses will be equal to I_{DC} .** The triangular approximation has the same average value (ideally).

Peak Repetitive Surge Current



Triangular Approximation

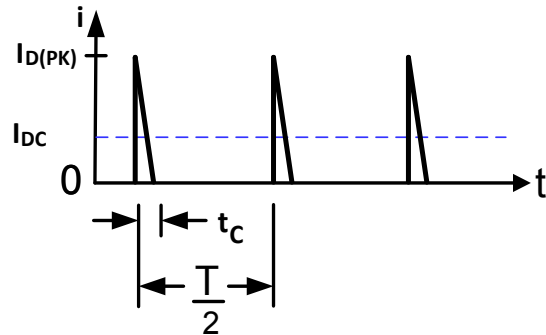


Figure 4-61.

The period T corresponds to the period of the power line frequency (f). The current pulses have one-half of the period, which means they occur at twice the frequency. (This is for full-wave rectification). We desire to find an equation for the average value of the current as it relates to the triangular approximation. We apply the techniques learned in Section 4-4.

The area of a triangle is $\frac{1}{2}$ base X height. The triangular approximation has a base equal to the charge time t_c and a height equal to the peak repetitive surge current $I_{D(PK)}$. Since the average value I_{DC} is the area divided by the time for one complete cycle, which is $T/2$, we obtain Eq. 4-40.

$$I_{DC} = \frac{1}{2} \frac{I_{D(PK)} t_c}{T/2} = \frac{I_{D(PK)} t_c}{T} \quad (4-40)$$

If we substitute $f = 1/T$, we have

$$I_{DC} = I_{D(PK)} t_c f$$

Solving for $I_{D(PK)}$ produces Eq. 4-41.

$$I_{D(PK)} = \frac{I_{DC}}{f t_c} \quad (4-41)$$

$I_{D(PK)}$ increases as the DC load current (I_{DC}) increases. It also increases as the charge time (t_c) becomes smaller. If we use the common North American power-line frequency (f) of 60 Hz, we have Eq. 4-42.

$$\text{For } f = 60\text{Hz: } I_{D(PK)} = \frac{I_{DC}}{60 t_c} \quad (4-42)$$

Next, we need to determine the charge time t_c . To find t_c we use Fig. 4-61 and a little trigonometry.

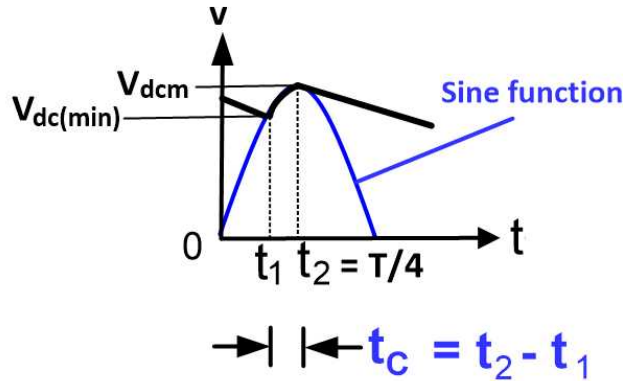


Figure 4-62.

The filter capacitor charges from t_1 to t_2 . The charge time t_c is the difference between these two points in time. Time t_2 occurs at $T/4$. This permits us to write Eq. 4-43.

$$t_c = \frac{T}{4} - t_1 \quad (4-43)$$

We have a sine function with a peak value of V_{dcm} , a frequency of 60 Hz, and we have an instantaneous voltage of $V_{dc(min)}$ at time t_1 . First, we write the *general equation* for the sine wave.

$$V_m \sin \omega t = v$$

We apply the conditions indicated in Fig. 4-62.

$$V_{dcm} \sin \omega t_1 = V_{dc(min)}$$

$$\sin \omega t_1 = \frac{V_{dc(min)}}{V_{dcm}}$$

We take the inverse sin (also called the arcsin) of both sides of the equation and solve for t_1 .

$$t_1 = \frac{1}{\omega} \sin^{-1} \frac{V_{dc(min)}}{V_{dcm}}$$

We substitute in $\omega = 2\pi f$ to get Eq. 4-44.

$$t_1 = \frac{1}{2\pi f} \sin^{-1} \frac{V_{dc(min)}}{V_{dcm}} \quad (4-44)$$

Assuming $f = 60$ Hz and substituting Eq. 4-44 into Eq. 4-43 yields Eq. 4-45.

$$\text{For } f = 60 \text{ Hz: } t_c = 4.17 \text{ ms} - 2.65 \sin^{-1} \frac{V_{dc(min)}}{V_{dcm}} \text{ ms} \quad (4-45)$$

To use Eq. 4-45 to find the charge time, it is critical to note the argument of the inverse sine is in *radians*. In simple terms, ***place your calculator in its radian mode of operation.***

Example 4-11. Continue the analysis of the DC power supply shown in Fig. 4-54. The DC load current (I_{DC}) is 150 mA. The DC power supply operates from a 60 Hz power line. In Example 4-10 we determined: $V_{dcm} = 24.8$ V, $V_{dc(min)} = 22.1$ V, $V_{DC} = 23.5$ V, and $V_{r(p-p)} = 2.66$ V_{p-p}.

Find $I_{D(AV)}$, I_o , $I_{D(PK)}$, and the $I_{D(PK)} / I_{D(AV)}$ ratio for the rectifier diodes.

Solution: We use Eq. 4-38 to find $I_{D(AV)}$.

$$I_{D(AV)} = 0.5 I_{DC} = (0.5)(150 \text{ mA}) = 75 \text{ mA}$$

Equation 4-39 provides the required average diode current rating that includes a 20% safety factor.

$$I_o \geq 1.2 I_{D(AV)} = 0.6 I_{DC} = (0.6)(150 \text{ mA}) = 90 \text{ mA}$$

We use Eq. 4-45 to find the filter capacitor charge time.

$$t_c = 4.17 \text{ ms} - 2.65 \sin^{-1} \frac{V_{dc(min)}}{V_{dcm}} \text{ ms} = 4.17 \text{ ms} - 2.65 \sin^{-1} \frac{22.1 \text{ V}}{24.8 \text{ V}} \text{ ms}$$

$$= 4.17 \text{ ms} - 2.915 \text{ ms}$$

$$= 1.255 \text{ ms}$$

Now we employ Eq. 4-42 to determine the peak value of the repetitive surge current.

$$I_{D(PK)} = \frac{I_{DC}}{60 t_c} = \frac{150 \text{ mA}}{(60)(1.255 \text{ ms})} = 1.99 \text{ A}$$

Now we calculate the $I_{D(PK)} / I_{D(AV)}$ ratio.

$$\frac{I_{D(PK)}}{I_{D(AV)}} = \frac{1.99 \text{ A}}{75 \text{ mA}} = 26.53$$

The peak currents through the diodes are about 27 times larger than their average currents.

Using Multisim to Analyze the Peak Repetitive Surge Currents

We construct the circuit using a current-sensing resistor as shown in Fig. 4-58. The Multisim circuit is provided in Fig. 4-62. The 0.1-Ω current-sensing resistor is monitored by the oscilloscope. ***In Multisim the oscilloscopes have differential inputs.*** That means the (virtual) oscilloscope input does not require a ground input connection. Commercial (real) oscilloscopes are typically referenced to ground. However, they can be configured to have a differential input.

The oscilloscope is using an *external* trigger input from the power line in this simulation. On-page connectors (e.g., “Line”) are used to minimize wiring.

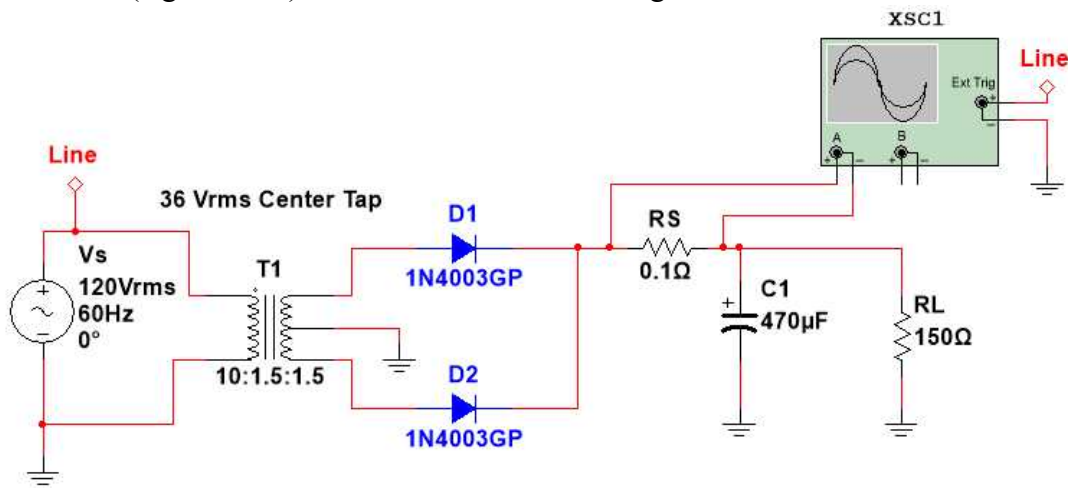


Figure 4-63.

The peak repetitive current pulses are shown on the screen (Fig. 4-64). These nonlinear transients are using a Multisim sampling algorithm. The sampling makes the pulses appear “ragged” and occasionally the peak is missed.

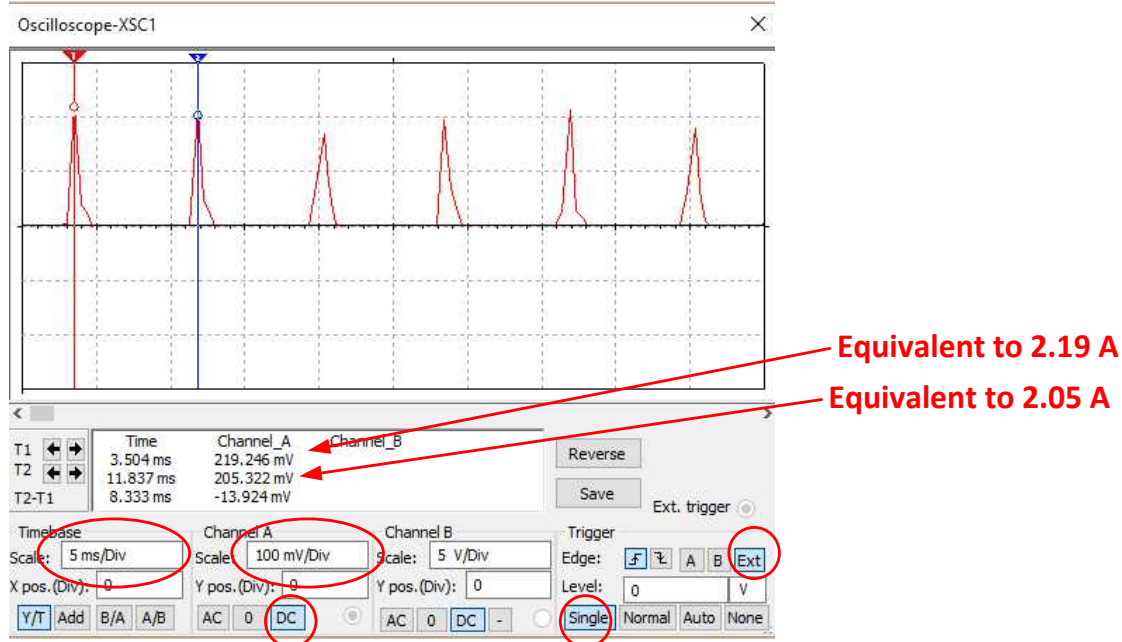


Figure 4-63.

In Example 4-11 we calculated a peak current of 1.99 A. The pulses on the oscilloscope appear to be close. Notice the amplitude setting is 100 mV per division, the time base is set to 5 ms per division, and channel A is direct coupled (DC). We are using an external trigger (Ext) and have selected a single (Single) sweep.

It should be noted the surge current has a frequency of 120 Hz. However, *because the diodes alternate in conduction, their individual surge currents have frequency of 60 Hz.*

4-16 Nonrepetitive Diode Surge Current

In addition to the repetitive surge currents through the rectifier diodes, the diodes must also pass a large **nonrepetitive surge current** when the power supply is first switched on. This nonrepetitive surge current $I_{D(SURGE)}$ occurs because the filter capacitor is uncharged initially. Since the capacitor has zero volts across it, and a capacitor opposes a change in voltage, it will appear as a *short circuit* when power is first applied.

When power is first applied, the instantaneous voltage could be as large as V_{dcm} . Only one diode in a full-wave rectifier using a center-tapped transformer, or one pair of diodes in a full-wave bridge rectifier will be conducting. If we model the transformer secondary as a voltage source, we have the equivalent circuit shown in Fig. 4-64(a). The second diode shown in the phantom box appears in the equivalent circuit of a full-wave bridge rectifier. Resistance R_2 represents the resistance of the secondary winding.

Since the capacitor is a short initially, both it and the load are *not* present in the circuit. Note the resistance of the diode(s) is significant in this analysis. In this case the resistance is the (small) bulk resistance of the semiconductor (r_B). The diode model consists of an ideal diode, a knee-voltage source, and the bulk resistance.

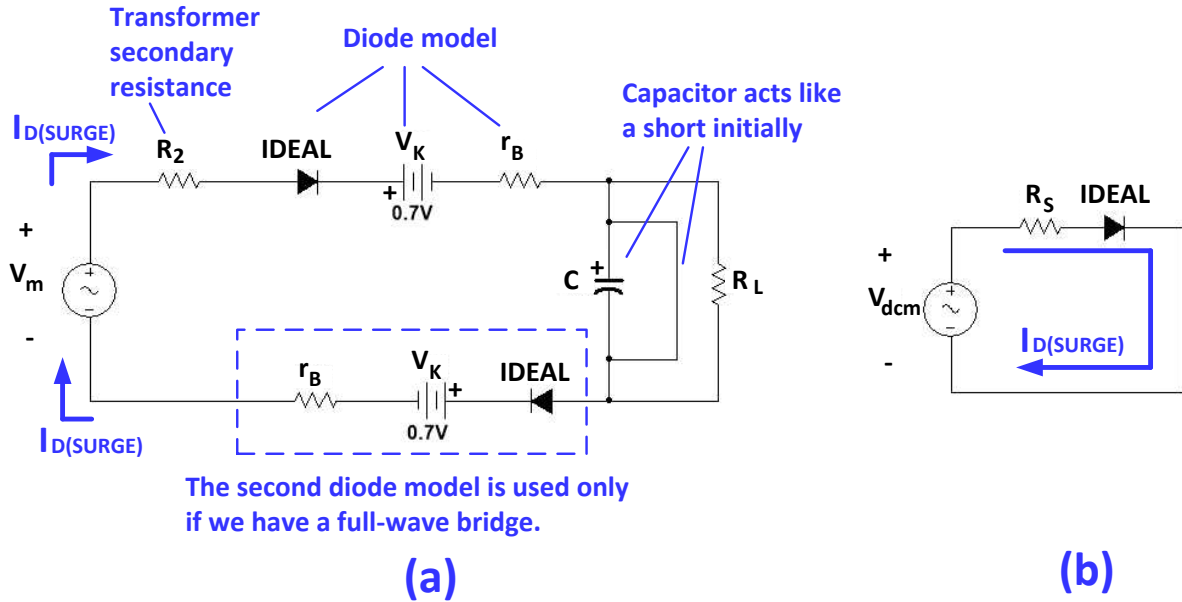


Figure 4-64.

Figure 4-64(b) shows the simplified equivalent circuit. The generator produces the peak rectified voltage and the total equivalent resistance is R_S . This resistance includes the transformer secondary resistance and the diode(s) bulk resistance. Since an ideal diode acts like a closed switch, only the generator voltage and the total equivalent resistance determine the surge current. Ohm's law produces Eq. 4-46.

$$I_{D(SURGE)} = \frac{V_{dcm}}{R_S} \quad (4-46)$$

Example 4-12. We continue the analysis of the DC power supply examined in Examples 4-10 and 4-11. Compute the nonrepetitive surge current ($I_{D(SURGE)}$) of the DC power supply shown in Fig. 4-56. The peak rectified voltage (V_{dcm}) is 24.8 V, the transformer secondary resistance (R_2) is 4.30 Ω , and the diode bulk resistance (r_B) is 0.2 Ω .

Solution: We calculate the total resistance R_S and then employ Eq. 4-46.

$$R_S = R_2 + r_B = 4.30 \, \Omega + 0.2 \, \Omega = 4.50 \, \Omega$$

$$I_{D(SURGE)} = \frac{V_{dcm}}{R_S} = \frac{24.8 \, V}{4.50 \, \Omega} = 5.51 \, A$$

The DC power supply is designed to supply a current of 150 mA, but the nonrepetitive surge current is much larger. Manufacturers provide a (nonrepetitive) surge current rating that is denoted as I_{FSM} . As a rough, but conservative guide, the surge current rating should be at least 20% greater than the surge current.

$$I_{FSM} \geq 1.2I_{D(SURGE)}$$

(4-47)

Example 4-12 presents an oversimplification. The transformer secondary resistance and the diode bulk resistance are usually *not* provided. The capacitor will start to charge immediately, which affects the analysis. The usual approach is to use a current-sensing resistor and a digital storage oscilloscope. Figure 4-65 is the same circuit used to monitor the peak repetitive surge current. However, the oscilloscope settings have been adjusted to permit us to capture the nonrepetitive surge current.

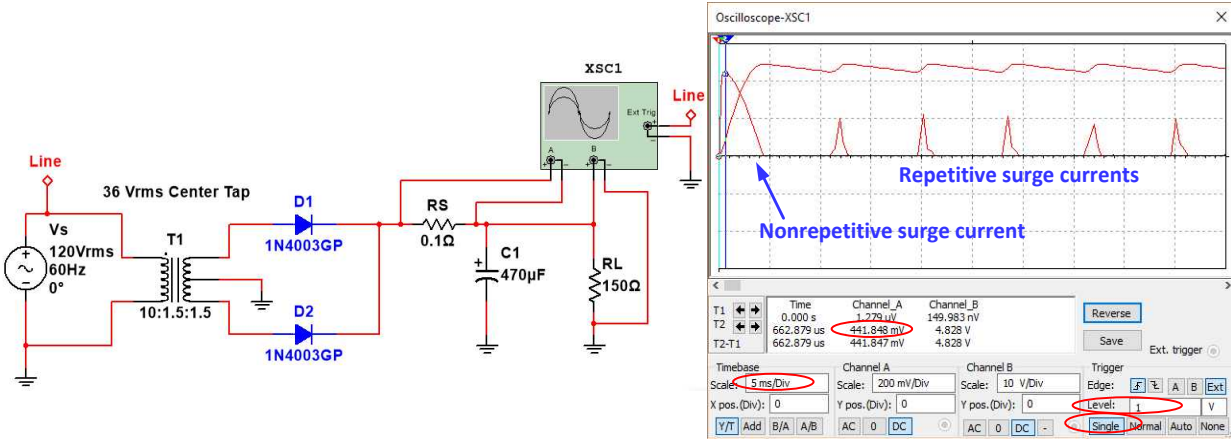


Figure 4-65.

At the far left of the oscilloscope screen we see the peak nonrepetitive surge current is about 4.42 A. Once the filter capacitor charges, we see the peak, repetitive surge currents have an amplitude of about 2 A as shown originally in Fig. 4-63.

In some larger I_{DC} designs, the current-sensing resistor must be much smaller (e.g., 0.01 Ω or less). An alternative is the use a clamp-on current probe. These probes use a Hall-effect device that responds to both DC and AC current. Recall that a magnetic field is developed around electrical conductors as current flows through them. The magnetic field intensity is directly proportional to the magnitude of the current. A Hall-effect device is sensitive to magnetic fields. A current-sensing oscilloscope probe is illustrated in Fig. 4-66. The probe produces a proportional voltage that is delivered to the input of the oscilloscope.

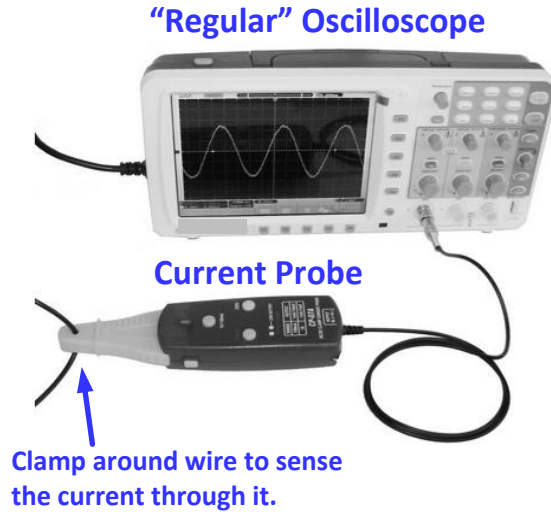


Figure 4-66.

Multisim also includes a current probe. It is in the virtual instrument suite as shown in Fig. 4-67. Simulation produces the same results achieved previously (see Fig. 4-65). (The current probe sensitivity is equivalent to our $0.1\text{-}\Omega$ current-sensing resistor. Specifically, we see that $0.1\text{ V/A} = 100\text{ mV/A} = 0.1\text{ mV/mA} = 100\text{ }\mu\text{V/mA}$.)

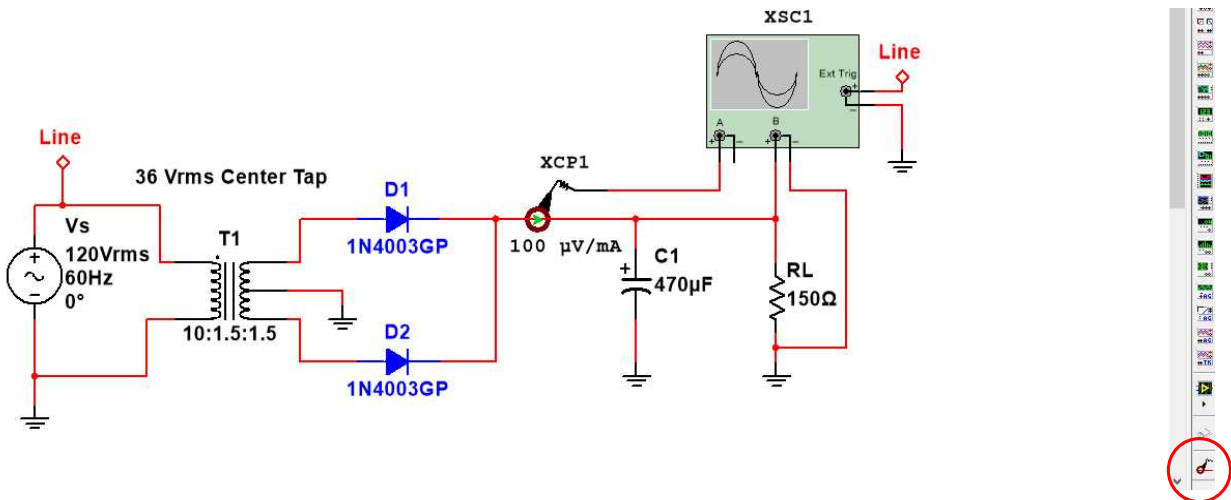


Figure 4-67.

4-17 Capacitor Ripple Current

We have seen that an electrolytic capacitor across the output of the rectifier circuit determines the magnitude of the ripple voltage, $V_{r(p-p)}$ or $V_{r(rms)}$, and the average DC level, V_{DC} . We have assumed the filter capacitor is discharged by a constant load current I_{DC} and recharged every 8.33 ms by a sharp current pulse $I_{D(PK)}$ [see Fig. 4-68(a)]. An approximation of this current waveform is provided in Fig. 4-68(b). This waveform is the *ripple current waveform* $i_r(t)$.

The ripple current waveform in Fig. 4-68 flows “through” the capacitor and can cause internal heating. Specifically, the rms value of this ripple current determines its heating effect.

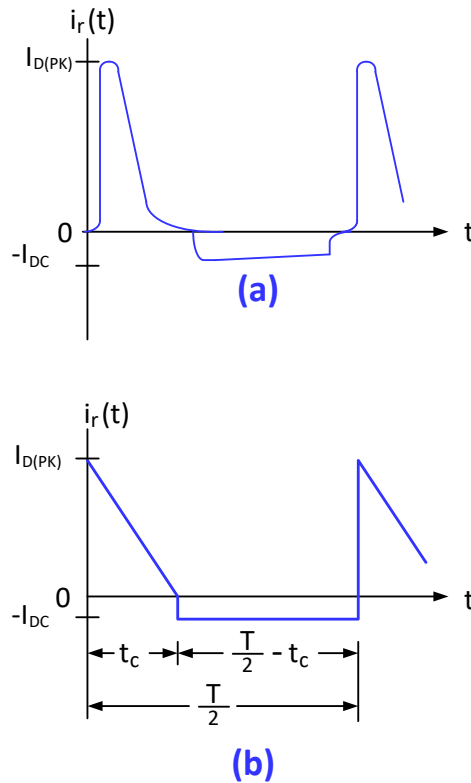


Figure 4-68.

For lightly loaded filter capacitors with an I_{DC} below one ampere, capacitor heating is usually not a major concern. However, as I_{DC} becomes larger, the size of the filter capacitor must be increased to keep the ripple factor low. ***At higher values of capacitance, the ratio of a capacitor’s outside surface area to its volume decreases. For these capacitors, internal heating may become a problem.***

Manufacturers typically specify the rms current rating for filter capacitors at a given ambient temperature. To verify a given capacitor will work, we must find the rms value of the ripple current and then consult its data sheet.

Employing the techniques described in Section 4-4, we find an equation to determine the rms value ($I_{r(rms)}$) of the ripple current approximation shown in Fig. 4-68(b).

$$\text{For 60 Hz: } I_{r(rms)} = \sqrt{120t_c \left[\frac{I_{D(PK)}^2}{3} - I_{DC}^2 \right] + I_{DC}^2} \quad (4-48)$$

Example 4-13. We continue the analysis of the DC power supply examined in Examples 4-10, 4-11, and 4-12. (The power-line frequency is 60 Hz.) The peak rectified voltage (V_{dcm}) is 24.8 V, the load current I_{DC} is 150 mA, the peak repetitive surge current $I_{D(PK)}$ is 1.99 A, and the charge time t_c is 1.255 ms. Calculate the rms value of the capacitor ripple current. If the filter capacitor has a WVDC rating of 35 V. Verify its WVDC rating is adequate. Refer to Fig. 4-67.

Solution: We calculate the rms value of the ripple current using Eq. 4-48.

$$\begin{aligned}
 I_{r(rms)} &= \sqrt{120t_c \left[\frac{I_{D(PK)}^2}{3} - I_{DC}^2 \right] + I_{DC}^2} \\
 &= \sqrt{(120)(1.255 \text{ ms}) \left[\frac{(1.99 \text{ A})^2}{3} - (150 \text{ mA})^2 \right] + (150 \text{ mA})^2}
 \end{aligned}$$

$$I_{r(rms)} = 467 \text{ mA rms}$$

Equation 4-27 is used to determine the capacitor's required WVDC rating.

$$\text{WVDC} \geq 1.2V_{dcm} = (1.2)(24.8 \text{ V}) = 29.8 \text{ V}$$

A WVDC rating of 35 V is more than adequate.

Multisim was used to simulate the circuit. A clamp-on current-sensing probe was used as shown in Fig. 4-69.

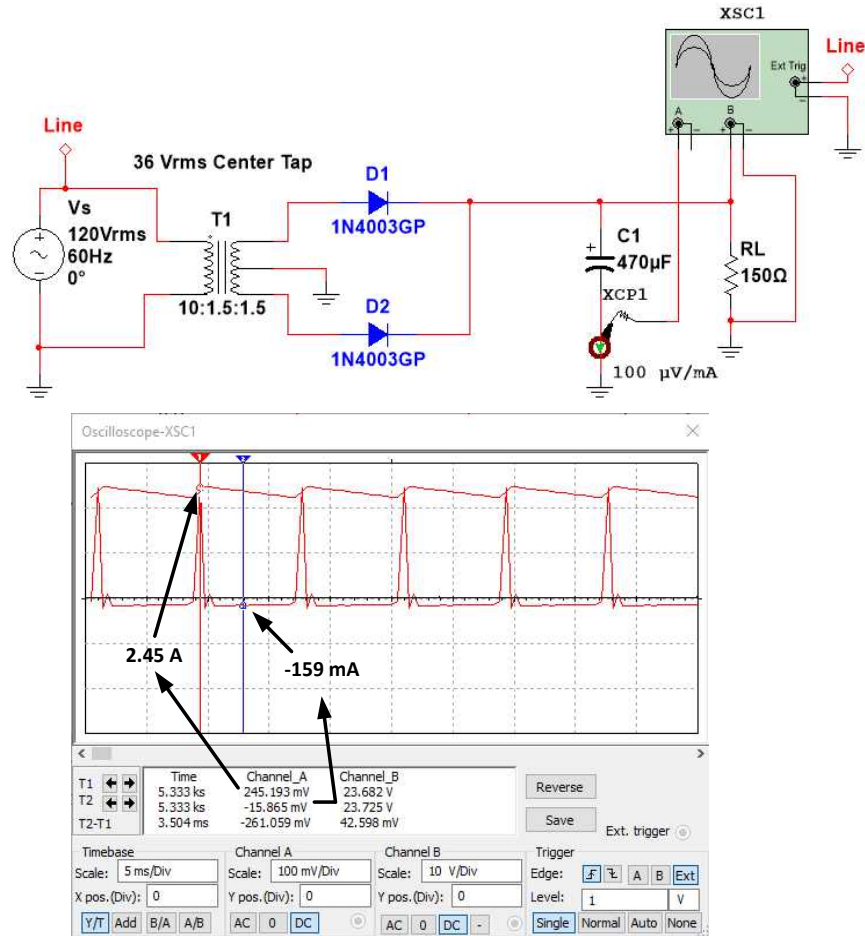


Figure 4-69.

The voltage measurements are converted to their corresponding currents by multiplying the voltages by the reciprocal of the current probe sensitivity.

$$\frac{1}{100 \mu\text{V}/\text{mA}} = \frac{1}{0.1 \text{ V}/\text{A}} = 10 \frac{\text{A}}{\text{V}}$$

The oscilloscope measurements are multiplied by ten and have units of amperes as shown in Fig. 4-69. While our approximation of the capacitor ripple current waveform simplifies analysis, it is a *crude approximation of the actual waveform*. Consequently, we offer a very conservative design rule for the capacitor ripple current rating.

$$I_{r(\text{rms}-\text{rating})} \geq 2I_{r(\text{rms})} \quad (4-49)$$

4-18 Transformer Secondary Current

When a capacitor is placed across the output of a rectifier circuit, it is recharged by spikes of current. This current is supplied by the transformer secondary. In the analysis and design of DC power supplies, it is often necessary to determine the required transformer secondary rms current rating.

A rigorous mathematical analysis to determine the required secondary current rating is very complex. This is because we have a nonsinusoidal secondary current. When we also include in any transformer nonlinearities, a rigorous mathematical analysis is of limited value. We avoid further discussion by using Table 4-2 as a design guide.

Table 4-2.

Transformer Secondary RMS Current Ratings for Full-Wave Rectifiers with Capacitive Filters	
Rectifier Configuration	Required Secondary RMS Current Rating
Full-wave rectifier using a center-tapped transformer	$1.18I_{DC}$
Full-wave bridge rectifier	$1.65I_{DC}$
Dual-complementary full-wave rectifier	$1.65I_{DC}$

Example 4-14. We continue the analysis of the DC power supply examined in Examples 4-10, 4-11, 4-12, and 4-13. The load current I_{DC} is 150 mA (see Fig. 4-69).

Solution: We calculate the rms value of the transformer secondary current using Table 4-2.

$$I_2 = 1.18I_{DC} = (1.18)(150\text{mA}) = 177\text{mA}$$

Example 4-15. Determine the required transformer secondary current (see Fig. 4-70).

Solution: We calculate the rms value of the transformer secondary current using Table 4-2.

$$I_2 = 1.65I_{DC} = (1.65)(700\text{mA}) = 1.16\text{A}$$

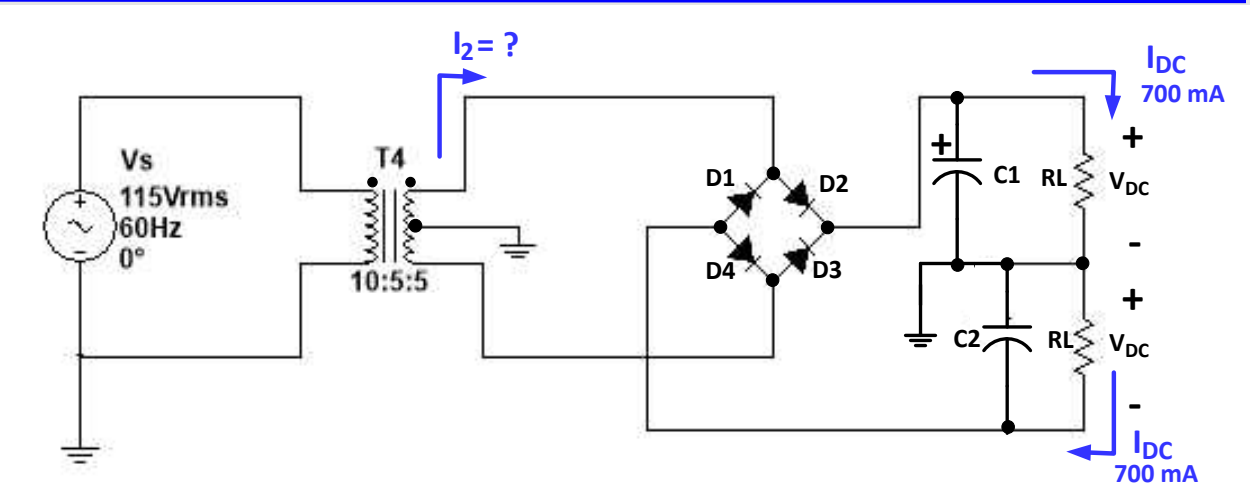


Figure 4-70.

4-19 Diode Rectifier Specifications

Specifications for diode rectifiers are established by the Joint Electron Device Engineering Council (JEDEC). JEDEC establishes standards for the electronics industry. The standards include registered part numbers (e.g., 1NXXXX), a standard set of symbols for diode ratings and electrical specifications, test conditions, test circuits, and standard case styles for electronic components. Nonregistered parts may *not* adhere to the JEDEC specification requirements. However, most manufacturers use the JEDEC standards as guidelines.

The advantage of JEDEC part numbers (e.g., 1N4003) is the *same* part is available from number of semiconductor manufacturers. For example, a 1N4003 is available from Diodes Incorporated, ON Semiconductor, Vishay Semiconductors, and others. The 1N4003 diodes are identical in all aspects.

In this section we point out some of the more common specifications and the general features offered by most data sheets. In critical applications, a design engineer would be well advised to search out the many manuals, articles, and application notes provided by manufacturers via the internet. If further questions arise, it may be necessary to call the manufacturer and discuss your technical concerns with an application engineer.

In the figures that follow, we examine a representative data sheet. Specification sheets generally cover five basic areas: (1) a general description and mechanical characteristics, (2) maximum ratings, (3) electrical characteristics, (4) derating information, and (5) dynamic information.

General Description and Mechanical Data

Consider Fig. 4-71, which is a partial data sheet for the 1N530X-series of rectifier diodes. The diodes are nearly identical except for their reverse voltage ratings. For example, a 1N5391 can withstand a maximum of reverse voltage of 50 V, while a 1N5399 is rated to withstand 1000 V.

This diode series has a JEDEC DO-204 (DO-41) case style., which has axial leads. *Axial leads* protrude out the ends of a (usually cylindrical or rectangular) component. (*Radial leads* lie on a radius and usually exit from the bottom of a cylindrical or rectangular component.)

Diode Series:

1N5391, 1N5392, 1N5393, 1N5394, 1N5395, 1N5396, 1N5397, 1N5398, 1N5399

General Purpose Plastic Rectifier



FEATURES

- Low forward voltage drop
- Low leakage current
- High forward surge capability
- Solder dip 275 °C max. 10 s, per JESD 22-B106



TYPICAL APPLICATIONS

For use in general purpose rectification of power supplies, inverters, converters, and freewheeling diodes application.

Note

- These devices are not AEC-Q101 qualified.

MECHANICAL DATA

Case: DO-204AL, molded epoxy body

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	1.5 A
V_{RRM}	50 V, 100 V, 200 V, 300 V, 400 V, 500 V, 600 V, 800 V, 1000 V
I_{FSM}	50 A
V_F	1.4 V
I_R	5.0 μ A
T_J max.	150 °C
Package	DO-204AL (DO-41)
Diode variations	Single die

Polarity: Color band denotes cathode end

Figure 4-71.

Observe one of the features of this diode series is lead (Pb) - free packages are available. **RoHS (Restriction of Hazardous Substances)** is a European Union (EU) directive that restricts the use of lead, mercury, cadmium, chromium (VI) and other materials in electrical and electronic equipment as of July 1, 2006.

Due to environmental concerns, the need for lead-free solutions in electronic components and systems receives priority attention within the semiconductor and electronics industries. Manufacturers are committed to working with their customers to be able to offer products which meet their specific needs while complying with RoHS legislation. Lead is the only RoHS-banned substance of concern for many electronic devices and integrated circuits. Therefore, lead-free products are also RoHS compliant products.

We have addressed the other features such a (low) voltage drop, (low) leakage current, and nonrepetitive surge current. Soldering temperature is a manufacturing concern. While we are interested in general purpose rectification in DC power supplies currently, other applications like inverters, converters, and free-wheeling diodes will be discussed later as our studies progress.

At the end of the data sheet, the diode dimensions are provided (see Fig. 4-72). This information is useful for the design of a printed circuit board. (Some printed circuit board layout software includes physical models for the component dimensions. Multisim includes them.)

PACKAGE OUTLINE DIMENSIONS in inches (millimeters)

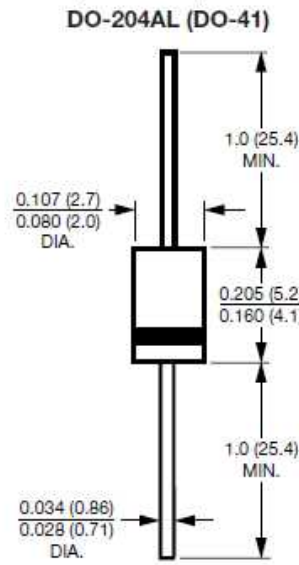


Figure 4-72.

Maximum Ratings

Unless otherwise specified, test conditions occur at a temperature of 25°C (77°F). The maximum repetitive peak reverse voltage V_{RRM} is the maximum allowable repetitive instantaneous value of the diode's reverse voltage. This rating does not apply to nonrepetitive transients or to DC conditions. Typical notation is V_R which is the maximum allowable DC reverse voltage that may be applied to the diode. This rating does not apply to repetitive and nonrepetitive transient reverse voltages and is valid across the full allowable operating temperature range of the diode.

Not used here is V_{RWM} , is the maximum allowable working peak reverse voltage of the diode. This rating does not apply to repetitive or nonrepetitive transient voltages. V_{RMS} is the rms value of a sine wave (with a current-limiting resistor in series) across diode and is equal to $0.7V_{RRM}$.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)											
PARAMETER	SYMBOL	1N5391	1N5392	1N5393	1N5394	1N5395	1N5396	1N5397	1N5398	1N5399	UNIT
Maximum repetitive peak reverse voltage	V_{RRM}	50	100	200	300	400	500	600	800	1000	V
Maximum RMS voltage	V_{RMS}	35	70	140	210	280	350	420	560	700	V
Maximum DC blocking voltage	V_{DC}	50	100	200	300	400	500	600	800	1000	V
Maximum average forward rectified current 0.500" (12.7 mm) lead length at $T_L = 70^\circ\text{C}$	$I_{F(AV)}$	1.5									A
Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load	I_{FSM}	50									A
Maximum full load reverse current, full cycle average 0.375" (9.5 mm) lead length at $T_L = 70^\circ\text{C}$	$I_{R(AV)}$	300									μA
Operation junction and storage temperature range	T_J, T_{STG}	- 50 to + 150									$^\circ\text{C}$

Figure 4-73.

I_{FSM} is the peak nonrepetitive surge current discussed in Section 4-16. $I_{F(AV)}$ (or I_o) is the average forward current at temperature of 70°C. The average reverse (leakage) current $I_{R(AV)}$ is also specified at 70°C.

The diode has an epoxy package. Epoxy does not conduct heat well. The heat within the diode is removed via its anode and cathode leads. Diode temperature can be measured indirectly by using the diode leads usually at a specified distance from the diode body.

Electrical Characteristics

Electrical characteristics typically describe such things as a diode's V-I characteristics, reverse leakage current, and temperature coefficients. Because a diode has a resistive characteristic (e.g., the bulk resistance of the semiconductor) its forward voltage drop (v_F) can increase beyond its knee voltage (of 0.7 V). In Fig. 4-74 we see the reverse current (I_R) increases as the temperature is increased as was explained in Section 3-3. We also see the reverse recovery time (t_{rr}), which was examined in Section 3-8.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)													
PARAMETER	TEST CONDITIONS		SYMBOL	1N5391	1N5392	1N5393	1N5394	1N5395	1N5396	1N5397	1N5398	1N5399	UNIT
Maximum instantaneous forward voltage	1.5 A	T _A = 70 °C	V _F	1.4									V
Maximum DC reverse current at rated DC blocking voltage		T _A = 25 °C	I _R	5.0									μA
		T _A = 150 °C		300									
Typical reverse recovery time	I _F = 0.5 A, I _R = 1.0 A, I _{rr} = 0.25 A		t _{rr}	2.0									μs
Typical junction capacitance	4.0 V, 1 MHz		C _J	15									pF

THERMAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)											
PARAMETER	SYMBOL	1N5391	1N5392	1N5393	1N5394	1N5395	1N5396	1N5397	1N5398	1N5399	UNIT
Typical thermal resistance	R _{θJA} ⁽¹⁾	55									°C/W
	R _{θJL} ⁽¹⁾	25									

Note

⁽¹⁾ Thermal resistance from junction to ambient at 0.375" (9.5 mm) lead length, P.C.B. mounted

Figure 4-74.

Thermal characteristics will be investigated in our later work. Figure 4-75 includes additional electrical characteristics in Figs. 3 and 4. Notice that semilog scales are used. This allows the data to be compressed which permits larger ranges to be presented.

RATINGS AND CHARACTERISTIC CURVES 1N5391 THRU 1N5399

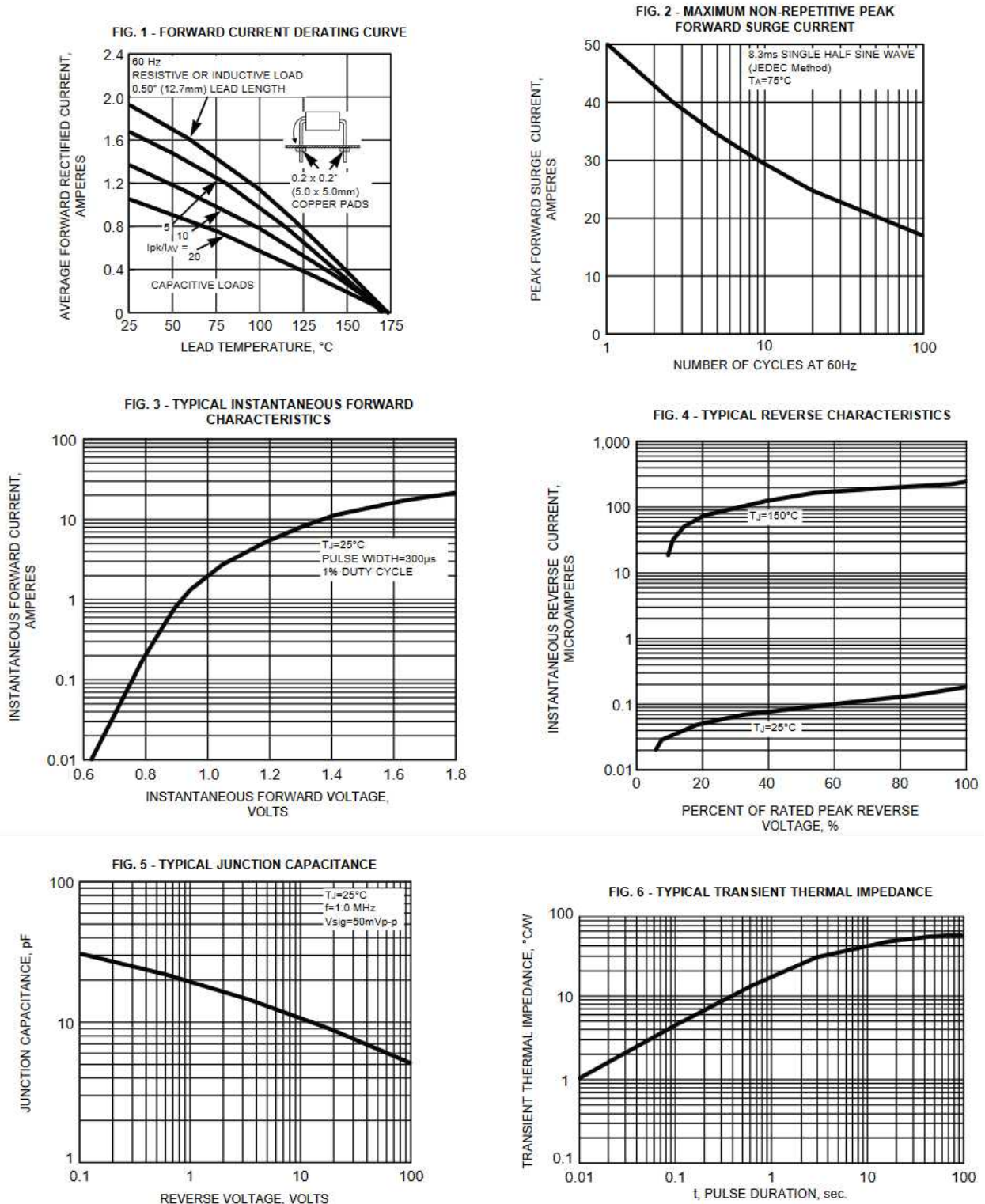


Figure 4-75.

Derating Information

Figure 1 in Fig. 4-75 shows how the average forward current rating is reduced based on the $I_{D(PK)}/I_{D(AV)}$ ratio. (The manufacturer does not include the “D” in the subscripts.) Figure 2 in Fig. 4-75 shows how the nonrepetitive surge current rating decreases as the number of cycle increases.

Dynamic Information

Reverse recovery time and junction capacitance are dynamic quantities. These quantities do not play a large role in 60-Hz, line-operated DC linear power supplies.

4-20 Three-Terminal IC Voltage Regulators

We reach the fourth functional block of our linear DC power supply – the **voltage regulator**. We make our “official” examination of voltage regulators in Chapter 18. For now, we introduce the use and application of **three-terminal voltage regulators**. The positive voltage regulators have 78XX part numbers, while the negative voltage regulators have 79XX part numbers. Package (case style) options for the 7800-series are shown in Fig. 4-76.

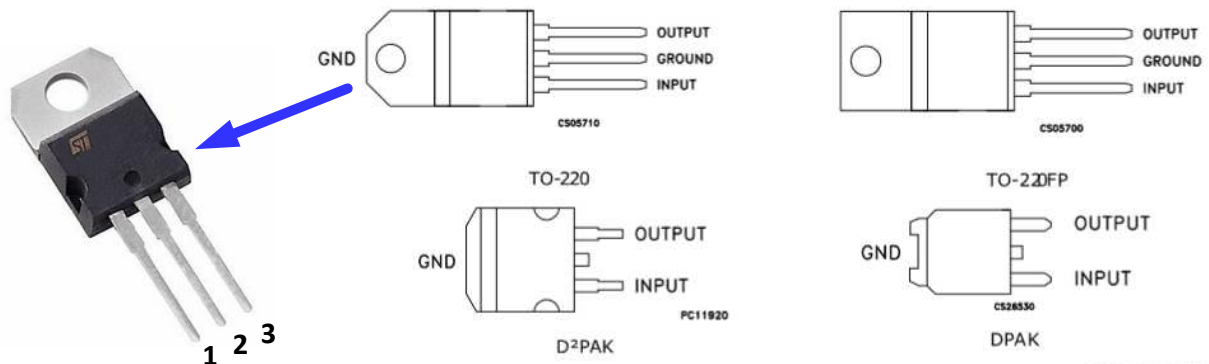


Figure 4-76.

Several fixed-output-voltage options are available such as 7805 (5 V), 7809 (9 V), 7815 (15 V), and 7824 (24 V). Obviously, the output voltage is included in the part number.

The application circuit is provided in Fig. 4-77. According to the manufacturers, capacitor C_1 should be used if more than three to four inches of conductor between the regulator’s input terminal and the filter capacitor to ensure the regulator does not oscillate. (Oscillation means unwanted high-frequency electrical noise is generated.) Capacitor C_2 is recommended to improve the regulator’s response to transient load changes. It is usually wise to comply with the manufacturer’s recommendations. The capacitors can be disc ceramics or metallized polyester types.

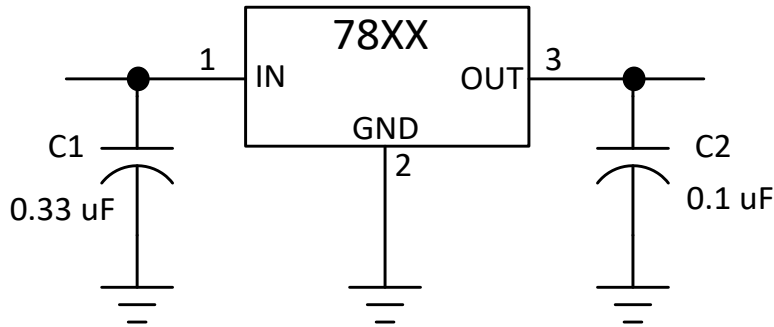


Figure 4-77.

In Fig. 4-78(a) we see the regulator's input voltage (v_{IN}) and, its output voltage (V_{OUT}) are defined. There is also a differential voltage drop (v_{DIFF}) across the regulator. We apply KVL around the regulator to obtain Eq. 4-50.

$$\begin{aligned} -v_{IN} + v_{DIFF} + V_{OUT} &= 0 \\ v_{DIFF} &= v_{IN} - V_{OUT} \end{aligned} \quad (4-50)$$

The voltage regulator requires a minimum value of v_{DIFF} to provide a constant output voltage. If the differential voltage falls below that value, the voltage regulator will drop out of regulation. That means its output voltage may not be constant. This minimum value of v_{DIFF} is called the **dropout voltage** ($v_{DROPOUT}$). The dropout voltage for the 7800 series has a typical value of 2 V and a maximum value of 2.5 V. ***If the minimum value ($V_{dc(min)}$) of the voltage across the filter capacitor is too low, the dropout voltage requirement will be violated.*** To maintain voltage regulation, equation 4-51 must be obeyed.

$$V_{dc(min)} \geq v_{DROPOUT} + V_{OUT} \quad (4-51)$$

As shown in Fig. 4-78(b), the output voltage of the three-terminal voltage regulator is constant. Although there is a ripple voltage across its input, its output voltage is perfectly smooth. The regulator is said to provide **ripple rejection**. Capacitor C_1 is the filter capacitor. Capacitor C_2 is used to prevent high-frequency oscillations in the regulator. It has been left in the circuit because electrolytic capacitors start to act like inductors at high frequencies.

The 7818 is an 18-volt voltage regulator. The 7800-series includes output short-circuit protection and will shut down if it overheats. Consequently, the device should be mounted to a heat sink. For now, that means a sheet of aluminum. Thermal effects and heat sinks are addressed in Chapters 15 (power amplifiers) and 18 (DC power supply regulators) **found in Volume Three of this series.**

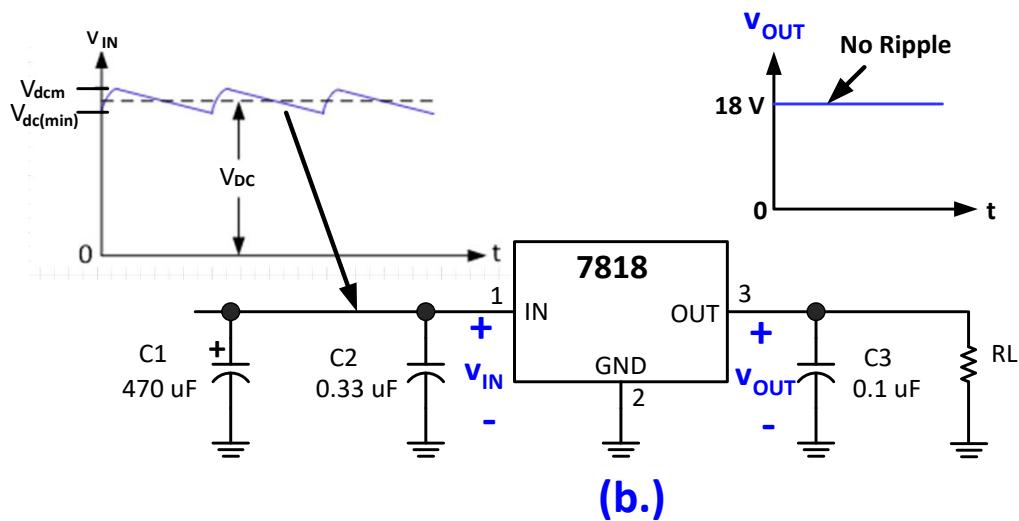
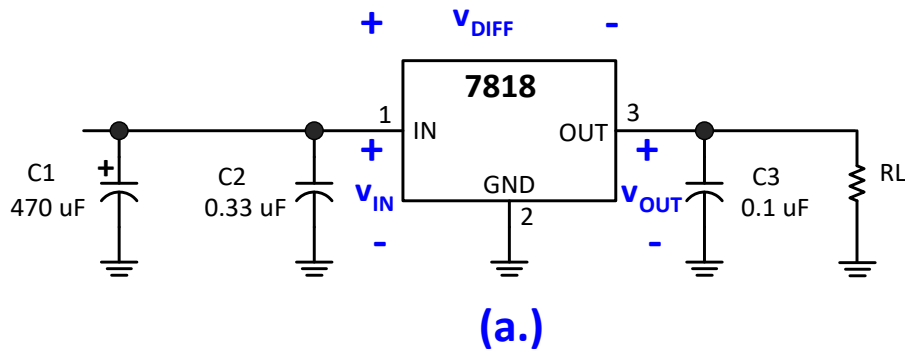


Figure 4-78.

Problems for Chapter 4

Drill Problems

Section 4-1

- 4-1 In comparison to a switching DC power supply, a linear DC power supply is _____.
- Lighter (and) more complex.
 - Heavier (and) simpler.
 - Lighter (and) simpler.
 - Heavier (and) more complex.
- 4-2 In comparison to a linear DC power supply, a switching DC power supply is _____ (more, less) suitable for portable applications like notebook computers.

Section 4-2

- 4-3 The headphone amplifier in Fig. 4-3 has been modified. The preamplifiers now draw 25 mA, power amplifiers now require 200 mA, but the USB battery charger still requires 1200 mA. The DC voltage across the output of the DC power supply is 22 volts. Determine the total load current draw (I_L), the equivalent load resistance (R_L) and the DC power (P_L) delivered to the load.
- 4-4 The headphone amplifier in Fig. 4-3 has been modified. The preamplifiers now draw 40 mA, power amplifiers now require 250 mA, but the USB battery charger still requires 1200 mA. The DC voltage across the output of the DC power supply is 18 volts. Determine the total load current draw (I_L), the equivalent load resistance (R_L) and the DC power (P_L) delivered to the load.

Section 4-3

- 4-5 Name the three wires associated with a single-phase AC power installation. What are their color assignments?
- 4-6 In a normal installation, the ground wire _____.
- (a) Should pass no current unless a fault has occurred.
 - (b) Should be connected to the neutral connection at the service entrance.
 - (c) Should never be defeated (e.g., cutting off the ground prong of a power plug).
 - (d) All of these.
- 4-7 When (if ever) is a ground connection unnecessary?

Section 4-4

- 4-8 A 6-V peak-to-peak triangle wave rides on a 25-V DC level ($V_{DC} = 25$ V). Determine the maximum and minimum positive values. The situation is like Fig. 4-11.
- 4-9 An 8-V peak-to-peak triangle wave rides on a 15-V DC level ($V_{DC} = 15$ V). Determine the maximum and minimum positive values. The situation is like Fig. 4-11.
- 4-10 The half-wave rectifier in Fig. 4-13(a) has a peak rectified voltage (V_{dcm}) of 22 volts. Determine its DC average value (V_{DC}).
- 4-11 The half-wave rectifier in Fig. 4-13(a) has a peak rectified voltage (V_{dcm}) of 15 volts. Determine its DC average value (V_{DC}).
- 4-12 The full-wave rectifier in Fig. 4-13(b) has a peak rectified voltage (V_{dcm}) of 22 volts. Determine its DC average value (V_{DC}).
- 4-13 The full-wave rectifier in Fig. 4-13(b) has a peak rectified voltage (V_{dcm}) of 15 volts. Determine its DC average value (V_{DC}).
- 4-14 A sine wave has a peak value (V_m) of 20 V. Refer to Fig. 4-15(a). What are its average and rms values?

- 4-15 A sine wave has a peak value (V_m) of 12 V. Refer to Fig. 4-15(a). What are its average and rms values?
- 4-16 An AC square wave has a peak value (V_m) of 12 V. Refer to Fig. 4-15(b). What are its average and rms values?
- 4-17 An AC square wave has a peak value (V_m) of 18 V. Refer to Fig. 4-15(b). What are its average and rms values?
- 4-18 A triangle wave has a peak-to-peak value of 5 Vp-p. Refer to Fig. 4-15(c). Find its peak value (V_m), its DC average value (V_{DC}), and its rms value (V_{rms}).
- 4-19 A triangle wave has a peak-to-peak value of 2 Vp-p. Refer to Fig. 4-15(c). Find its peak value (V_m), its DC average value (V_{DC}), and its rms value (V_{rms}).
- 4-20 A half-wave rectified waveform has a peak value (V_m) of 20 V. Refer to Fig. 4-15(d). What are its average and rms values?
- 4-21 A half-wave rectified waveform has a peak value (V_m) of 12 V. Refer to Fig. 4-15(d). What are its average and rms values?
- 4-22 A full wave rectified waveform has a peak value (V_m) of 30 V. Refer to Fig. 4-15(e). What are its average and rms values?
- 4-23 A full wave rectified waveform has a peak value (V_m) of 12 V. Refer to Fig. 4-15(e). What are its average and rms values?

Section 4-5

- 4-24 A transformer is given in Fig. 4-18. Its primary voltage (V_1) is 117 Vrms and its secondary voltage (V_2) is 25.2 Vrms. The load resistance R_L is changed to 20 Ω . Compute the transformer turn ratio (N_2/N_1), the secondary current (I_2), and the primary current (I_1). Find the AC power delivered to the primary winding (P_{in}) and the AC power absorbed by the load (P_{out}).
- 4-25 A transformer is given in Fig. 4-18. Its primary voltage (V_1) is 120 Vrms and its secondary voltage (V_2) is 6.3 Vrms. The load resistance R_L is changed to 10 Ω . Compute the transformer turn ratio (N_2/N_1), the secondary current (I_2), and the primary current (I_1). Find the AC power delivered to the primary winding (P_{in}) and the AC power absorbed by the load (P_{out}).
- 4-26 A transformer has a secondary voltage of 6.3 Vrms under a full-load secondary current of 0.96 Arms. Calculate its VA rating and use Table 4-1 to determine its typical percent of voltage regulation. What is its no-load voltage (V_{NL})?
- 4-27 A transformer has a secondary voltage of 12.6 Vrms under a full-load secondary current of 0.96 Arms. Calculate its VA rating and use Table 4-1 to determine its typical percent of voltage regulation. What is its no-load voltage (V_{NL})?

Section 4-6

- 4-28 The transformer secondary voltage in Fig. 4-27(a) has been increased to 25.2 Vrms. Determine the peak secondary voltage (V_m), the peak rectified voltage across the load (V_{dcm}), the DC load voltage (V_{DC}), the diode's maximum reverse bias (V_{RM}), the peak load current (I_m), and the DC load current (I_{DC}). What is the diode's average forward current ($I_{D(AV)}$)?
- 4-29 The transformer secondary voltage in Fig. 4-27(a) has been increased to 40 Vrms. Determine the peak secondary voltage (V_m), the peak rectified voltage across the load (V_{dcm}), the DC load voltage (V_{DC}), the diode's maximum reverse bias (V_{RM}), the peak load current (I_m), and the DC load current (I_{DC}). What is the diode's average forward current ($I_{D(AV)}$)?
- 4-30 Cite two disadvantages associated with the half-wave rectifier.

Section 4-7

- 4-31 Analyze the full-wave rectifier circuit given in Fig. 4-34. The transformer has been replaced with a Signal ST 4-28. It too is designed to be mounted on a printed-circuit board. The transformer has two separate secondary windings that can be connected as shown in Fig. 4-34 to form a center tap. **The transformer is rated to be 28 VCT at a maximum secondary current of 0.2 Arms.** Determine the peak secondary voltage (V_m) across one half of the secondary, the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$].
- 4-32 Analyze the full-wave rectifier circuit given in Fig. 4-34. The transformer has been replaced with a Signal ST 5-56. It too is designed to be mounted on a printed-circuit board. The transformer has two separate secondary windings that can be connected as shown in Fig. 4-34 to form a center tap. **The transformer is rated to be 56 VCT at a maximum secondary current of 0.22 Arms.** Determine the peak secondary voltage (V_m) across one half of the secondary, the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$].

Section 4-8

- 4-33 Analyze the full-wave bridge rectifier circuit given in Fig. 4-38(a). The transformer has a secondary voltage of 12.6 Vrms with a maximum current rating of 2.6 Arms. The load resistor R_L is 30 Ω . Determine the peak secondary voltage (V_m), the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$].
- 4-34 Analyze the full-wave bridge rectifier circuit given in Fig. 4-38(a). The transformer has a secondary voltage of 28 Vrms with a maximum current rating of 1.5 Arms. The load resistor R_L is 60 Ω . Determine the peak secondary voltage (V_m), the peak rectified voltage (V_{dcm}) across the load, the DC load voltage (V_{DC}), the diode maximum reverse bias (V_{RM}), the peak load current (I_m), the DC load current (I_{DC}), and the average diode current [$I_{D(AV)}$].

Section 4-9

- 4-35 Analyze the dual-complementary full-wave rectifier circuit given in Fig. 4-45(b). **The transformer is rated to be 28 VCT at a maximum secondary current of 0.2 Arms.** The load resistors (the R_L 's) are both $60\ \Omega$. Determine the peak secondary voltage (V_m) across one half of the secondary, the positive peak rectified voltage (V_{dcm}) across the upper load, the DC load voltage (V_{DC}) across the upper load, the diode maximum reverse bias (V_{RM}), the peak load current (I_m) through the upper load, the DC load current (I_{DC}) through the upper load, and the average diode current [$I_{D(AV)}$]. What is the DC voltage with respect to ground across the lower load?
- 4-36 Analyze the dual-complementary full-wave rectifier circuit given in Fig. 4-45(b). **The transformer is rated to be 56 VCT at a maximum secondary current of 0.22 Arms.** The load resistors (the R_L 's) are both $60\ \Omega$. Determine the peak secondary voltage (V_m) across one half of the secondary, the positive peak rectified voltage (V_{dcm}) across the upper load, the DC load voltage (V_{DC}) across the upper load, the diode maximum reverse bias (V_{RM}), the peak load current (I_m) through the upper load, the DC load current (I_{DC}) through the upper load, and the average diode current [$I_{D(AV)}$]. What is the DC voltage with respect to ground across the lower load?

Section 4-10

- 4-37 Simple capacitor filters are placed in _____ (series, parallel) with the load.
- 4-38 Other “classic” DC power supply filter circuits called L-input, R-C pi, and L-C pi tend to be _____.
- (a) Simple and inexpensive.
 - (b) Effective and low weight.
 - (c) Heavy and expensive.
 - (d) None of these.
- 4-39 What is the key advantage offered by electrolytic capacitor? Explain briefly.
- 4-40 Electrolytic capacitors are typically _____ (nonpolarized, polarized).
- 4-41 Name the two common types of electrolytic capacitors. Which type offers the higher voltage ratings?
- 4-42 A filter capacitor experiences a peak rectified voltage (V_{dcm}) of 47 V. What is its *minimum* WVDC rating? Which standard rating (25, 35, 50, or 75 V) should be selected?
- 4-43 A filter capacitor experiences a peak rectified voltage (V_{dcm}) of 30.5 V. What is its *minimum* WVDC rating? Which standard rating (25, 35, 50, or 75 V) should be selected?

Section 4-11

- 4-44 When a filter capacitor is in parallel with the load [see Fig. 4-48(c)] a ripple voltage is produced. After the initial charge, what is required to permit the filter capacitor to recharge? When does a filter capacitor discharge? Explain briefly.
- 4-45 A DC power supply with a simple capacitor filter and a full-wave rectifier has a peak rectified voltage (V_{dcm}) of 22 V. The peak-to-peak ripple voltage is 1.9 Vp-p. Calculate the minimum instantaneous voltage ($V_{dc(min)}$) across the load. Find the DC average level (V_{DC}) across the load.
- 4-46 A DC power supply with a simple capacitor filter and a full-wave rectifier has a peak rectified voltage (V_{dcm}) of 18 V. The peak-to-peak ripple voltage is 1.5 Vp-p. Calculate the minimum instantaneous voltage ($V_{dc(min)}$) across the load. Find the DC average level (V_{DC}) across the load.
- 4-47 To reduce the peak-to-peak ripple, the size of the filter capacitor must be _____ (increased, decreased).
- 4-48 To reduce the peak-to-peak ripple, the size of the DC load current must be _____ (increased, decreased).

Section 4-12

- 4-49 Analyze the rectifier circuit block diagram shown in Fig. 4-50. The **total waveform** across the load appears as shown in Fig. 4-51(a). The peak rectified voltage (V_{dcm}) across the load is 25 V. The peak-to-peak ripple voltage $V_{r(p-p)}$ is 2.5 V. Find $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the %r, and the required WVDC rating for the capacitor.
- 4-50 Analyze the rectifier circuit block diagram shown in Fig. 4-50. The total waveform across the load appears as shown in Fig. 4-51(a). The peak rectified voltage (V_{dcm}) across the load is 15 V. The peak-to-peak ripple voltage $V_{r(p-p)}$ is 1.0 V. Find $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the %r, and the required WVDC rating for the capacitor.
- 4-51 The **ideal** percent ripple factor (%r) is _____ (0%, 50%, 100%, 125%).

Section 4-13

- 4-52 If the peak rectified voltage (V_{dcm}) across the simple filter capacitor is 30 V and the filter is loaded lightly, determine the minimum DC voltage (V_{DC}) across the load. (Hint: Use Eq. 4-33 and Eq. 4-29 to solve for $V_{r(p-p)}$. Then use Eq. 4-28 to find $V_{dc(min)}$.)
- 4-53 If the peak rectified voltage (V_{dcm}) across the simple filter capacitor is 11.3 V and the filter is loaded lightly, determine the minimum instantaneous DC voltage ($V_{dc(min)}$) across the load. (Hint: Use Eq. 4-33 and Eq. 4-29 to solve for $V_{r(p-p)}$. Then use Eq. 4-28 to find $V_{dc(min)}$.)

- 4-54 Show that the percent ripple factor ($\%r$) for light loading is **6.42%**. (Hint: Use Eq. 4-33 and Eq. 4-29 to solve for $V_{r(p-p)}$. Figure 4-15(c) gives $V_{r(rms)}$. Equation 4-31 provides the ripple factor percentage.)

Section 4-14

- 4-55 A simple capacitor filter uses a $1000\ \mu\text{F}$ capacitor (C). The DC load current (I_{DC}) is $0.15\ \text{A}$ and the ripple frequency (f_r) is $120\ (\text{Hz})$. Find the peak-to-peak ripple ($V_{r(p-p)}$).
- 4-56 A simple capacitor filter uses a $510\ \mu\text{F}$ capacitor (C). The DC load current (I_{DC}) is $0.2\ \text{A}$ and the ripple frequency (f_r) is $120\ (\text{Hz})$. Find the peak-to-peak ripple ($V_{r(p-p)}$).
- 4-57 Analyze the DC power supply shown in Fig. 4-79. The DC load current (I_{DC}) is $250\ \text{mA}$. Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the $\%r$, and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter.
- 4-58 Analyze the DC power supply shown in Fig. 4-79. The **transformer** is changed to a **25.2 VCT** unit. The load resistance (R_L) is now **$20\ \Omega$** . The capacitor (C_I) is changed to a **$2000\text{-}\mu\text{F}$** unit. The DC load current (I_{DC}) is **$750\ \text{mA}$** . Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the $\%r$, and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter.

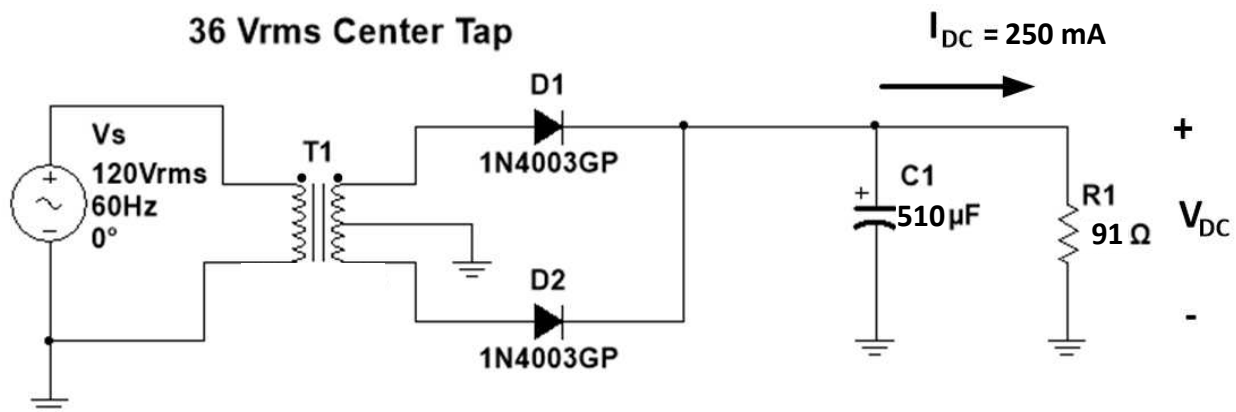


Figure 4-79.

- 4-59 Analyze the DC power supply shown in Fig. 4-80. The **transformer secondary voltage** is **$25.2\ \text{Vrms}$** . The load resistance (R_L) is **$40.7\ \Omega$** . The capacitor (C_I) is a **$2000\text{-}\mu\text{F}$** unit. The DC load current (I_{DC}) is **$800\ \text{mA}$** . Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the $\%r$, and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter.

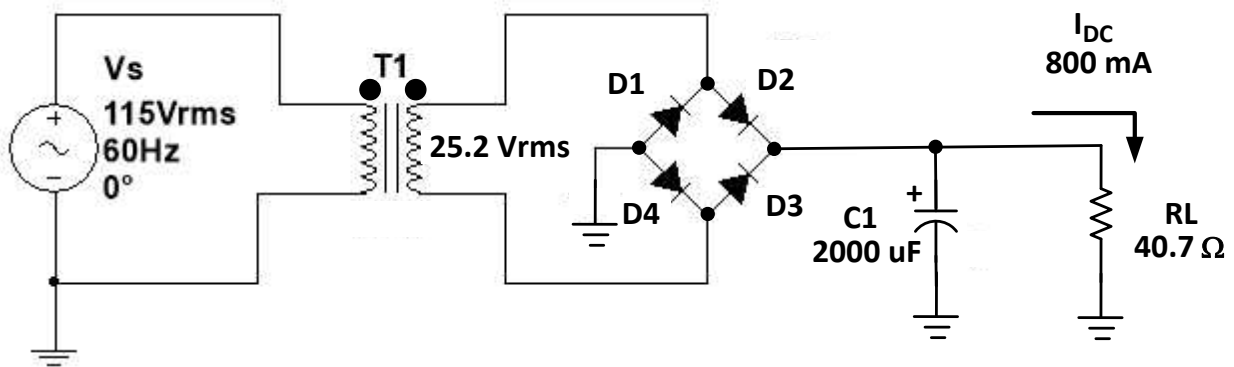


Figure 4-80.

- 4-60 Analyze the DC power supply shown in Fig. 4-80. The **transformer secondary voltage** is now **36 Vrms**. The load resistance (R_L) is **40.7 Ω**. The capacitor (C_1) is a **1500-μF** unit. The DC load current (I_{DC}) is **300 mA**. Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the $\%r$, and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter.
- 4-61 Analyze the dual-complementary DC power supply shown in Fig. 4-81. (Hint: Analyze the top portion of the circuit as a full-wave rectifier using a center-tapped transformer. The voltages associated with the bottom portion have the same magnitudes but are negative with respect to ground.) The transformer secondary voltage is 25.2 VCT. The capacitor (C_1) is a 470-μF unit. The DC load current (I_{DC}) is 150 mA. Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the $\%r$, and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter. What is the voltage across the bottom load resistor with respect to ground?

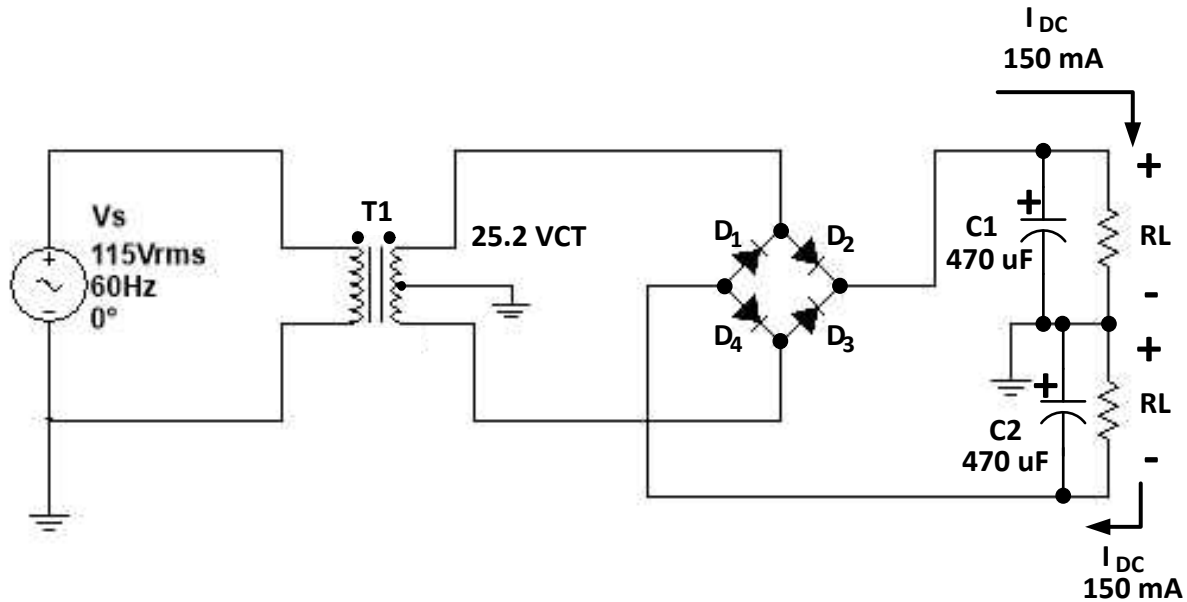


Figure 4-81.

- 4-62 Analyze the dual-complementary DC power supply shown in Fig. 4-81. (Hint: Analyze the top portion of the circuit as a full-wave rectifier using a center-tapped transformer. The voltages associated with the bottom portion have the same magnitudes but are negative with respect to ground.) **The transformer secondary voltage is now 12.6 VCT.** The capacitor (C_1) is a 470- μF unit. The DC load current (I_{DC}) is 150 mA. Find V_m , V_{dcm} , $V_{r(p-p)}$, $V_{dc(min)}$, V_{DC} , $V_{r(rms)}$, the % r , and determine the required WVDC rating for the capacitor. Check that we have a lightly loaded filter. What is the voltage across the bottom load resistor with respect to ground?

Section 4-15

- 4-63 As the size of a simple capacitor filter *increases*, the peak-to-peak ripple voltage _____ (increases, decreases, remains the same) and the peak repetitive current _____ (increases, decreases, remains the same).
- 4-64 A DC power supply has a DC load current (I_{DC}) of 150 mA. The DC power supply operates from a 60 Hz power line. Previous analysis has given a $V_{dcm} = 17.10$ V and a $V_{dc(min)} = 14.46$ V. Find $I_{D(AV)}$, I_o , the filter capacitor charge time t_c , $I_{D(PK)}$, and the $I_{D(PK)} / I_{D(AV)}$ ratio for the rectifier diodes.
- 4-65 A DC power supply has a DC load current (I_{DC}) of 300 mA. The DC power supply operates from a 60 Hz power line. Previous analysis has given a $V_{dcm} = 49.51$ V and a $V_{dc(min)} = 47.84$ V. Find $I_{D(AV)}$, I_o , the filter capacitor charge time t_c , $I_{D(PK)}$, and the $I_{D(PK)} / I_{D(AV)}$ ratio for the rectifier diodes.

Section 4-16

- 4-66 Compute the nonrepetitive surge current ($I_{D(SURGE)}$) of a DC power supply. The peak rectified voltage (V_{dc}) is 17.1 V, the transformer secondary resistance (R_2) is 0.5 Ω , and the diode bulk resistance (r_B) is 0.2 Ω .
- 4-67 Compute the nonrepetitive surge current ($I_{D(SURGE)}$) of a DC power supply. The peak rectified voltage (V_{dc}) is 49.51 V, the transformer secondary resistance (R_2) is 0.2 Ω , and the diode bulk resistance (r_B) is 0.15 Ω .

Section 4-17

- 4-68 A 60-Hz, line operated DC power supply has a peak repetitive surge current ($I_{D(PK)}$) of 5 A. The charge time (t_c) is 1.15 ms. The load current (I_{DC}) is 300 mA. Calculate the rms value of the capacitor ripple current ($I_{r(rms)}$).
- 4-69 A 60-Hz, line operated DC power supply has a peak repetitive surge current ($I_{D(PK)}$) of 3 A. The charge time (t_c) is 1.28 ms. The load current (I_{DC}) is 350 mA. Calculate the rms value of the capacitor ripple current ($I_{r(rms)}$).

Section 4-18

- 4-70 A 60-Hz line operated transformer-coupled DC power supply is to supply a DC load current of 1 A. The DC power supply design incorporates a full-wave rectifier using a center-tapped transformer. Determine the minimum required transformer secondary current rating.
- 4-71 A 60-Hz line operated transformer-coupled DC power supply is to supply a DC load current of 1 A. The DC power supply design incorporates a full-wave bridge rectifier. Determine the minimum required transformer secondary current rating.

Section 4-19

- 4-72 Without datasheet information it is very likely the reverse voltage rating of a 1N4009 diode is _____ (greater than, less than, equal to) the reverse voltage rating of a 1N4001 diode.
- 4-73 Explain briefly the differences between components that have *axial leads* versus *radial leads*.
- 4-74 What is meant by RoHS compliant products? Explain briefly.
- 4-75 With reference to Fig. 4-75, when the reverse voltage across a diode increases its junction capacitance _____ (increases, decreases, remains the same).

Section 4-20

- 4-76 A LM7805 three-terminal voltage regular provides a 5-volt DC output voltage. It has a maximum dropout voltage of 3.5 V. Determine the smallest value of $V_{dc(min)}$ required to ensure the regulator operates properly.

- 4-77 A LM7812 three-terminal voltage regulator provides a 12-volt DC output voltage. It has a maximum dropout voltage of 3.5 V. Determine the smallest value of $V_{dc(min)}$ required to ensure the regulator operates properly.

Electronic Design Automation (EDA) Problems

Section 4-4

- 4-78 Use Multisim to generate and display the triangle waveform (using the oscilloscope). Using the multimeters display the average (DC) and rms (AC) values of the waveform. Figure 4-82 provides hints. The triangle wave has a peak-to-peak value of 5 V. The frequency is 1 kHz, which means the period is 1 ms. The voltage offset is -2.5 V. The causes the waveform to be ± 2.5 V around 0 V. The circuit wiring is simplified by using on-page connectors. Double clicking on the triangle generator schematic symbol will cause its value-edit window to pop up. Duplicate the circuit and conditions shown in Fig. 4-82. Once you are confident in its set up and results, change the triangle generator to produce 3-V p-p waveform at a frequency of 120 Hz riding on a 16.5-V DC level. The trigger level for the single sweep of the oscilloscope can be set to 15.5 V.

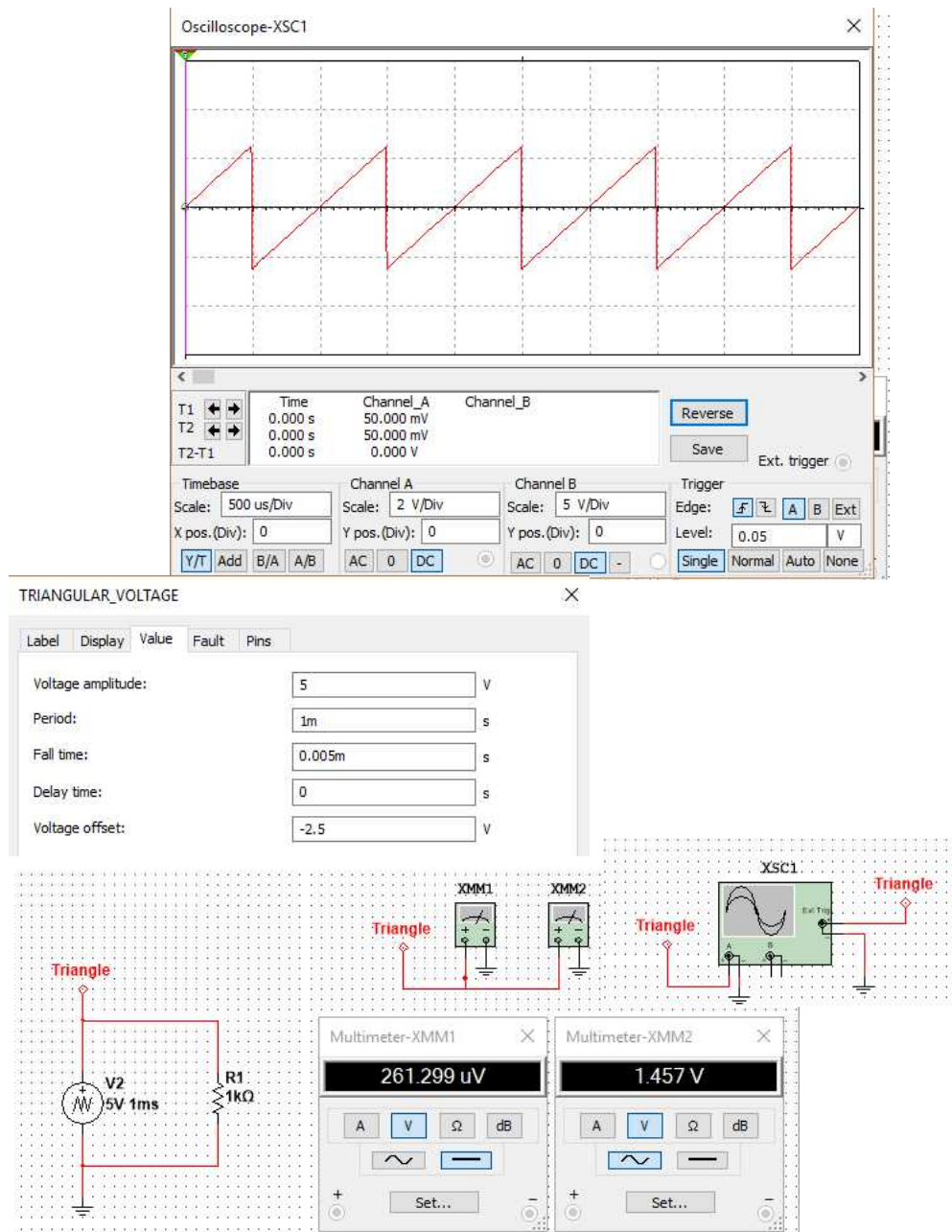


Figure 4-82.

- 4-79 Use the cursor of the oscilloscope to find $V_{dc(min)}$ for 3 Vp-p ripple waveform simulated in Prob 4-78. How does the triangle generator voltage offset compare to $V_{dc(min)}$? Duplicate the simulation of a square wave using the Multisim pulse generator as shown in Fig. 4-83.
- 4-80 Modify the simulation of a square wave shown in Fig. 4-83 to produce a waveform that goes from 0 V (initial value) to 10 V. Use the Multisim multimeters to display the average and rms values of the square wave?

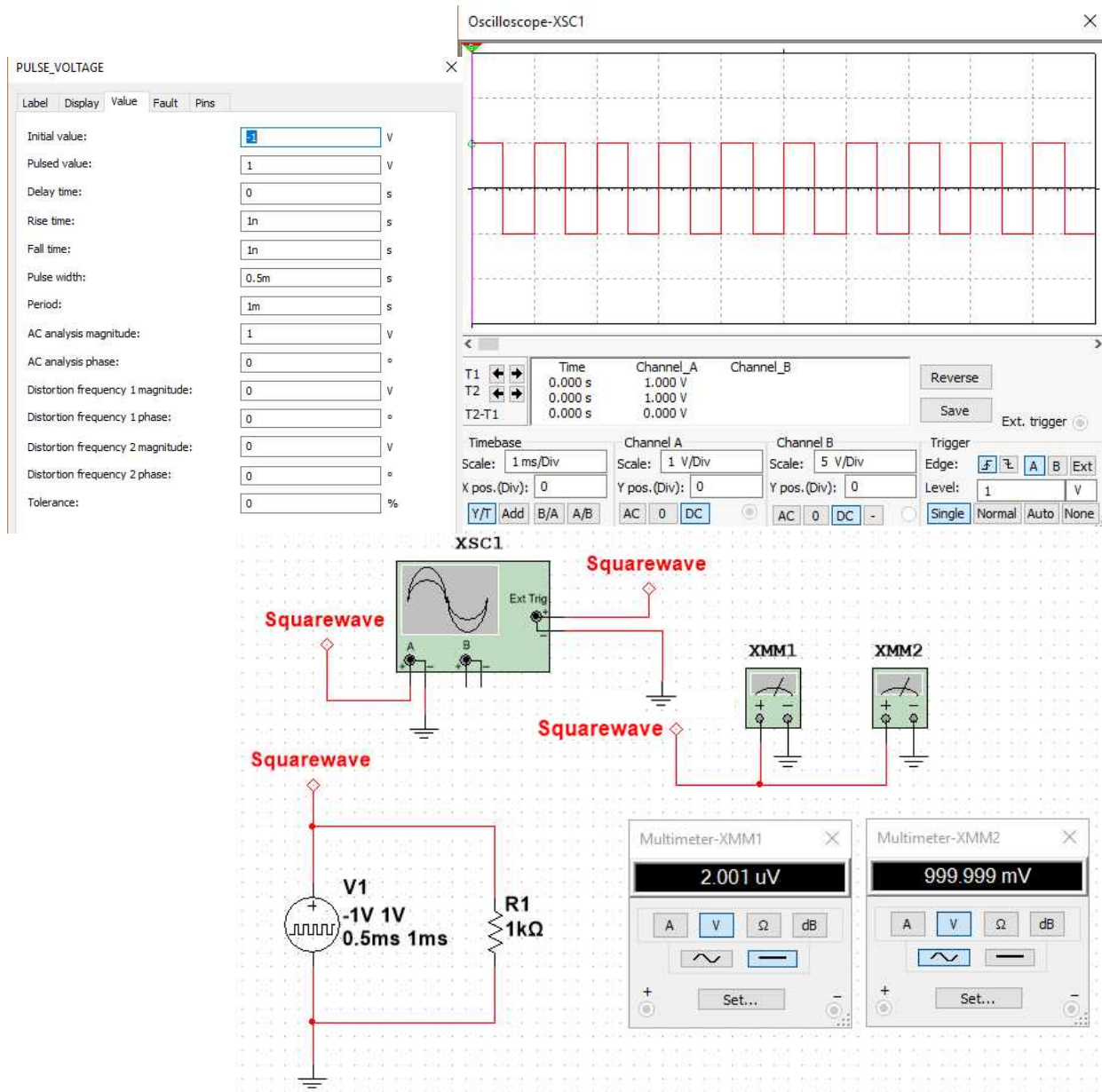


Figure 4-83.

Section 4-6

- 4-81 Repeat the simulation in Fig. 4-21, but change the transformer turns ratio to 10:2.
- 4-82 A transformer has a secondary voltage full-load voltage rating (V_{FL}) of 36 V at a secondary current of 2 Arms. Determine its VA rating and use Table 4-1 to determine its %VR. Find its no-load voltage (V_{NL}). **In Fig. 4-23 the secondary voltage (V_S) is the same as V_{NL} .** Refer to Fig. 4-22. Determine the equivalent secondary resistance (R_S) and the equivalent load resistance (R_L). Use Multisim to verify your results as shown in Fig. 4-23.

- 4-83 Use Multisim to analyze the half-wave rectifier given in Fig. 4-27(a). Display the load voltage waveform and the voltage waveform across the diode rectifier as indicated in Fig. 4-27(d). The two-channel oscilloscope has a *differential* input. That means it can display the difference between two signals. The channel A “+” input is connected to “Secondary” while the channel A “-” input is connected to the “Load”. This will permit channel A to display the voltage across the diode. We expect to see a waveform such as that shown in Fig. 4-27(d).

Section 4-8

- 4-84 Use Multisim to produce the load voltage waveform for the schematic in Fig. 4-42 if the transformer secondary voltage is 12.6 Vrms. Your challenge is to determine the required turns ratio and then run the simulation.

Section 4-9

- 4-85 Employ Multisim to develop the load voltage waveforms for Fig. 4-45. The transformer is 25.2 VCT. Connect the oscilloscope so that its grounds are connected to the circuit ground.

Power Supply Design

In this problem set, you will be guided through design choices and be required to make decisions and calculations. The first thing any designer must do is determine the design specifications (requirements). The electrical input and output(s) requirements are obvious. However, “real” project requirements will include detailed electrical performance requirements, packaging needs, economics, environmental considerations, and the schedule timeline. Quite often schedule is the biggest challenge. Our specifications will be minimalistic.

Input power: 115 Vrms, 60 Hz.

Output: 18 VDC @ 140 mA maximum

The usual approach is for a designer to investigate previous solutions and then decide the best approach to the current problem and develop a block diagram. The block diagram is provided in Fig. 4-84. Each of the blocks should be familiar, with the exception of “Input Protection”, which will be explained later.

DC Power Supply System Block Diagram

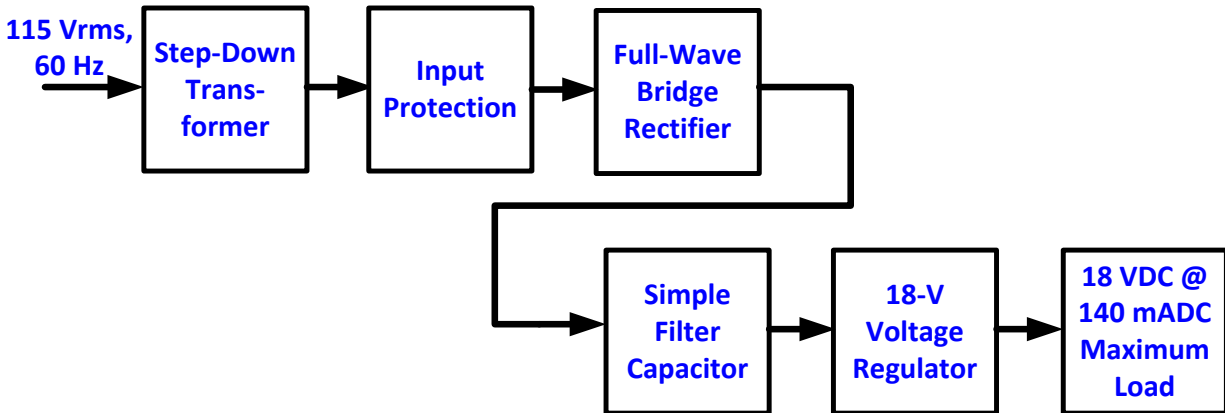


Figure 4-84.

- 4-86 Given the DC power supply is to deliver 18 volts, first select the three-terminal regulator. The choices include the LM7805CT, LM7809CT, LM7812CT, LM7815CT, LM7818CT and the LM7824CT. The “LM” in the part number stands for Linear Monolithic. The “CT” suffix specifies the precision and case style. Some manufacturers may use a different prefix.
- 4-87 Recall the last two digits specify the nominal output voltage. The correct choice is an LM7818CT. A partial data sheet is given in Fig. 4-85. This manufacturer uses an MC prefix. An MC7818CT is equivalent to an LM7818CT. The output voltage can range from 17.3 to 18.7 V. **While the typical dropout voltage is 2 V, an application note indicates a maximum dropout voltage of 3.5 V.** The integrated circuit includes short-circuit protection. This means if there is a failure in the external load such that it forms a short-circuit to ground, the fault current is limited to 200 mA. **Find the data sheet for the part using an internet search engine. Locate the output voltage range, the dropout voltage and the short-circuit current.**
- 4-88 Use Eq. 4-51 to determine $V_{dc(min)}$. If the minimum instantaneous voltage gets too low, ripple voltage will begin to appear at the output of the voltage regulator and its output voltage will decrease as the load current increases. It will no longer be in regulation.
- 4-89 Equation 4-33 (repeated below) defines the condition for light loading. The ripple voltage makes an excursion from $V_{dc(min)}$ to V_{dcm} and V_{DC} is centered between these two boundaries. We can extend light loading to be expressed in terms of $V_{dc(min)}$ and $V_{r(p-p)}$.

$$V_{dc(min)} \geq 0.8V_{dcm}$$

$$V_{DC} \geq 0.9V_{dcm}$$

$$V_{r(p-p)} \leq 0.2V_{dcm}$$

Use $V_{dc(min)}$ found in Prob. 4-88 to find V_{dcm} under the condition of light loading.

MC7800, MC7800A, MC7800AE, NCV7800

1.0 A Positive Voltage Regulators

These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

Features

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 1.5%, 2% and 4% Tolerance
- Available in Surface Mount D²PAK-3, DPAK-3 and Standard 3-Lead Transistor Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices



TO-220
T SUFFIX
CASE 221AB

Heatsink surface
connected to Pin 2.



Pin 1. Input
2. Ground
3. Output

D²PAK-3
D2T SUFFIX
CASE 936

Heatsink surface (shown as terminal 4 in
case outline drawing) is connected to Pin 2.



DPAK-3
DT SUFFIX
CASE 369C

MC7800, MC7800A, MC7800AE, NCV7800

ELECTRICAL CHARACTERISTICS ($V_{in} = 27\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to 125°C (Note 27), unless otherwise noted)

Characteristic	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = 25^\circ\text{C}$)	V_O	17.64	18	18.36	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$) $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$	V_O	17.3	18	18.7	Vdc
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_A = 25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{SC}	—	0.2	—	A

Figure 4-85.

4-90 Since a full-wave bridge rectifier is to be used (Fig. 4-84), we use Eq. 4-24 to find the transformer peak secondary voltage V_m using the peak rectified voltage V_{dcm} determined in Prob. 4-89.

4-91 Compute the rms value of the transformer secondary voltage. Use a 20% safety margin to determine the transformer secondary voltage V_2 .

$$V_2 = 1.2 \frac{V_m}{\sqrt{2}}$$

4-92 Determine the required transformer secondary current rating using Table 4-2. Based on the results of Probs. 4-90 and 4-91 a **Triad F24-250-C2** transformer is specified. A partial data sheet is given in Fig. 4-86. Use the data sheet and Eq. 4-15 to determine the no-load rms secondary voltage V_{NL} .

4-93 Find the equivalent resistance (R_S) that can be used to model the transformer's voltage regulation. Refer to Fig. 4-22.

4-94 Determine the no-load V_{dcm} and the full-load V_{dcm} based on the transformer's voltage regulation. Use the no-load V_{dcm} to determine the minimum voltage rating of the filter capacitor. Equation 4-27 applies a 20% safety factor.

F24-250-C2

Description:

The F24-250-C2 is a single primary and dual secondary, split bobbin design which operates with an input of 115V. The secondaries are 12V @ 0.25A each. They can be used independently (up to 300V difference between them) or in series for double the voltage or in parallel for double the current. The split bobbin design eliminates the need for costly electrostatic shielding.

Electrical Specifications (@25C)

1. Maximum Power: 6.0VA
2. Primary: 115V
3. Secondaries: 12.0V @ 0.25A each
4. Voltage Regulation: 25% TYP @ full load to no load
5. Temperature Rise: 25C TYP
6. Hipot tested 100% at 4200 VRMS pri to sec
7. Hipot tested 100% at 2160 VRMS sec to sec
8. Recommended fuse (fuse on primary): Cooper/Bussman, Type MDL, rated 500mA, 250V

Construction:

Three flange bobbin construction with primaries and secondaries wound side by side for low capacitive coupling. UL Class F Insulation System (155°C).

Dimensions:

Units in inches.

H	W	L	A	B	C	D	E	F
1.398 MAX	1.331 MAX	1.650 MAX	0.250±0.02	0.350±0.02	1.280±0.02	0.041	0.020	0.217±0.02

Weight: 0.44 lbs

Schematic:

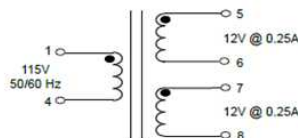


Figure 4-86.

- 4-95 Find the minimum value for the filter capacitor capacitance for light loading under full-load conditions. Employ the peak-to-peak ripple relationship provided in Prob. 4-89 and solve Eq. 4-37 for C . Use $1.2C$ to determine the required capacitor value. A suitable (20% safety factor) capacitor manufactured by Nichicon is indicated in Fig. 4-87.
- 4-96 Calculate the rms ripple current that effectively flows through the selected $220\text{-}\mu\text{F}$ filter capacitor. First, calculate the peak-to-peak ripple voltage using Eq. 4-37. Next, find $V_{dc(\min)}$ under full conditions. Use Eq. 4-45 to find the charge time t_c . Equation 4-42 is used to find the peak repetitive diode surge current $I_{D(PK)}$. Use Eq. 4-48 to find the capacitor ripple current $I_{r(rms)}$. Is the capacitor ripple current rating Fig. 4-87 adequate?

ALUMINUM ELECTROLYTIC CAPACITORS

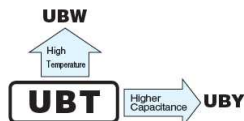
nichicon

UBT

High Temperature Range, For $+125^\circ\text{C}$ Use



- Highly dependable reliability withstanding load life of 2000 to 10000 hours at $+125^\circ\text{C}$.
- Suited for automobile electronics where heavy duty services are indispensable.
- Compliant to the RoHS directive (2011/65/EU).
- AEC-Q200 compliant. Please contact us for details.



Specifications

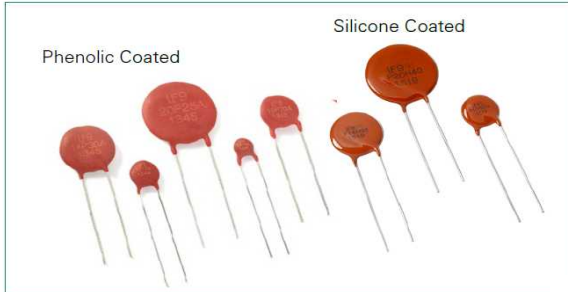
Cap. (μF)	V (Code) Item	10 (1A)			16 (1C)			25 (1E)			35 (1V)			50 (1H)		
		Case size $\phi D \times L$ (mm)	Impedance (Ω) MAX.	Rated ripple (mA rms)	Case size $\phi D \times L$ (mm)	Impedance (Ω) MAX.	Rated ripple (mA rms)	Case size $\phi D \times L$ (mm)	Impedance (Ω) MAX.	Rated ripple (mA rms)	Case size $\phi D \times L$ (mm)	Impedance (Ω) MAX.	Rated ripple (mA rms)	Case size $\phi D \times L$ (mm)	Impedance (Ω) MAX.	Rated ripple (mA rms)
4.7	4R7															
10	100													8 × 11.5	1.15	85
22	220													8 × 11.5	0.75	180
33	330													8 × 11.5	0.50	250
47	470													8 × 11.5	0.45	300
														8 × 11.5	0.35	440
100	101				8 × 11.5	0.32	340	8 × 11.5	0.13	500	10 × 12.5	0.15	620	10 × 12.5	0.18	555
220	221	8 × 11.5	0.26	340	10 × 12.5	0.15	620	10 × 12.5	0.10	680	10 × 16	0.094	790	10 × 20	0.098	930
330	331	10 × 12.5	0.15	620	10 × 12.5	0.10	680	10 × 16	0.075	945	10 × 20	0.075	950	12.5 × 20	0.070	1330
470	471	10 × 12.5	0.10	680	10 × 16	0.075	945	10 × 20	0.057	1100	12.5 × 20	0.058	1330	12.5 × 25	0.055	1650
1000	102	10 × 20	0.057	1100	12.5 × 20	0.049	1400	12.5 × 25	0.033	1750	16 × 25	0.031	2010	16 × 31.5	0.031	2430

Figure 4-87 Partial Data Sheet Courtesy of Nichicon.

- 4-97 In Chapter 3, Section 3-5, varistors are introduced. A varistor can be placed across the transformer primary to limit (or clamp) power line voltage transients. The part selected here is a Littelfuse 14H150A. A partial datasheet is shown in Fig. 4-88. What is its maximum rms voltage rating? (This would be the voltage across it before it starts protection by conducting current.) If the transient condition lasts too long, or another (down-stream) failure occurs, the fuse (F1) shown in Fig. 4-89 will open.
- 4-98 Switch (S1) in Fig. 4-89 is a single-pole, single-throw (SPST) toggle switch. It is the ON/OFF switch for the DC power supply. The (green) LED is the power-on indicator. It drops a voltage of about 2 volts. Resistor R1 limits the current through it. Calculate the LED current.

AUMOV® Varistor Series

AUTOMOTIVE GRADE RoHS Pb HF



Description

The Littelfuse AUMOV® Varistor Series of low voltage, high surge current, radial leaded varistors provides an ideal circuit protection for load dump, jump start voltage transient conditions specifically for automotive applications.

The maximum peak surge current rating is rated up to 5kA (8/20 μ s pulse) to protect sensitive infotainment systems from voltage transients. This AEC-Q200 (Table 10) qualified series is available in five disc sizes: 5mm, 7mm, 10mm, 14mm and 20mm; it features a wide VDC voltage range from 16V to 825V.

AUMOV® Varistor Series Device Ratings & Specifications

Phenolic Coated Models		Silicone Coated Models		Size Disc Dia. (mm)	Max Continuous Voltage		Varistor Voltage at 1mA			Maximum Clamping Voltage		Max Peak Current (8 x 20 μ s 1 pulse)	Energy Rating (2ms, 1 pulse)	Energy (Load Dump, 10 pulses)*	Jump Start DC V _{jump} (5 min)	Typical Capacitance f = 1MHz
Part Number (Base part)	Branding	Part Number (Base part)	Branding		V _{RMS} (V)	V _{DC} (V)	Min (V)	Nom (V)	Max (V)	V _C (V)	I _{PK} (A)					
V20P130AUTO	20P130A	V20H130AUTO	20H130A	20	130	170	184.5	205	225.5	340	100	10000	145	-	-	1900
V10P140AUTO	10P140A	V10H140AUTO	10H140A	10	140	180	198	220	242	360	25	3500	45	-	-	400
V14P140AUTO	14P140A	V14H140AUTO	14H140A	14	140	180	198	220	242	360	50	6500	65	-	-	900
V20P140AUTO	20P140A	V20H140AUTO	20H140A	20	140	180	198	220	242	360	100	10000	155	-	-	1750
V10P150AUTO	10P150A	V10H150AUTO	10H150A	10	150	200	216	240	264	395	25	3500	50	-	-	360
V14P150AUTO	14P150A	V14H150AUTO	14H150A	14	150	200	216	240	264	395	50	6500	70	-	-	800
V20P150AUTO	20P150A	V20H150AUTO	20H150A	20	150	200	216	240	264	395	100	10000	165	-	-	1600
V10P175AUTO	10P175A	V10H175AUTO	10H175A	10	175	225	243	270	297	455	25	3500	55	-	-	350

Figure 4-88 Partial Data Sheet Courtesy of Littelfuse.

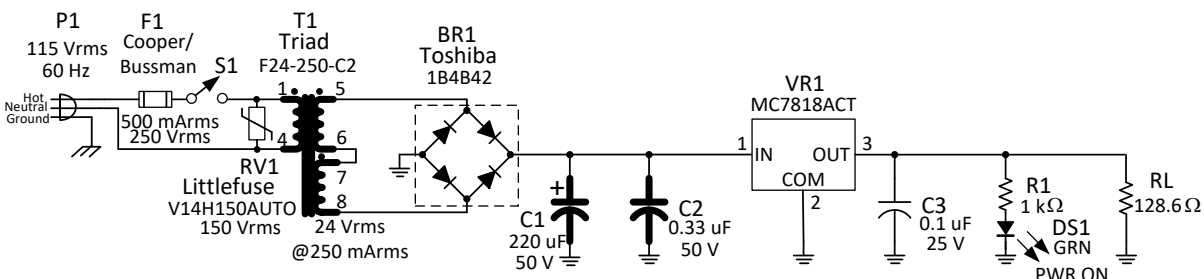


Figure 4-89 Complete DC Power Supply Design.

5

Bipolar Junction Transistors

In 1947, W. H. Brattain and J. Bardeen, both of Bell Laboratories, brought two closely-spaced metallic needles into contact with the same germanium “base” wafer. The two needle-like electrodes were called the *emitter* and *collector* terminals. A third *base* terminal was also connected to the germanium crystal. Their initial experiments demonstrated that varying either the base or the emitter terminal currents produced a proportional variation in the voltage level measured between the collector and base terminals. Since an *input* (base or emitter) current could be used to control the *output* (collector) voltage, the *gain* (input-to-output transfer) across the device can be described as

$$\text{Gain} = \frac{\text{Output Voltage}}{\text{Input Current}}$$

This gain relationship has units of ohms. Consequently, another researcher, J. R. Pierce (also of Bell Laboratories), described the device as being a transfer resistor and coined the term *transistor*. In 1949, William Shockley provided a theoretical description of the *bipolar junction transistor*, or *BJT*. The BJT revolutionized the electronics industry. Not only did it serve to render vacuum tubes obsolete, but the search for improved transistor manufacturing techniques established the basis for modern integrated-circuit fabrication. Today, the integrated circuit is pushing the discrete BJT into obsolescence in many applications. Many new electronic designs are a combination of both linear integrated circuits and discrete transistors. We need to be comfortable with both of these electronic “tools”. The specific topics covered in this chapter include

- The Basic BJT Structure
- Unbiased Transistors
- BJT Operation
- BJT Connections and Current Gain
- Leakage Currents
- The Transistor Convention
- *V-I* Curves
- Finding the Q Point
- The BJT Amplifier
- The Transistor Switch
- The Clapper

The *Clapper* is the name we have given to a toy robot. It spins when it “hears” a loud clap. Transistor switches are fundamental to its operation. It’s an entertaining way to learn.

5-0 Study Objectives

After completing this chapter, you should be able to:

- Describe the basic structure of the BJT and identify the *npn* and *pnp* schematic symbols.
- Explain the formation of the *p-n* junctions within the BJT.
- Explain the basic operation of the BJT, and describe how the charge carriers move through it.
- Name and define the CE, CB, and CC configurations.
- Define the current gains β_{DC} and α_{DC} .
- Explain the leakage currents associated with the BJT.
- Apply the transistor convention.
- Generate and interpret V - I curves.
- Use Multisim to create BJT V - I curves.
- Analyze a simple transistor amplifier circuit to find its Q point.
- Explain the operation of a common-emitter amplifier.
- Analyze a transistor switch.
- Explain the operation of the transistor switches used in a toy robot called the *Clapper*.

5-1 The Basic BJT Structure

The ubiquitous³⁹ transistor is illustrated in Fig. 5-1 (circa 1970's). Most new designs use integrated circuits whenever and wherever possible. Discrete transistors are used only when it becomes cost-effective to do so. They are often selected to embellish the performance of an integrated circuit.

The Discrete BJT Circuit

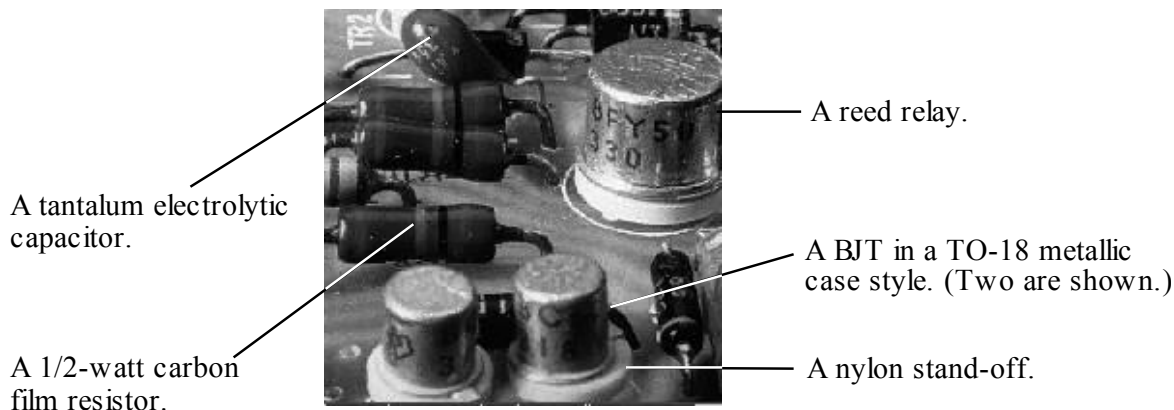


Figure 5-1.

We need to develop the skills necessary to analyze BJTs in discrete designs as well as their application in combination with integrated circuits. Further, by understanding the discrete BJT, we shall also better grasp the capabilities and inherent limitations of integrated circuits.

³⁹ *Ubiquitous* means universal, used everywhere, or omnipresent. This is the perfect description of the BJT.

There are two fundamental types of BJTs *npn* and the *pnp*. The basic structures are depicted in Fig. 5-2. The *npn* BJT in Fig. 5-2(a) has an *n*-type emitter region that is doped heavily. Consequently, it is designated as being n^+ . The base region is very thin and doped moderately with acceptor impurities. This makes it a *p* region. The collector region is the largest of the three and is doped very lightly (n^-). As can be seen in Fig. 5-2(a), the BJT has two *p-n* junctions. One exists between the emitter and base terminals. A second *p-n* junction exists between the base and collector terminals. The *pnp* BJT is a complementary device as shown in Fig. 5-2(c).

The corresponding schematic symbols are illustrated in Fig. 5-2 (b) and (d). ***In virtually all schematic symbols for solid-state electronic devices, the arrow always points to the *n*-type material.*** Some prefer the memory aid: the arrow for the *npn* BJT is **Not Pointing iN**.

NPN and PNP BJT Structures and Symbols

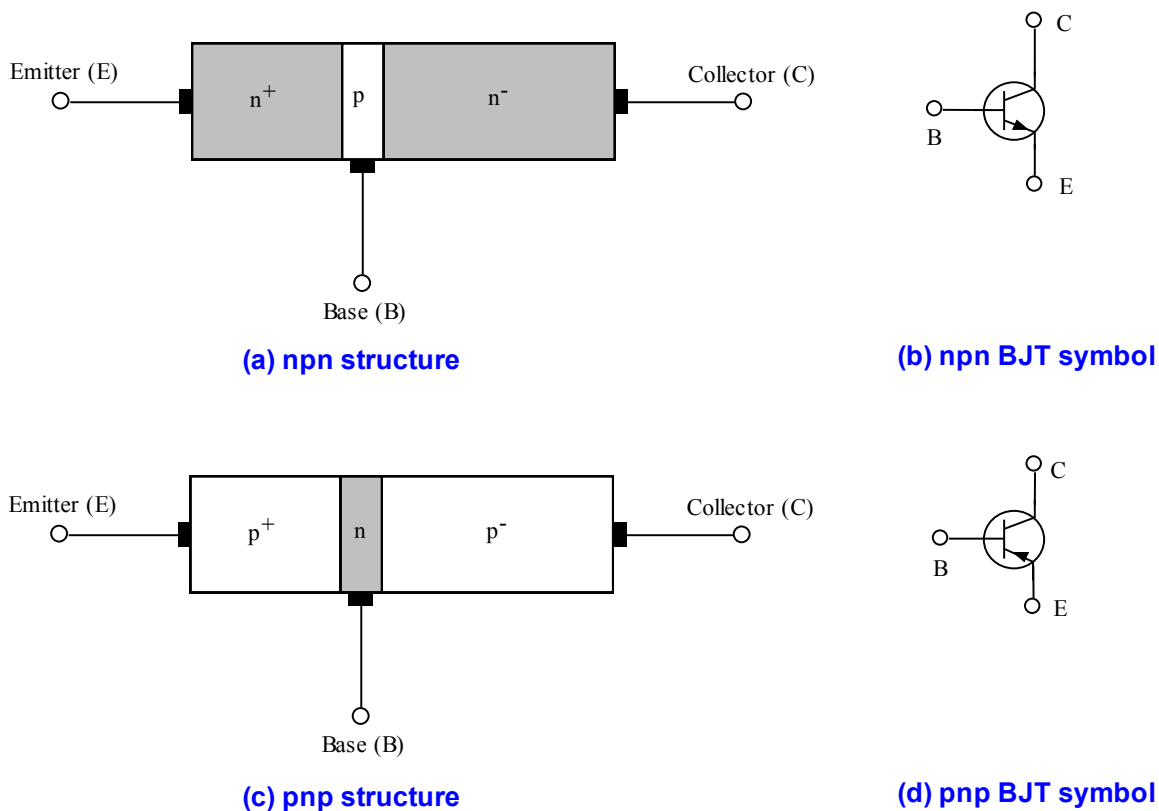


Figure 5-2.

5-2 Unbiased Transistors

Recall that when a semiconductor has been doped with pentavalent (donor) impurity atoms, it becomes an *n*-type semiconductor. In an *n*-type semiconductor, free electrons are the majority carriers. When a semiconductor has been doped with trivalent (acceptor) impurities, it becomes a *p*-type semiconductor. In a *p*-type semiconductor, holes are the majority carriers. When a *p-n* junction is formed, a layer of *n*-type semiconductor is placed next to a layer of *p*-type semiconductor.

Electrons on the n -side diffuse across the p - n junction. After they cross the junction, they lose energy and recombine with the holes on the p -side. Consequently, a layer of positive ions is left on the n -side and a layer of negative ions forms on the p -side. The resulting build-up of electrical charge forms the barrier potential that stops the diffusion process.

The ionized regions are called depletion regions since they have been depleted of their majority charge carriers. Depletion regions extend into the semiconductor crystal as a function of the doping levels. This means the depletion region extends slightly into heavily-doped semiconductors (e.g., n^+) and extends much further into lightly-doped semiconductors (e.g., n^-). The depletion regions are illustrated in Fig. 5-3. The *effective base region* lies between the depletion region edges and is very narrow.

Unbiased Transistor Depletion Regions

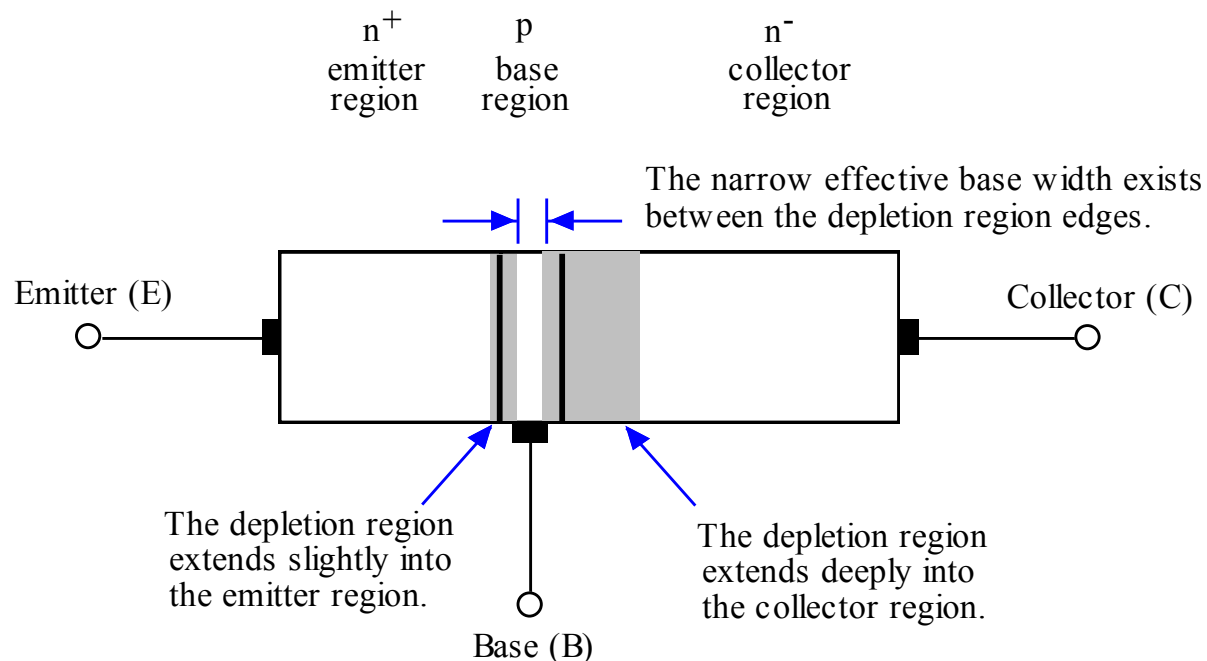


Figure 5-3.

5-3 BJT Operation

To be used as an active (amplifying) device, the emitter-base p - n junction must be forward biased, while the collector-base p - n junction must be reverse biased. This is true for both the n pn and the p np transistors. These biasing conditions are shown in Fig. 5-4 for an n pn BJT. To forward bias a p - n junction the supply positive terminal is connected to the p -material. (That's positive to p .) To reverse-bias a p - n junction, the supply positive terminal is connected to the n -side of the p - n junction. (That's positive to n .) Also, recall that a forward bias tends to make the depletion region around a p - n junction narrower. Reverse bias tends to widen the depletion region. In the case of the BJT, the adjustment in the depletion region widths tends to reduce the effective base width. This is because the increase in the reverse-biased collector-base depletion region tends to be larger than the decrease in the forward-biased emitter-base depletion region. The significance of the narrow base region will be explained shortly.

Two DC voltage sources have been indicated. V_{EE} is the *emitter supply*.⁴⁰ It provides the forward emitter-base bias. *Emitter resistor* R_E is used to limit the emitter current flow. Similarly, V_{CC} is the *collector supply*, which is used to provide the required reverse collector-base bias. *Collector resistor* R_C restricts the maximum collector current to a safe value. Let us trace the flow of electrons through the n pn transistor.

Biasing the BJT

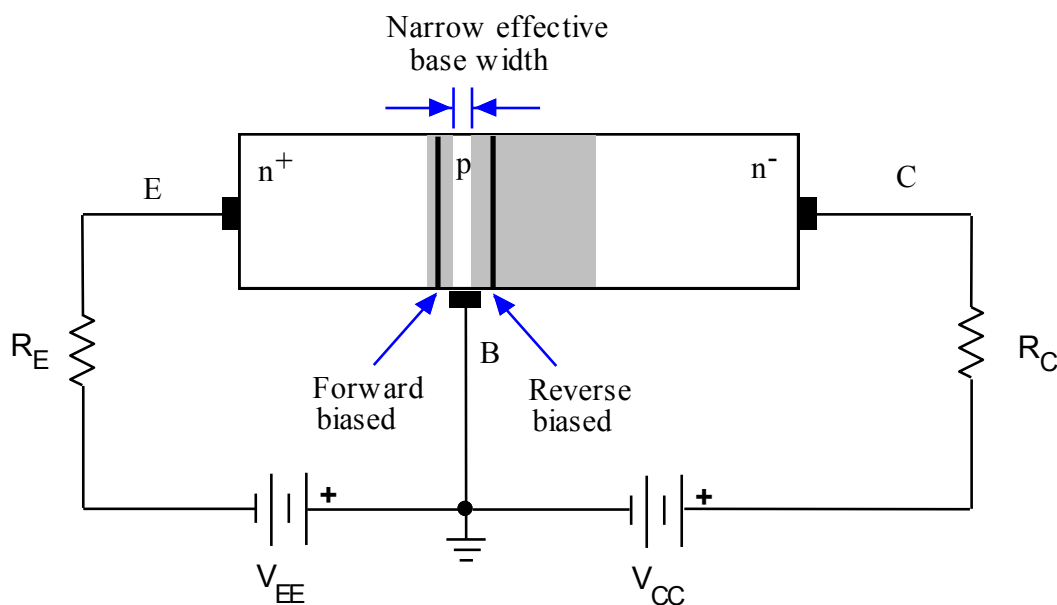


Figure 5-4.

⁴⁰ In basic circuit analysis double subscript notation is used widely. It is applied to transistors too. For example, V_{CB} is the voltage at the collector terminal relative to the base terminal. In the case of a single subscript, the reference point is ground. V_C is the voltage at the collector terminal relative to ground. The notation V_{CC} is silly. The voltage at terminal C relative to terminal C is zero. This is demonstrated easily by shorting the two probes of a digital multimeter adjusted to measure voltage together. It will read zero. If it doesn't return it to the vendor and insist on a full refund. The otherwise laughable nature of V_{CC} and V_{EE} made them a great choice for denoting DC voltage supplies. It is consistent throughout the industry.

As we see in Fig. 5-5 (a), the emitter supply V_{EE} provides a forward bias on the emitter-base p - n junction. Consequently, conduction-band electrons leave the negative terminal of V_{EE} and are injected into the emitter region. Recall that forward-bias causes the majority carriers to move toward the p - n junction. Provided the external bias (e.g., V_{EE}) is large enough to overcome the barrier potential, the electrons will move across the p - n junction to enter the base region. This is shown in Fig. 5-5(b).

Basic Operation of an NPN BJT

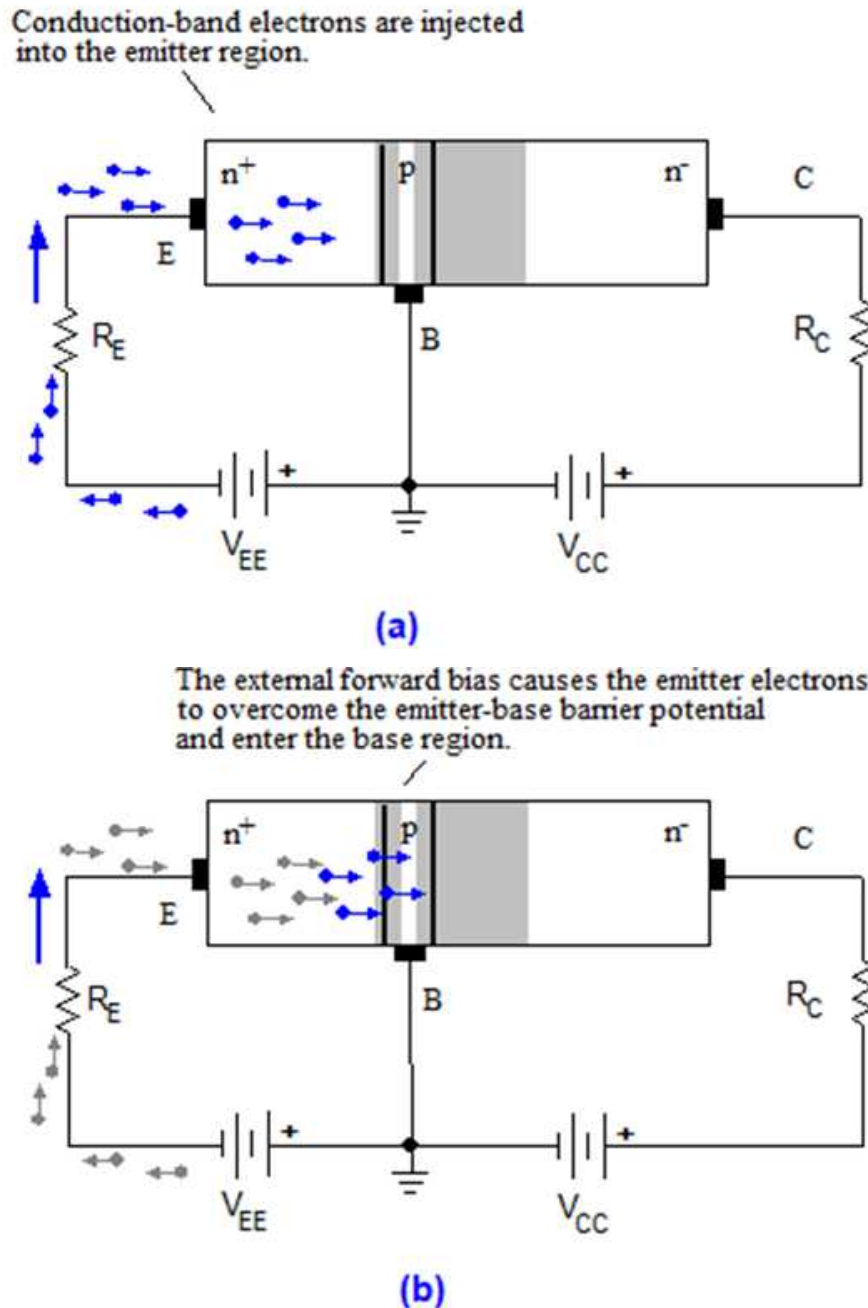


Figure 5-5.

The Base Current is *Small*, and the Collector Current is *Large*!

Most beginning electronics students would assume the base current must be large because it is associated with the forward-biased emitter-base p - n junction. Further, it would also seem likely that the collector current must be small because it is associated with the reverse-biased collector-base p - n junction. However, the *opposite* is true! The base current is very small, and the collector current is large and very nearly equal to the emitter current. Before you decide to give up electronics, find a lawyer and sue this author, let's find out why this true.

There are two reasons why this occurs. First, the base region is lightly doped relative to the emitter. This means there simply are not enough holes to capture the “flood” of electrons from the emitter region. Second, the base is very thin. When electrons enter the base region, they are affected by the collector-base depletion region. They are swept across it to enter the collector region. The principle is similar to the leakage current that flows through a reverse-biased diode. When electrons enter the (p -type) base region, they become minority carriers. Minority carriers near a depletion region tend to be swept across it. In this case, they are “collected” by the collector region. This action is depicted in Fig. 5-5(c).

The carriers in the collector region are drawn into the external circuit by the collector supply V_{CC} as indicated in Fig. 5-5(d). Also, note in Fig. 5-5(d) that three (electron-flow) currents have been defined.

The emitter current is called I_E , the base current is I_B , and the collector current is labeled I_C . The BJT must obey Kirchhoff's current law. Specifically, the emitter current is equal to the sum of the collector and base currents. This leads us to Eq. 5-1.

$$I_E = I_C + I_B \quad (5-1)$$

Because the base current so small, the first-order approximation given by Eq. 5-2 is used extensively.

$$I_E \cong I_C \quad (5-2)$$

Basic Operation of an NPN BJT (continued)

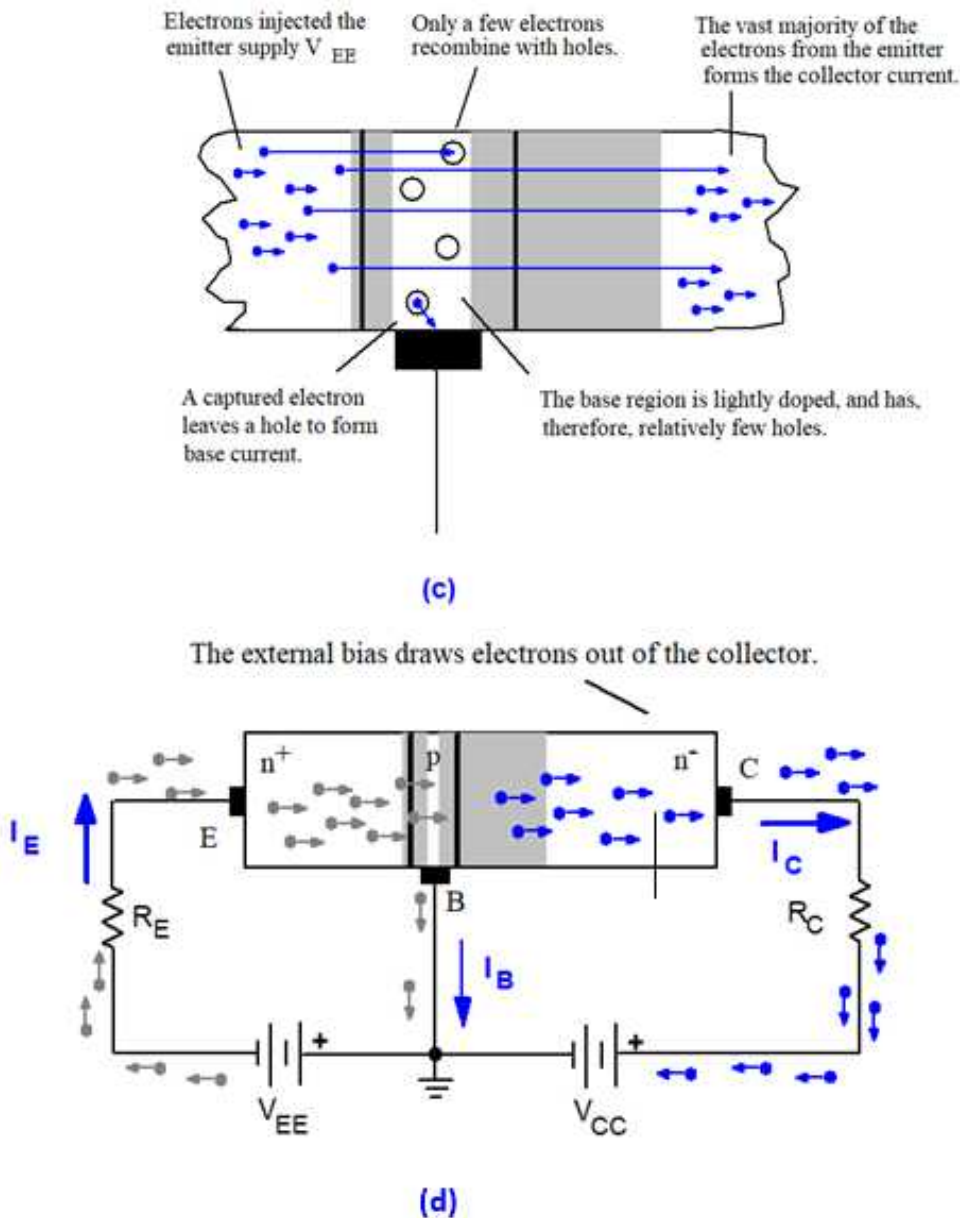


Figure 5-5 (continued).

The Base-Emitter Forward Bias Controls the Collector Current

The forward base-emitter bias controls the collector current. Refer to Fig. 5-6. As the forward bias applied to the base-emitter p - n junction is increased, the collector current will also increase. When the base-emitter bias is increased the voltage V_{BE} across the base-emitter p - n junction will increase. There will also be an increase in the base and emitter currents.

The transistor can be viewed in *three* different ways. First, we can consider V_{BE} to be the controlling quantity. Second, we can also consider the transistor's collector current to be controlled by the emitter current I_E . Third, it is also correct to regard the base current I_B to be the controlling quantity.

Conventional current directions have been indicated in Fig. 5-6. The double subscript notation means the voltage at the first terminal relative to the second terminal listed. Consequently, V_{BE} means the voltage at the base terminal (B) with respect to the emitter terminal (E). If V_{BE} is 0.7 V, then V_{EB} will be -0.7 V. Think about this. ***If the base is 0.7 V more positive than the emitter, then the emitter must be -0.7 V with respect to the base.*** Equation 5-3 is based on these concepts.

$$V_{BE} = -V_{EB} \quad (5-3)$$

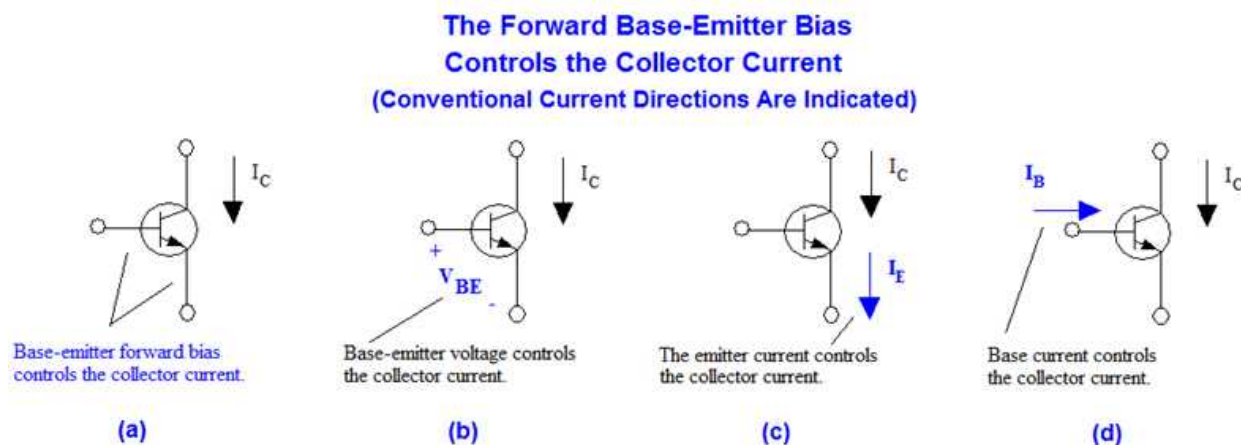


Figure 5-6.

Why is the Collector Region the Largest?

The operation of the BJT can also be examined by means of its energy diagram. Recall from Chapter 1 that forward bias tends to align the valence and conduction energy bands, while reverse bias tends to increase the misalignment. In the case of the BJT with its forward-biased emitter-base p - n junction, and its reverse-biased collector-base p - n junction, we arrive at the energy diagram provided in Fig. 5-7.

Conduction-band electrons from the emitter supply (V_{EE}) enter the emitter region. These electrons overcome the small potential barrier associated with the forward-biased, emitter-base p - n junction. A few of the electrons in the base region lose enough energy such that they fall into the holes located in the valence-energy band. These electrons are captured by the holes. The captured electrons are ultimately liberated by V_{EE} to form the base current.

The majority of the electrons from the emitter form collector current. They are “swept across” the depletion region associated with the reverse-biased collector-base p - n junction. Consequently, the electrons give up a large amount of energy as they travel from the base region to the collector region. Typically, the electrons give up their energy in the form of heat. Consequently, the collector region must be able to dissipate this heat energy.

It is for this reason that it is the largest of the three regions. Further, it is normal to find the collector bonded to a metallic header to promote heat radiation. This illustrated in Fig. 5-8. It is for this reason that it is the largest of the three regions. Further, it is normal to find the collector bonded to a metallic header to promote heat radiation. This illustrated in Fig. 5-8.

The Basic Construction of a Bipolar Junction Transistor

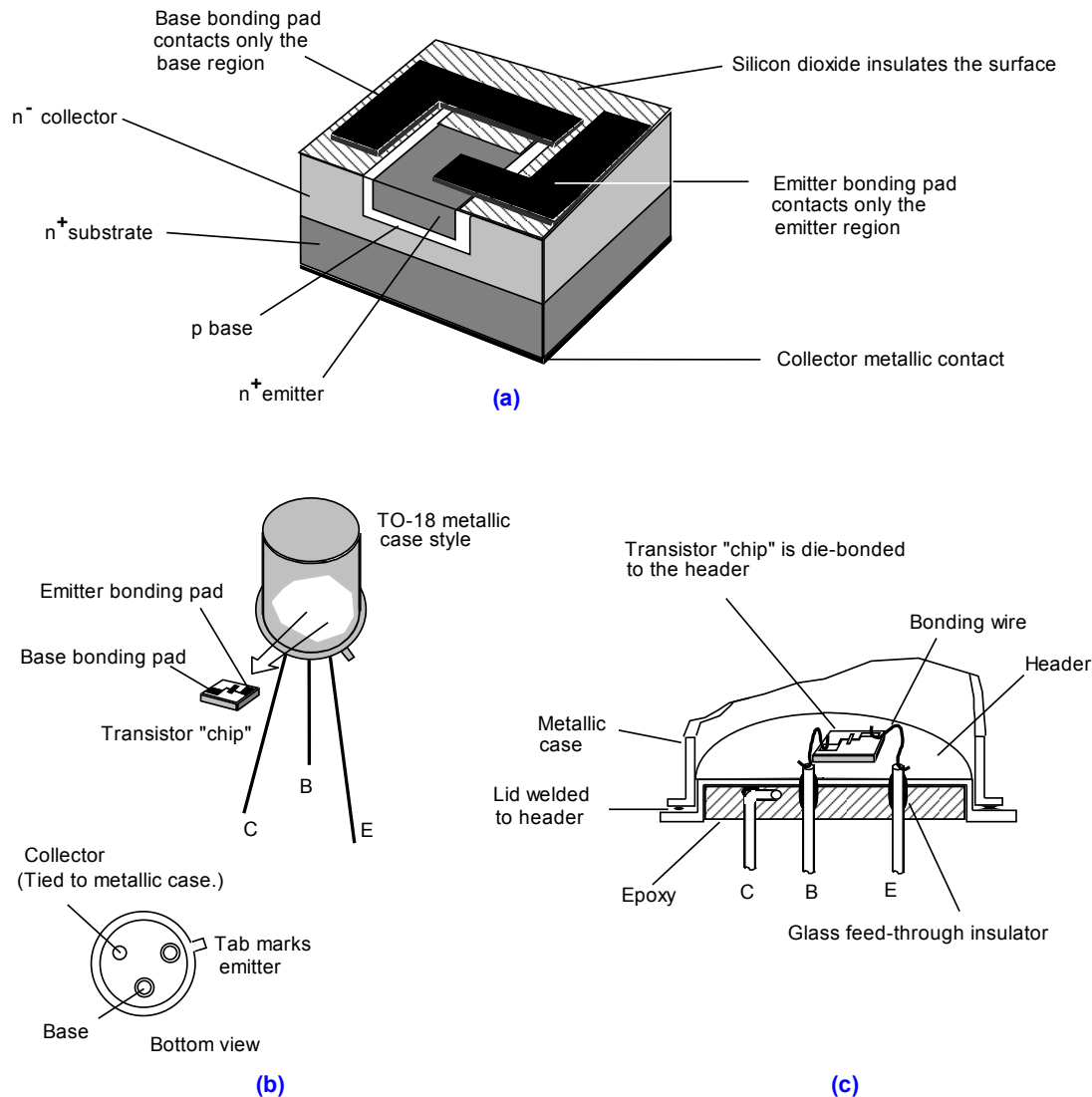


Figure 5-8.

In Fig. 5-8(a) we see the construction of the transistor “chip”. Aluminum is vacuum-deposited on the silicon structure to make the base and emitter bonding pads. In Fig. 5-8(b) we see the transistor chip is contained within the transistor package. A TO-18 metallic case style has been illustrated. Its bottom view has also been indicated. Figure 5-8(c) shows the construction details. The collector is tied to the substrate (which is heavily doped n^+ to act like a semiconductor extension of an electrical conductor). The substrate is die-bonded to the metallic header.

The collector terminal is butt-welded to the header, and the header is welded to the metallic case. There are two important ideas here. First, the collector is tied electrically to the metallic case. Second, this is done to help the collector region to radiate the heat built-up within it.

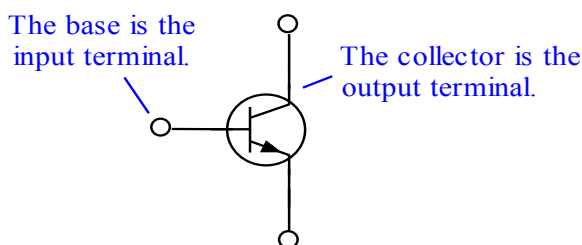
5-4 BJT Connections and Current Gain

The BJT has three distinct possible connections, when used as an amplifier. They are called the **common-emitter**, **common-base**, and **common-collector** configurations. Many beginning students assume that the “common” terminal is tied directly to ground in each case. *This is not always true.* The particular configuration depends on the choice of the input and output terminals. An input signal will be applied to the input terminal with respect to ground. Similarly, the output signal will be extracted from the output terminal with respect to ground. The three configurations are summarized in Table 5-1 and in Fig. 5-9. These should be memorized.

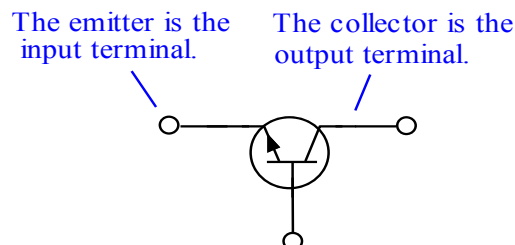
Table 5-1. BJT Amplifier Connections

Configuration Name	Input Terminal	Output Terminal
Common Emitter	Base	Collector
Common Base	Emitter	Collector
Common Collector	Base	Emitter

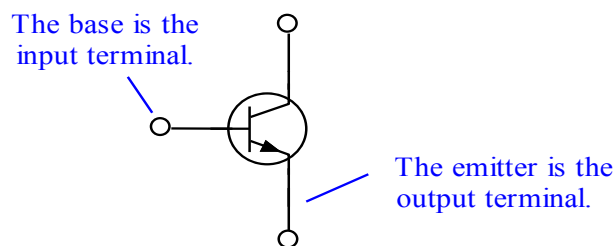
BJT Amplifier Connections



(a) common emitter



(b) common base



(c) common collector

Figure 5-9.

The Current Gain for a BJT in its Common-Emitter Configuration

When the energy input to a system affects its energy output in some fashion, we often need to define the interaction between the two quantitatively. The *transfer function* describes the relationship between the input and output. In its simplest form, a transfer function is the ratio of some output quantity to the corresponding input quantity. In many instances, this ratio is referred to as a *gain*. The use of the term gain implies that the output quantity must be larger than the input quantity. **However, this is not always the case.**

Current gain is defined by Eq. 5-4. It is the ratio of the output current to the input current.

$$\text{Current gain} = \frac{\text{Output current}}{\text{Input current}} \quad (5-4)$$

In the case of the common-emitter configuration, the current gain is given a special symbol (the Greek letter) β_{DC} and is called “the dc beta”⁴¹. Since the output terminal is the collector, and the input terminal is the base, the current gain is the ratio of the collector current to the base current.

$$\beta_{DC} = \frac{I_C}{I_B} \quad (5-5)$$

This DC current gain is often denoted as h_{FE} on manufacturers’ data sheets. The nomenclature h_{FE} is described as the **hybrid parameter, Forward DC current gain for the common-Emitter BJT**. Note this current gain applies to *npn* and *pnp* BJTs equally. This is indicated in Fig. 5-10. **An “input” current controls, while the “output” current is controlled. The input and output adjectives do not refer to the actual current directions.**

The Current Gain for a BJT in its Common-Base Configuration

The common-emitter BJT configuration is the most popular. Consequently, the majority of BJT data sheets will include minimum and typical values of h_{FE} . Occasionally, manufacturers will specify the current gain for a BJT in its common-base configuration. This gain is denoted as h_{FB} (**hybrid parameter, Forward DC current gain, common Base**). The symbol used for common-base current gain is the Greek letter alpha (α). The DC alpha is given by Eq. 5-6.

$$\alpha_{DC} = \frac{I_C}{I_E} \quad (5-6)$$

Again, we see in Fig. 5-10(b) that this current gain applies to both *npn* and *pnp* BJTs. Equations 5-1, 5-5, and 5-6 can be used to determine the BJT terminal currents as the examples that follow illustrate.

⁴¹ The DC subscript is used to help distinguish the (common emitter) *DC current gain* β_{DC} from the *AC current gain* β . The same convention is used for the (common-base) current gain. The DC current gain is designated α_{DC} , while the AC current gain is called α .

BJT Current Gains

- Conventional current directions are shown.
- "Input" currents can flow in or out of the BJT.
- "Input" currents control the "output" currents.
- "Output" currents can flow in or out of the BJT.

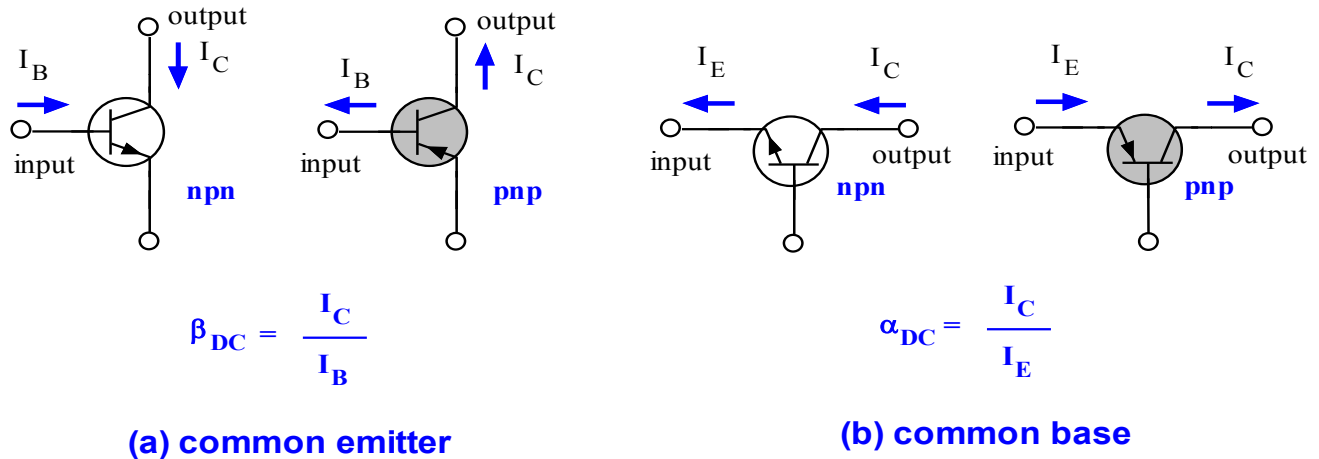


Figure 5-10.

Example 5-1. The *npn* BJT in Fig. 5-10(a) has a base current of 20 μA and a collector current of 2 mA. Calculate its β_{DC} , emitter current I_E , and its α_{DC} .

Solution: We apply Eq. 5-5 to determine its β_{DC} .

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{2 \text{ mA}}{20 \mu\text{A}} = 100$$

The emitter current is found by using Eq. 5-1.

$$I_E = I_C + I_B = 2 \text{ mA} + 20 \mu\text{A} = 2 \text{ mA} + 0.02 \text{ mA} = 2.02 \text{ mA}$$

Equation 5-6 provides us with the BJT's α_{DC} .

$$\alpha_{DC} = \frac{I_C}{I_E} = \frac{2 \text{ mA}}{2.02 \text{ mA}} = 0.990$$

The results of this example may be used to produce some important generalizations about the operation of the BJT. Because the base current is small, the β_{DC} tends to be large. Typical values range from 20 to about 400. A high value of β_{DC} is desirable. Because the emitter current is *always* greater than the collector current, α_{DC} must *always* be less than unity (1). An α_{DC} that is equal to one (1) is ideal.

Example 5-2. A transistor has a base current (I_B) of 50 μA and an α_{DC} of 0.993. Determine its collector current (I_C).

Solution: We have not yet developed a relationship between I_B , α_{DC} , and I_C . However, by using the relationships developed thus far and a little algebra, we can solve this problem. First, we solve Eq. 5-6 for I_C .

$$I_C = \alpha_{DC} I_E$$

Next, we substitute Eq. 5-1 ($I_E = I_C + I_B$) in for I_E and distribute α_{DC} .

$$I_C = \alpha_{DC} I_E = \alpha_{DC} (I_C + I_B) = \alpha_{DC} I_C + \alpha_{DC} I_B$$

Now we move the I_C term to the left-hand side of the equation and factor out I_C .

$$I_C - \alpha_{DC} I_C = \alpha_{DC} I_B$$

$$I_C (1 - \alpha_{DC}) = \alpha_{DC} I_B$$

To solve for I_C , we divide both sides by $(1 - \alpha_{DC})$.

$$I_C = \frac{\alpha_{DC}}{1 - \alpha_{DC}} I_B$$

We finish the problem requirements by substituting in the appropriate values.

$$I_C = \frac{\alpha_{DC}}{1 - \alpha_{DC}} I_B = \frac{0.993}{1 - 0.993} (50 \mu\text{A}) = 7.09 \text{ mA}$$

Example 5-2 would have been a lot easier if we had been given β_{DC} since $I_C = \beta_{DC} I_B$. With one more algebraic step, we can arrive at the relationship between α_{DC} and β_{DC} . From Example 5-2, we obtain the equation for I_C .

$$I_C = \frac{\alpha_{DC}}{1 - \alpha_{DC}} I_B$$

Dividing both sides by I_B yields Eq. 5-7.

$$\boxed{\beta_{DC} = \frac{I_C}{I_B} = \frac{\alpha_{DC}}{1 - \alpha_{DC}}} \quad (5-7)$$

Since $\beta_{DC} = \alpha_{DC} / (1 - \alpha_{DC})$ we can solve this for α_{DC} to obtain Eq. 5-8. (*The required algebra is left as an exercise for the student.*)⁴²

⁴² They teach us this rather nasty phrase in Professor school. This means it will show up in a home-work problem, or maybe even in a quiz. Try it.

$$\alpha_{DC} = \frac{I_C}{I_E} = \frac{\beta_{DC}}{1 + \beta_{DC}} \quad (5-8)$$

Example 5-3. A transistor has an emitter current (I_E) of 5 mA and a β_{DC} of 250. Determine its base current (I_B).

Solution: If we obtain a value for α_{DC} , we can then find I_C . Once I_C is known, it is relatively easy to find I_B . First, we apply Eq. 5-8.

$$\alpha_{DC} = \frac{\beta_{DC}}{1 + \beta_{DC}} = \frac{250}{1 + 250} = 0.996$$

Now we find I_C by using 5-6 (which has been solved for I_C).

$$I_C = \alpha_{DC} I_E = (0.996)(5 \text{ mA}) = 4.98 \text{ mA}$$

Equation 5-1 provides us with I_B .

$$I_B = I_E - I_C = 5 \text{ mA} - 4.98 \text{ mA} = 0.02 \text{ mA} = 20 \mu\text{A}$$

5-5 Leakage Currents

Since the collector-base p - n junction is reverse-biased, it is subject to the same reverse leakage currents that plague all reverse-biased diodes. In Fig. 5-11(a) we see the effect of the reverse leakage current. ***When the emitter circuit of a transistor is opened, the collector current should be zero, ideally.*** However, because of thermally produced minority carriers, a small leakage current will flow. The leakage current component is called I_{CBO} . Triple subscript notation is employed extensively in the electronics industry. I_{CBO} is defined in Fig. 5-11(a).

BJT Current Components

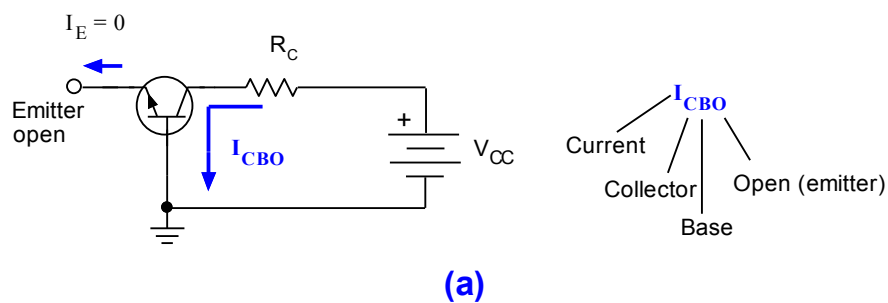
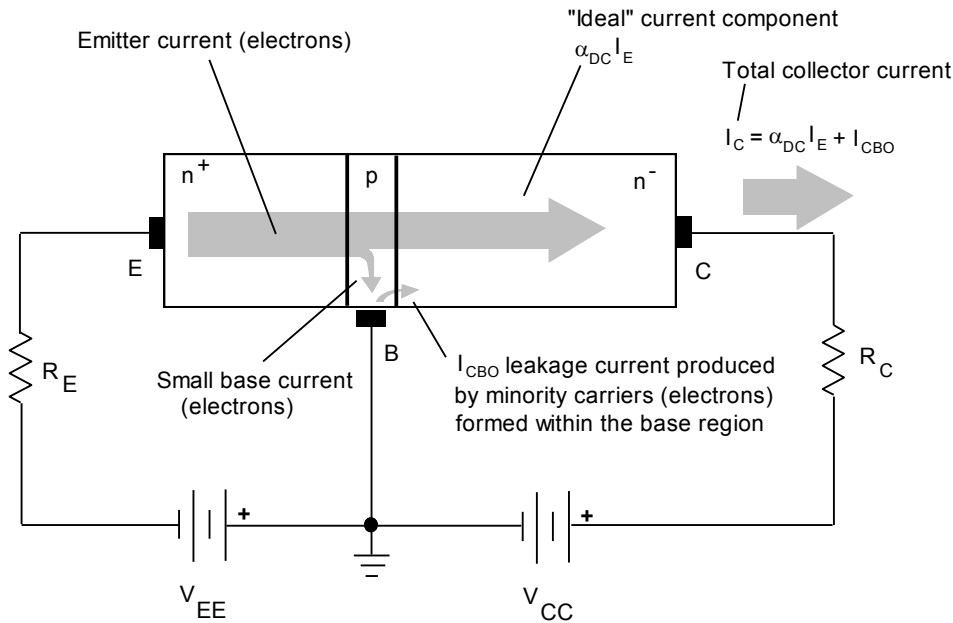


Figure 5-11.

BJT Current Components (continued)



(b)

Figure 5-11 (continued).

The current components found in an *npn* BJT have been illustrated in Fig. 5-11(b). The emitter electrons from the n^+ emitter region become minority carriers once they enter the p -type base region. Thermal energy will liberate additional minority-carrier electrons in the base region. Most of the electrons within the base region will be swept across the collector-base depletion region. This means the total collector current will contain an ideal component from the emitter and a leakage current component. Inspection of Fig. 5-11(b) leads us to Eq. 5-9.

$$I_C = \alpha_{DC} I_E + I_{CBO}$$

(5-9)

I_{CBO} is like the reverse saturation current (I_S) through a “regular” p - n junction. This means it has values on the order of a few nanoamperes (nA). If I_{CBO} is nearly zero, we arrive at the idealization suggested by Eq. 5-6 ($I_C = \alpha_{DC} I_E$). We use this as an approximate relationship extensively. Equation 5-9 is helpful in that it shows how temperature affects I_C . Specifically, as we raise the temperature, more minority carriers are produced. This means I_{CBO} will increase. Since I_{CBO} is a component of I_C , this means I_C will increase. Thus, **I_C increases as the temperature is raised.**

Understanding I_{CBO} is straightforward and this leakage current lends itself to the common-base configuration. However, the common-emitter configuration is a much more popular connection. Consequently, a leakage current term denoted I_{CEO} , which is based on the common-emitter configuration, is more useful. I_{CEO} is defined in Fig. 5-12(a). The collector current and its relationships to I_{CEO} and I_{CBO} , are described in Fig. 5-12(b).

Common Emitter Leakage

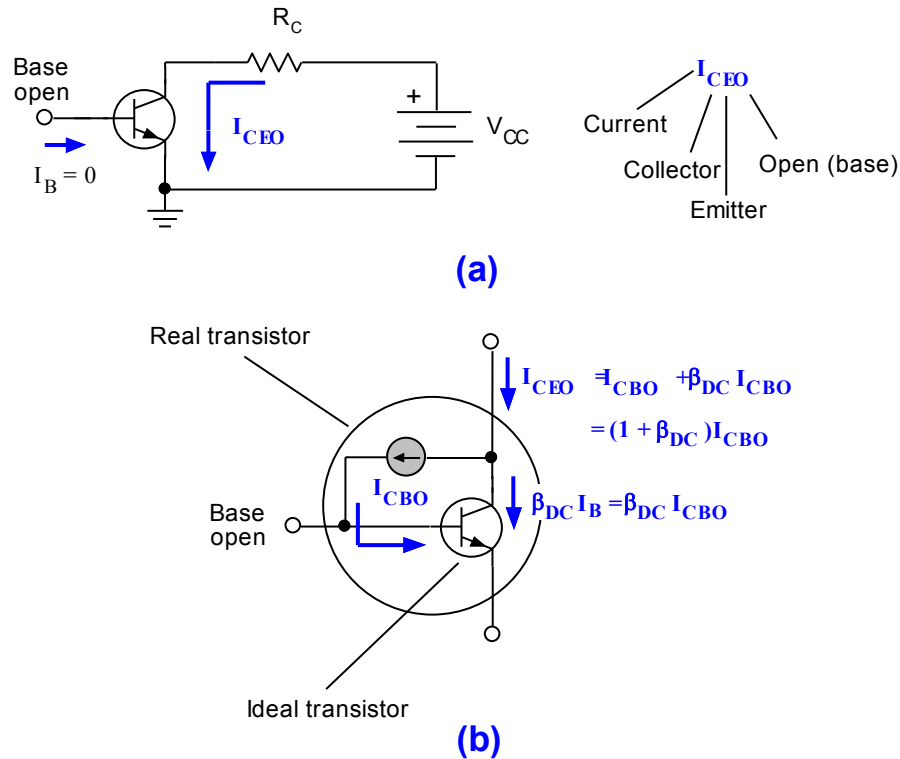


Figure 5-12.

If the base terminal is open, the base current is zero. Ideally, the collector current should also be zero. (From Eq. 5-5, we have $I_C = \beta_{DC} I_B$.) However, a small collector (leakage) current will be present as depicted in Fig. 5-12(a). ***This leakage current is called I_{CEO} and it tends to be much larger than I_{CBO} .*** The reason this is true is explained in Fig. 5-12(b).

A real transistor is being modeled as an ideal (no leakage) transistor with a ***constant-current source*** connected between its collector and base. The constant current source is used to represent the collector-base leakage current I_{CBO} . (This equivalent circuit concept is developed in Section 2-5.)

Although the transistor's base terminal is open, I_{CBO} is still injected into its base internally. Since the ideal transistor produces a collector current that is equal to its β_{DC} times its base current, its collector current becomes $\beta_{DC} I_{CBO}$. Kirchhoff's current law and a little algebra yields Eq. 5-10.

$$I_{CEO} = (1 + \beta_{DC}) I_{CBO} \quad (5-10)$$

Since β_{DC} can become rather large, Eq. 5-10 reveals that ***I_{CEO} is always much larger than I_{CBO} .*** The leakage current term I_{CEO} can be added to the ideal collector current component $\beta_{DC} I_B$ as provided by Eq. 5-11.

$$I_C = \beta_{DC} I_B + I_{CEO} \quad (5-11)$$

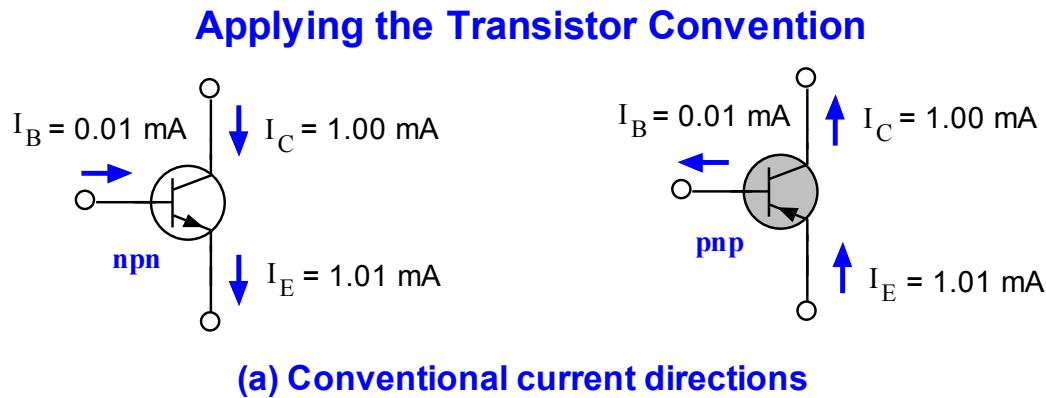
Leakage currents, such as I_{CBO} and I_{CEO} , are undesirable. These leakage currents tend to cause the collector current I_C to increase as the BJT's temperature is raised. Leakage currents can promote a phenomenon known as **thermal runaway**. Let us see how thermal runaway occurs.

A transistor will heat up when it dissipates power. When a transistor heats up, its leakage current increases. The increased leakage causes the collector current to increase. Since $P_C = V_{CE} I_C$, the BJT's power dissipation will increase further. The attendant temperature rise causes an additional increase in the collector current. If unchecked, the process can continue until the transistor destroys itself. Avoiding thermal runaway is an important design consideration.

5-6 The Transistor Convention

During the development of BJT V - I curves, and on manufacturers' data sheets, it is customary to apply the **transistor convention**. The transistor convention is illustrated in Fig. 5-13. Its application is straightforward. **Currents that flow into a BJT are called positive and currents that flow out are called negative.**

The transistor convention is applied to all solid-state devices with three or more terminals. This includes both analog and digital integrated circuits. It is employed extensively on V - I curves and manufacturer's data sheets.



NPN Transistor Convention Values			PNP Transistor Convention Values		
Quantity	Value	Units	Quantity	Value	Units
I_C	1.00	mA	I_C	-1.00	mA
I_B	0.01	mA	I_B	- 0.01	mA
I_E	-1.01	mA	I_E	1.01	mA

(b) Application of the transistor convention

Figure 5-13.

5-7 V-I Curves

Just as V - I curves are often used to illustrate diode behavior, they are also employed to describe BJTs. However, because BJTs are three-terminal devices, a *set* of V - I curves can be generated. The three types most frequently generated (in order of popularity) are **output curves**, **input curves**, and **transfer characteristic curves**.

The V-I Curves for a Common-Base BJT

Remember (from Table 5-1) the emitter terminal serves as the input terminal for a common-base transistor while its collector is the designated output terminal. The input curves for a common-base BJT are provided in Fig. 5-14. Since we have a forward-biased p - n junction between the emitter and base terminals, the V - I input curves remind us of a forward-biased diode. The curves are obtained by adjusting the emitter current (I_E) to various values and measuring the corresponding emitter-base voltage (V_{EB}) drop. Each separate curve is developed while holding the collector-base voltage (V_{CB}) constant. V_{CB} is called the *parameter*. **A variable, which is held constant temporarily, is called a parameter.** The transistor convention has been applied which means the emitter current values are called negative. For an n pn BJT, the emitter-base forward bias requires that the emitter be negative with respect to the base. Consequently, the V_{EB} values are negative. The collector-base p - n junction is reverse biased. This means the collector of the n pn BJT must be positive with respect to the base and the V_{CB} values must be positive.

Common Base Input Curves

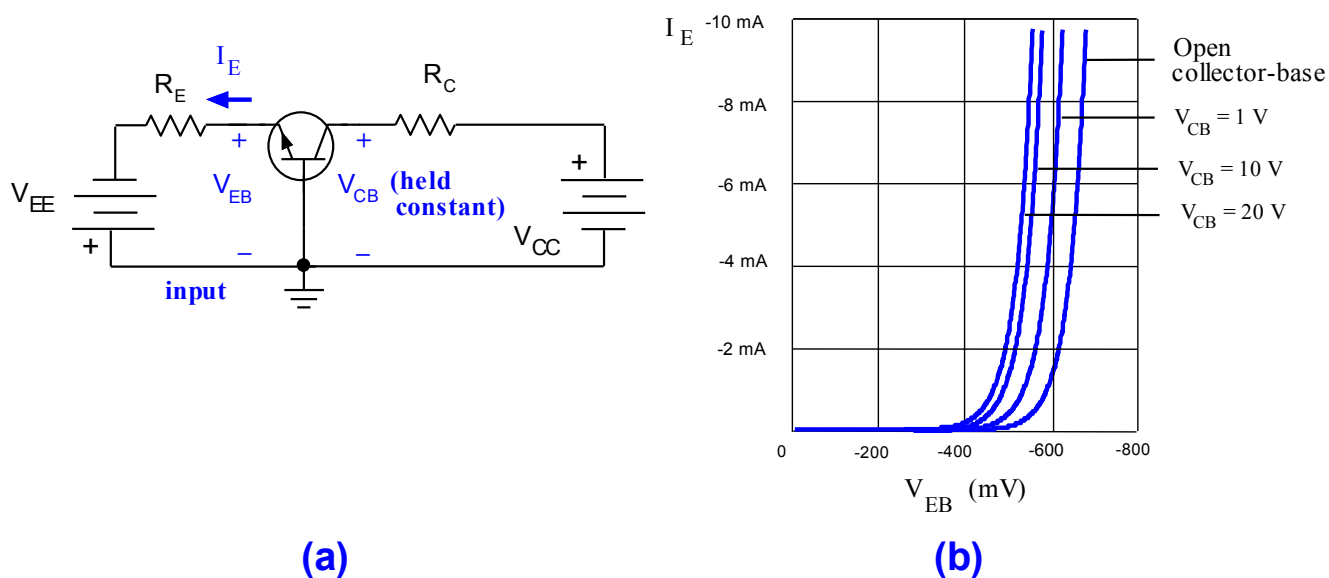


Figure 5-14.

The common-base output curves for an *nnp* BJT are generated using the circuit given in Fig. 5-15(a). The output current is I_C . Since the base is taken to ground, the output voltage is V_{CB} . The emitter current I_E controls the collector current. Consequently, I_E is taken as the parameter. It is held constant while each output curve is being generated. The result is the family of output curves shown in Fig. 5-15(b). The emitter current values are labeled negative in observance of the transistor convention. Note that the emitter and collector currents are almost equal to one another. A sample DC operating point (Q) has also been indicated in Fig. 5-15(b).

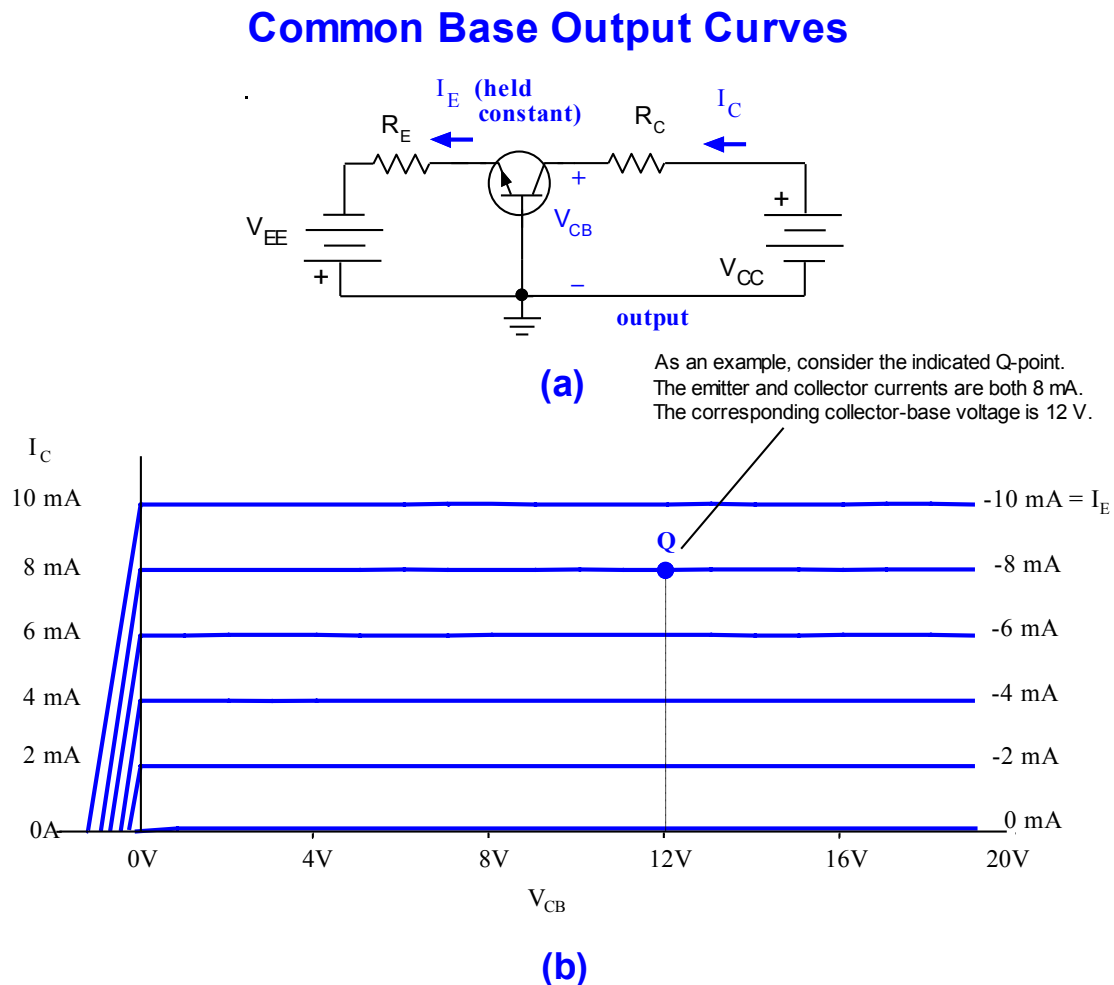


Figure 5-15.

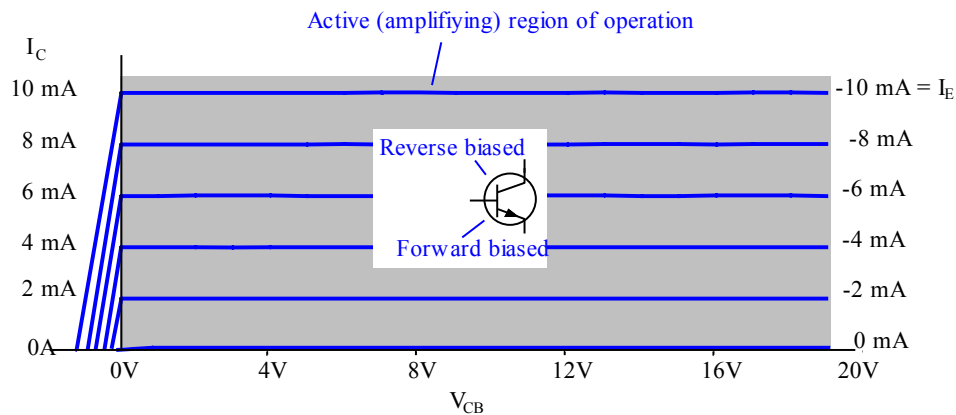
A BJT has three regions of possible operation. These are called the **active**, **saturation**, and **cutoff** regions. When a BJT is to be used as an amplifier, it must be operated in the active region. A transistor acts like a closed switch when in its saturation region. A transistor behaves like an open switch when in its cutoff region. The particular region of operation depends on the biasing of the BJT's *p-n* junctions. The relationships are defined in Table 5-2. They have been depicted graphically in Fig. 5-16.

Table 5-2. BJT Regions of Operation and Biasing

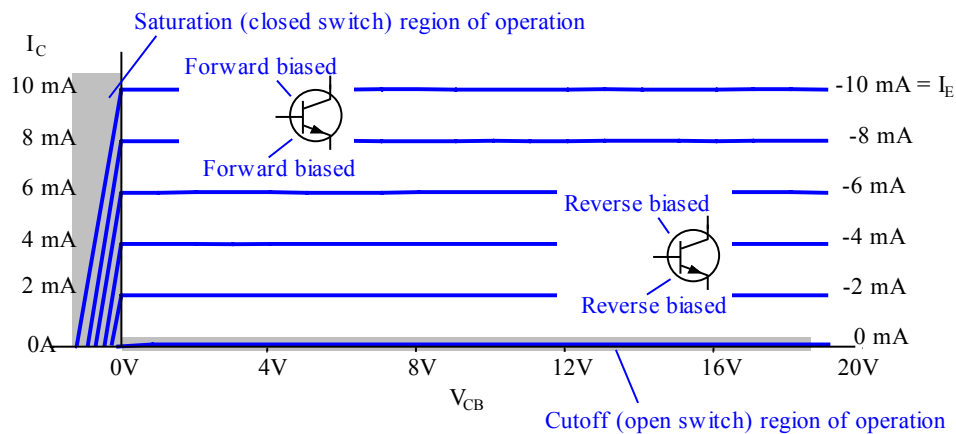
Region of Operation	Emitter-Base Bias	Collector-Base Bias
Active	Forward	Reverse
Cutoff	Reverse	Reverse
Saturation	Forward	Forward

We shall make a closer examination of the three regions of operation as our work progresses. The operation of the BJT as an amplifier is introduced in Section 5-9. The use of the BJT as a switch is described in Section 5-10. An example of a switching application is provided in Section 5-11. A simple toy robot called the *Clapper* uses four separate transistor switches.

BJT Regions of Operation



(a)



(b)

Figure 5-16.

When a BJT is to be used as a linear amplifier, we expect its output signal to be a scaled-up version of its input signal. A BJT that enters saturation and/or cutoff will produce a form of amplitude distortion called **clipping**. In digital (on-off) applications, the transistor is operated in either saturation (as a closed switch) or cutoff (as an open switch). The BJT makes a very quick transition through its active region. In switching applications, operation within the active region is undesirable⁴³.

The V - I Curves for a Common-Emitter BJT

If we peek at Table 5-1, we are reminded the base terminal serves as the input terminal for the common emitter BJT. The collector is the designated output terminal. The input curves for the common-emitter BJT are provided in Fig. 5-17. Again, because the base-emitter p - n junction is forward biased, the V - I curves are like those produced by a diode. The collector-emitter voltage (V_{CE}) is taken as the parameter.

Application of the transistor convention requires the base current be regarded as a positive quantity. To forward bias the base-emitter p - n junction, the base supply V_{BB} is used. Therefore, positive values of V_{BE} occur.

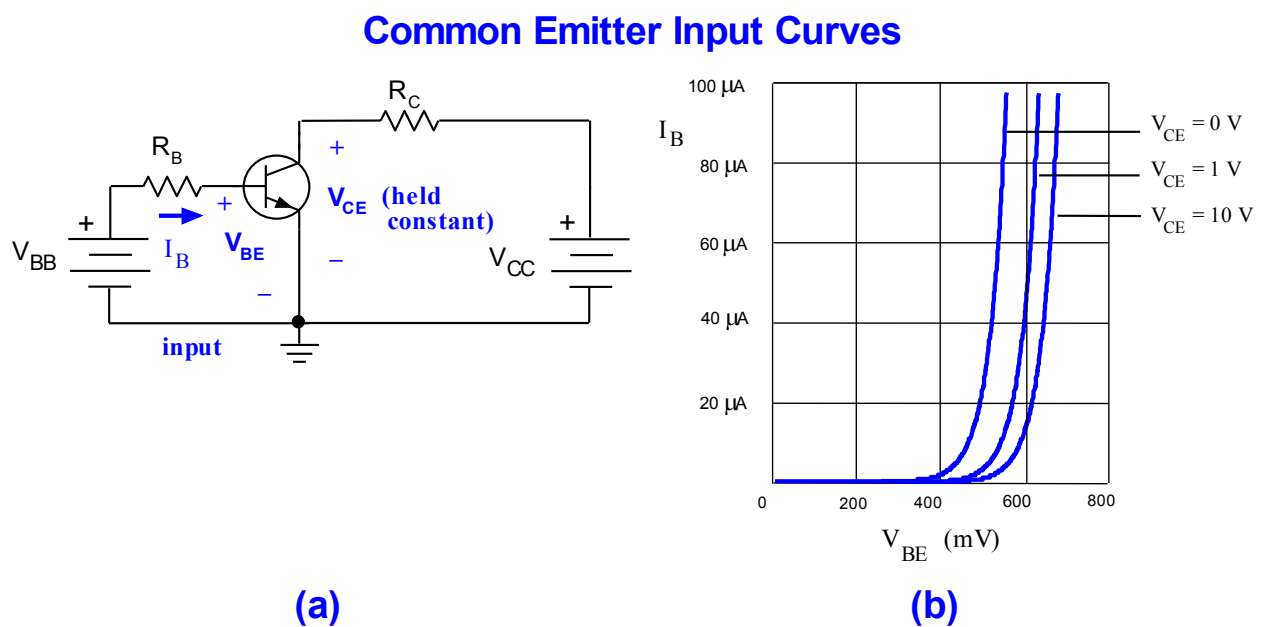


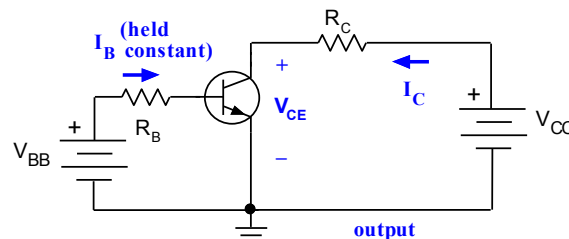
Figure 5-17.

⁴³ In the early years, the linear viewpoint was to joke that digital designers are perverse in their exclusive operation in regions of distortion. To counter, the digital designers would joke that analog (linear) designers lack the strength of character to commit to solid operation. The present-day approach is to use digital techniques whenever possible.

The common-emitter output curves are shown in Fig. 5-18. The base current is taken as the controlling input parameter. The (output) collector current is on the vertical axis, while the (output) collector-emitter voltage is placed on the horizontal axis. A typical DC bias point (Q) has been indicated in Fig. 5-18. A 20- μA base current produces a collector current of about 1 mA. The corresponding collector-to-emitter voltage is 8 V.

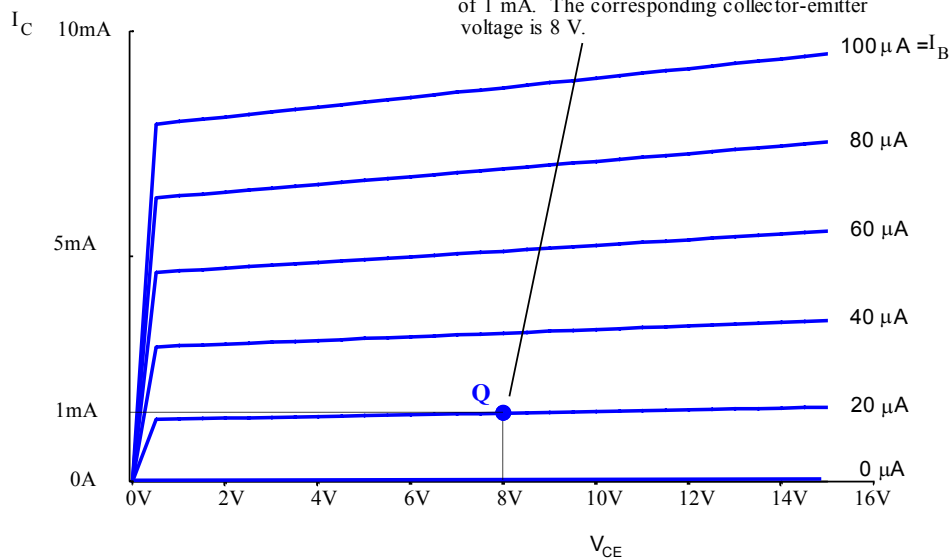
The collector supply V_{CC} provides the collector bias. The collector current is treated as a positive quantity because of the transistor convention. The voltage at the collector will be positive with respect to the emitter terminal. Accordingly, V_{CE} will assume positive values. Base current is the parameter. Again, it is a positive quantity because it flows into the BJT.

Common Emitter Output Curves



(a)

A sample Q point indicates a base current of 20 microamps produces a collector current of 1 mA. The corresponding collector-emitter voltage is 8 V.

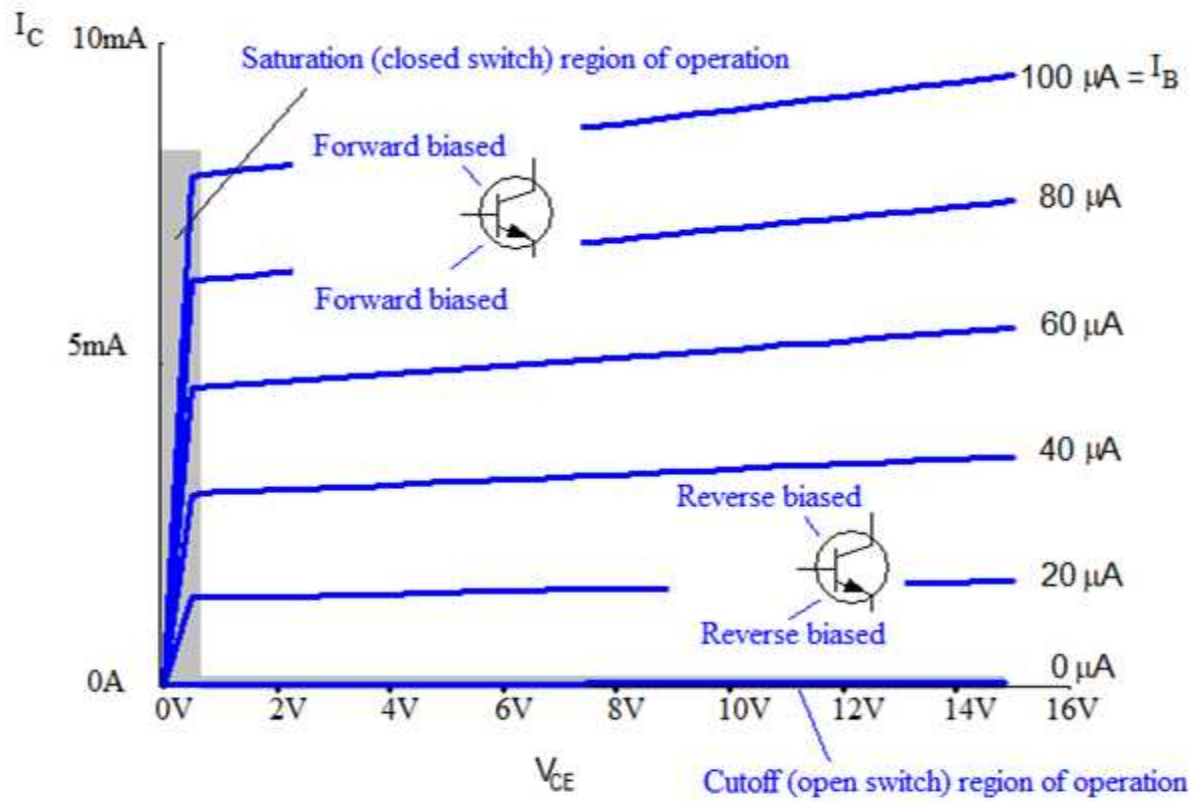


(b)

Figure 5-18.

The BJT's three regions of possible operation (saturation, active, and cutoff) have been indicated in Fig. 5-19(a) and (b).

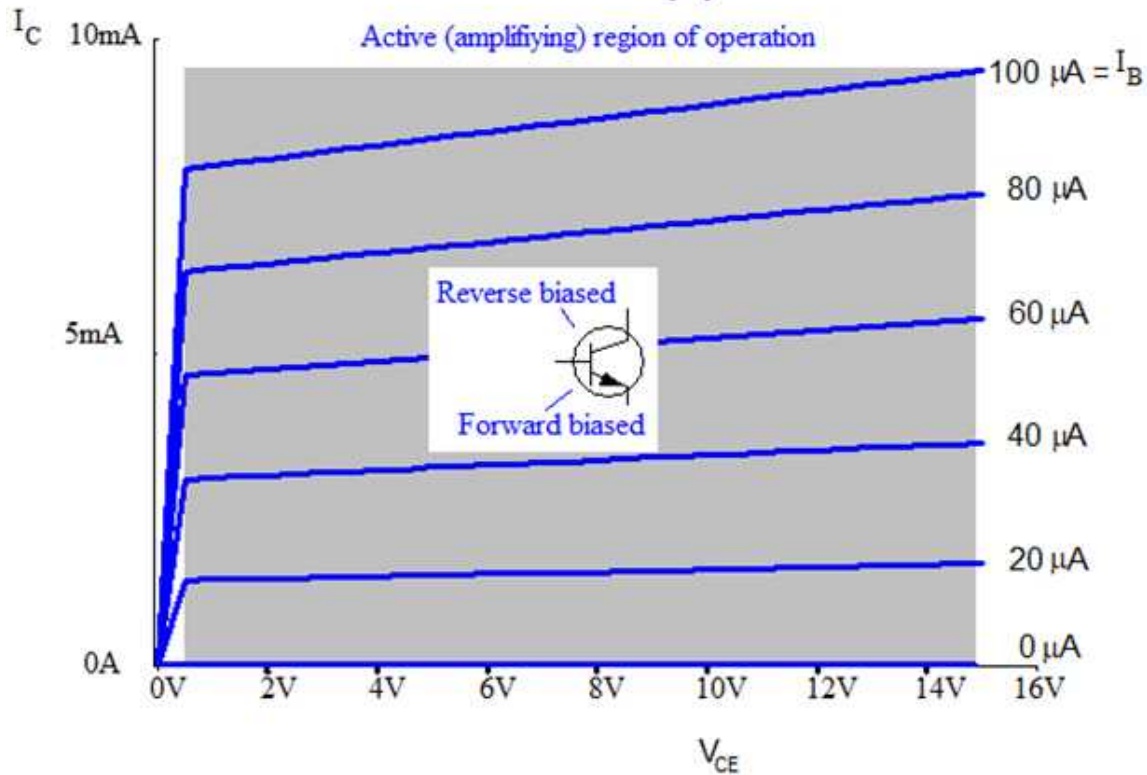
Common Emitter Regions of Operation



(a)

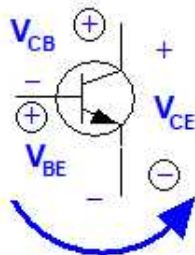
Figure 5-19.

Common Emitter Regions of Operation (continued)



(b)

$$-V_{CE} + V_{CB} + V_{BE} = 0$$



Apply KVL around the BJT and solve for the collector-base voltage.

(c)

Figure 5-19 (continued).

While most beginning students can determine the BJT's emitter-base voltage, the collector-base bias is not so obvious when the BJT is in its common-emitter configuration. The solution to this problem is to recognize that ***Kirchhoff's voltage law applies around the transistor***. In Fig. 5-19(c) we pick the emitter as the starting point and sum the voltages around the transistor. The signs given to each of the three voltages depend on the polarity mark we encounter first as we move around the transistor. In Fig. 5-19(c), we move in a counterclockwise direction. The sum equals zero. We then solve for V_{CB} .

$$-V_{CE} + V_{CB} + V_{BE} = 0$$

$$V_{CB} = V_{CE} - V_{BE} \quad (5-12)$$

Since we have an *npn* BJT, the collector-base *p-n* junction will be reverse biased provided the collector is more positive than the base terminal. This occurs for positive values of V_{CB} .

Example 5-4. An *npn* transistor has a V_{CE} of 2 V and a V_{BE} of 0.7 V. Find its V_{CB} and determine if the transistor is in its active, cutoff, or saturation region of operation.

Solution: First, we apply Eq. 5-12.

$$V_{CB} = V_{CE} - V_{BE} = 2 \text{ V} - 0.7 \text{ V} = 1.3 \text{ V}$$

The positive value of V_{BE} means the base-emitter *p-n* junction is forward biased. The positive V_{CB} value means the collector-base *p-n* junction is reverse biased. Therefore, the BJT is in its active region of operation.

Example 5-5. An *npn* transistor has a V_{CE} of 0.5 V and a V_{BE} of 0.7 V. Find its V_{CB} and determine if the transistor is in its active, cutoff, or saturation region of operation.

Solution: We apply Eq. 5-12.

$$V_{CB} = V_{CE} - V_{BE} = 0.5 \text{ V} - 0.7 \text{ V} = -0.2 \text{ V}$$

The positive value of V_{BE} means the base-emitter *p-n* junction is forward biased. The negative V_{CB} value means the collector-base *p-n* junction is also forward biased. Therefore, the BJT is *saturated*.

Example 5-6. An *npn* transistor has a V_{CE} of 15 V and a V_{BE} of -1 V. Find its V_{CB} and determine if the transistor is in its active, cutoff, or saturation region of operation.

Solution: We apply Eq. 5-12.

$$V_{CB} = V_{CE} - V_{BE} = 15 \text{ V} - (-1 \text{ V}) = 16 \text{ V}$$

The negative value of V_{BE} means the base-emitter p - n junction is reverse biased. The positive V_{CB} value means the collector-base p - n junction is also reverse biased. Therefore, the BJT is in *cutoff*.

Whenever V_{CE} becomes less than the forward-bias voltage found across a p - n junction, the BJT is entering saturation. This is an important fact to remember and can help us in the analysis, design, and troubleshooting of BJT circuits.

Using Multisim to Generate BJT V - I Curves

Multisim can be used to generate BJT V - I curves using a nested DC sweep. We are conducting this exercise to observe the Multisim BJT models are non-linear and the steps needed to perform a nested DC sweep. We do *not* need to generate V - I curves normally. We add the BJT as explained in Fig. 5-20. We shall run the common-emitter output curves for a 2N3904 *npn* BJT. It is in the Transistor library in the NPN_BJT family. After we place the BJT on the schematic page, we add a DC current source, a DC voltage source, and ground as also illustrated in Fig. 5-20.

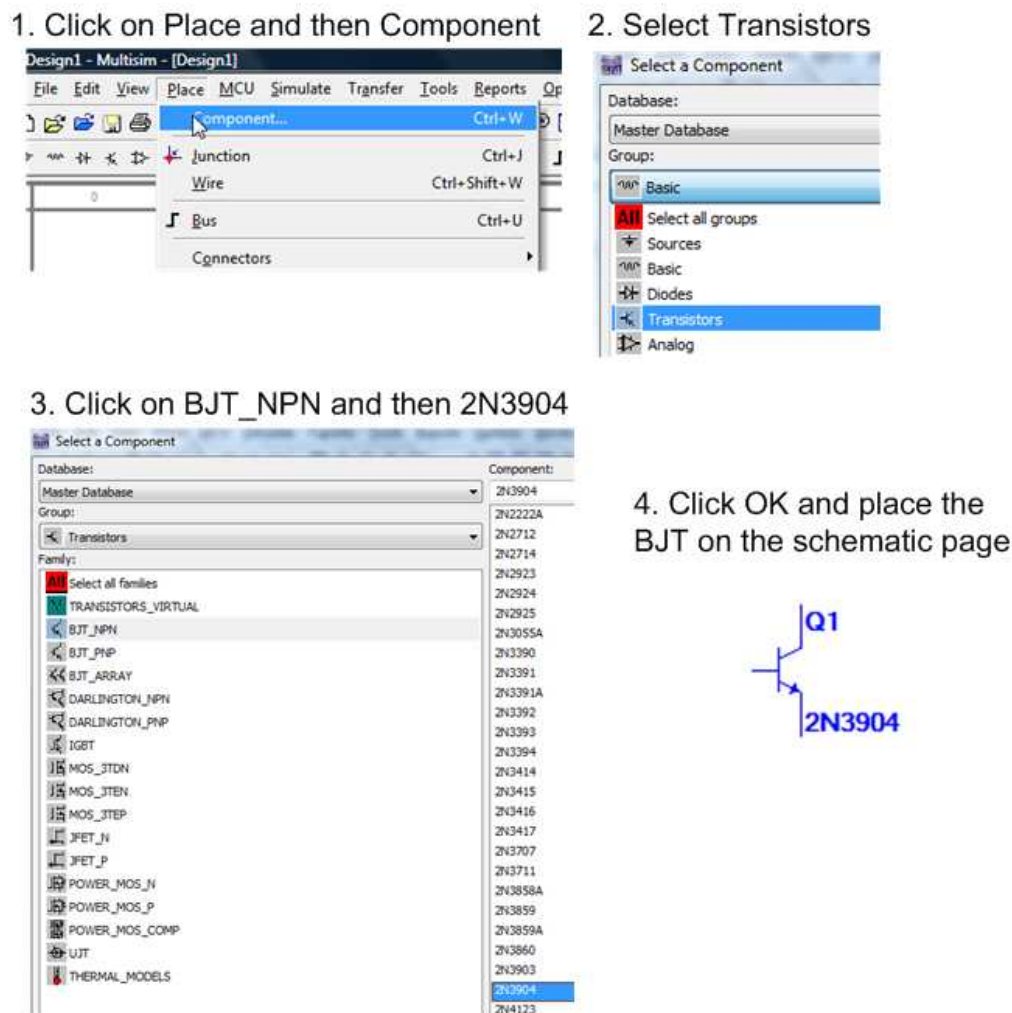
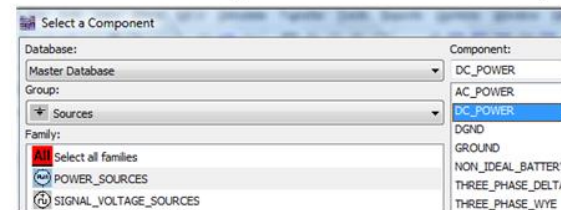


Figure 5-20.

5. Place a ground on the schematic page



6. Place a DC voltage source on the schematic page



7. Place a DC current source on the schematic page

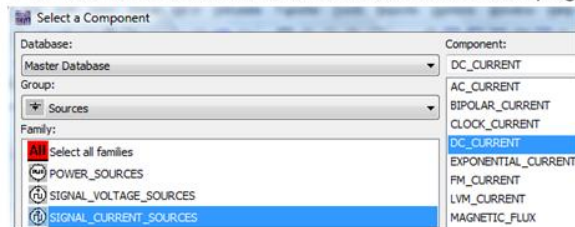
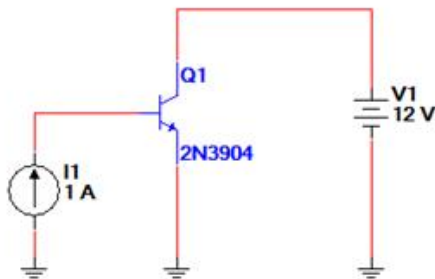


Figure 5-20 (continued).

We wire the circuit and select the simulation analysis to be a DC sweep as shown in Fig. 5-21.

8. Wire the circuit neatly



9. Select - Simulate- Analysis - DC Sweep

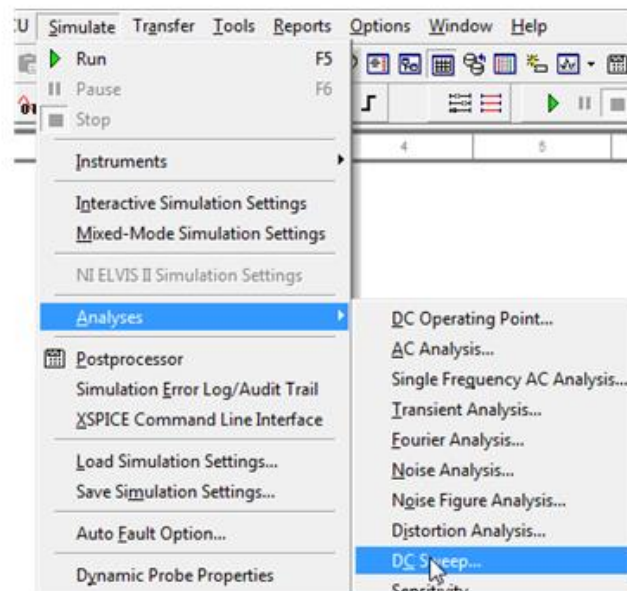


Figure 5-21.

The DC sweep is set up as indicated in Fig. 5-22. The primary sweep is the collector-to-emitter voltage that starts from zero and goes to 10 V in steps of 0.1 V. The secondary sweep is the base current. The base current starts at zero and goes to 10 μA in steps of 2 μA . The vertical axis is set up to be the collector current under the Output tab.

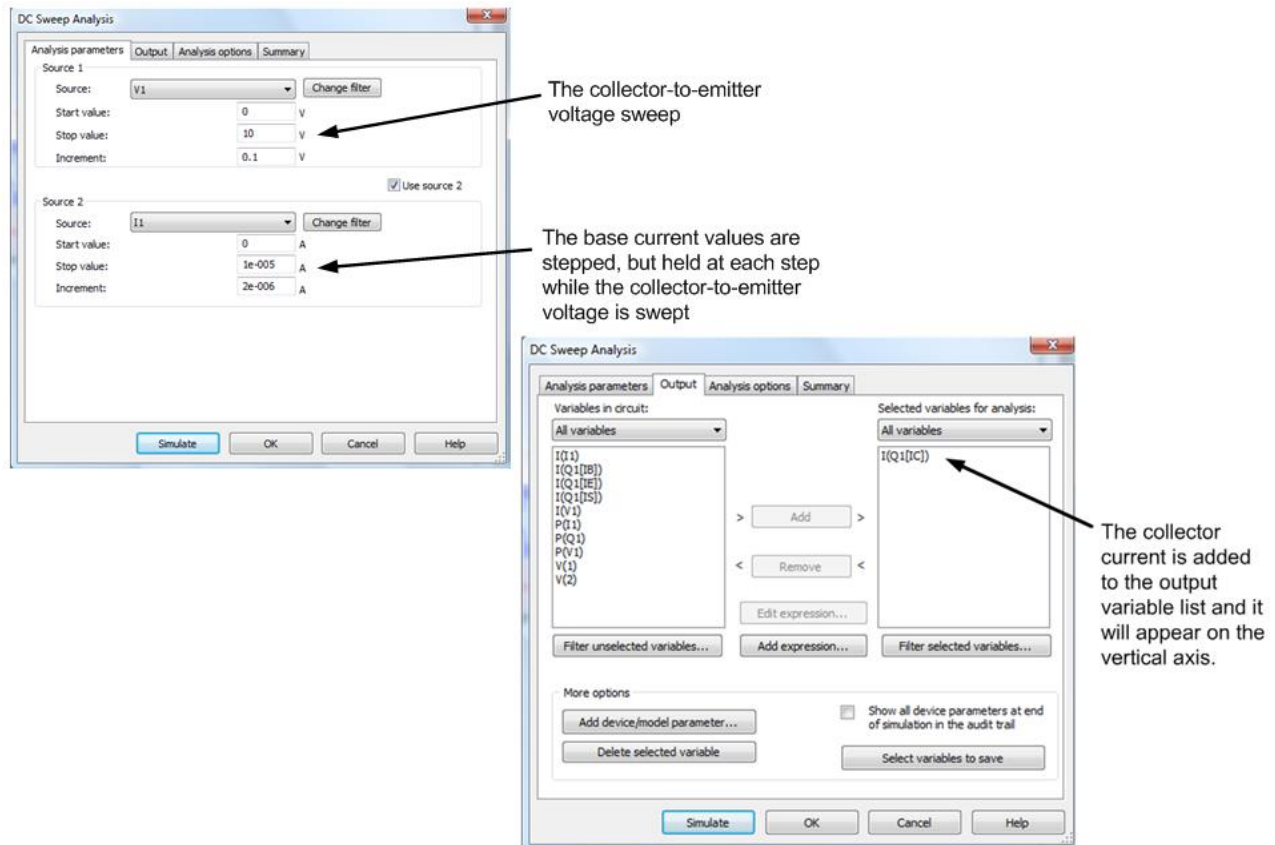


Figure 5-22.

We simulate the common-emitter output characteristics by clicking on the Simulate (Fig. 5-22) button in the DC Sweep Analysis window. The resulting curves will appear as shown in Fig. 5-23. However, we select a black-and-white plot with a white background to save ink or toner supplies.

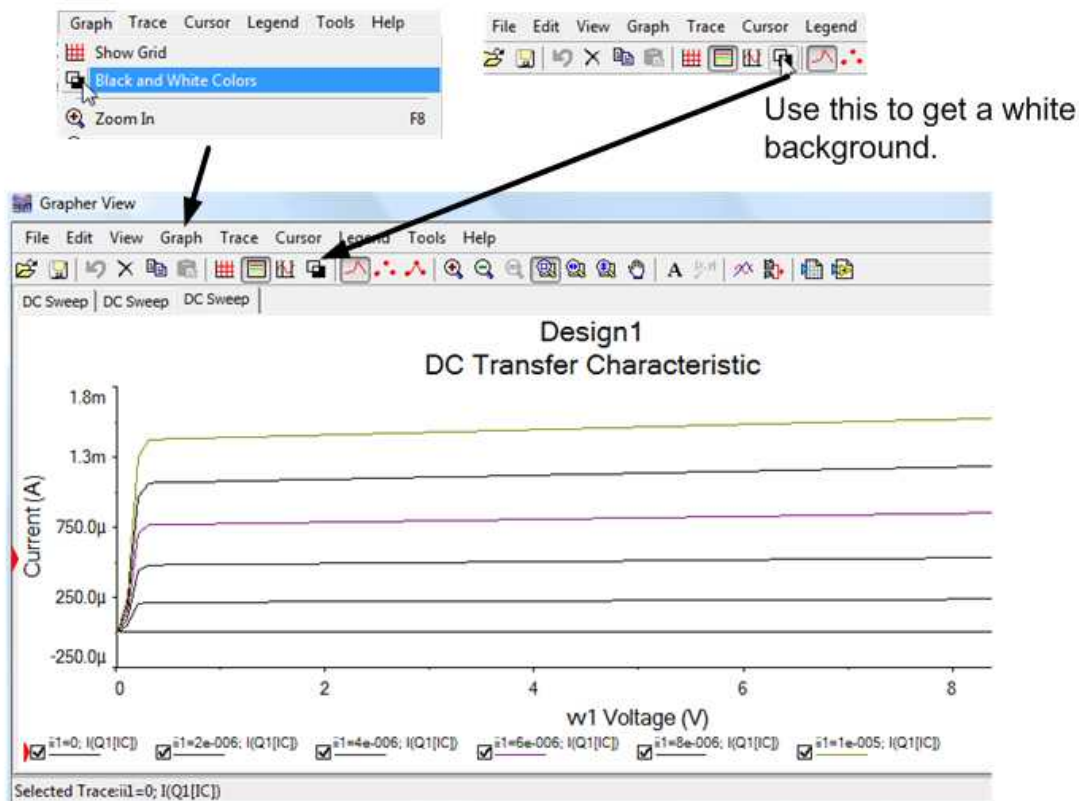


Figure 5-23.

5-8 Finding the Q Point

Transistors are used to provide amplification and to work as switches. For a transistor to work properly, it must have the correct DC bias. ***The DC operating point is critical to the operation of the BJT.*** We investigate bias circuits in detail in Chapter 7 of Volume 2. Our goal here is to deliver an introduction to the DC analysis of the BJT.

In the dawn of the transistor era (e.g., the 1960's and early 1970's), the *DC load line* approach was a popular method for finding a transistor's DC operating point, or Q point. Like the diode's DC load line, we introduce it, but we will *not* use it largely. We will instead favor analytical methods and approximations. However, we should note that the *AC load line* is still a useful tool in predicting a transistor's large-signal AC response in power amplifier problems. (We will deal with this much later in our work.)

In Fig. 5-24(a), we have a common base BJT circuit. The emitter-base *p-n* junction is forward-biased by the emitter supply V_{EE} . Note that the $-V_{EE}$ notation means the negative terminal of the emitter supply is tied to that point. The positive terminal of V_{EE} is tied to ground. The circuit has been redrawn in Fig. 5-24(b). Our next task is to find the controlling emitter current I_E . This can be accomplished by applying Kirchhoff's voltage law and solving for I_E . (Assuming the BJT is a silicon device, the forward voltage drop across the emitter-base *p-n* junction is approximately 0.7 V.)

We work our way around the emitter circuit in the direction of the emitter current.

$$0.7 \text{ V} + I_E R_E - V_{EE} = 0$$

Next, we transpose the voltage terms to the right-hand side.

$$I_E R_E = V_{EE} - 0.7 \text{ V}$$

The last step is to divide both sides of the equation by R_E .

$$I_E = \frac{V_{EE} - 0.7 \text{ V}}{R_E} \quad (5-13)$$

Equation 5-13 is important. We will use it to find the emitter current (I_E) regardless of the analysis approach to finding the collector current (I_C) and the collector-base voltage V_{CB} .

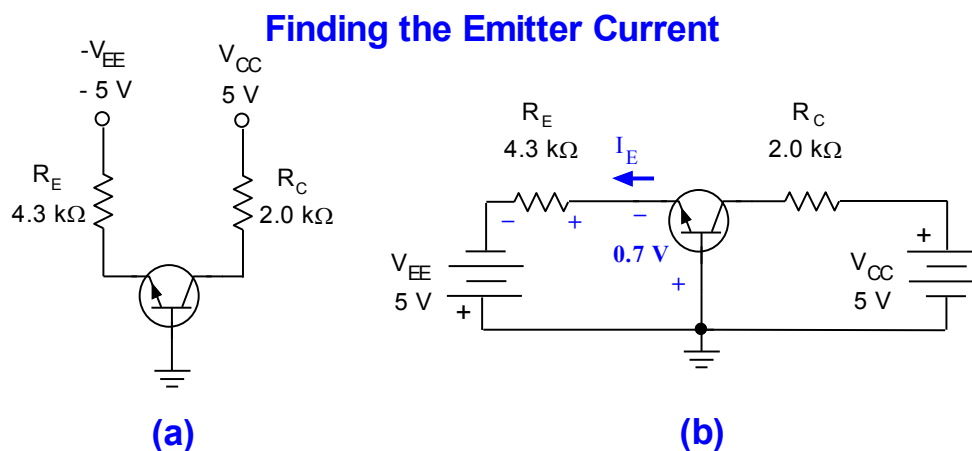


Figure 5-24.

Example 5-7. Find the emitter current I_E flowing in the common-base BJT circuit shown in Fig. 5-24.

Solution: We apply Eq. 5-13.

$$I_E = \frac{V_{EE} - 0.7 \text{ V}}{R_E} = \frac{5 \text{ V} - 0.7 \text{ V}}{4.3 \text{ k}\Omega} = 1 \text{ mA}$$

Now that we have determined the controlling (input) current, we begin our analysis of the controlled (output) side. Specifically, we must find the collector current I_C and the collector-base voltage V_{CB} . We shall illustrate the required analysis using the graphical (DC load line) approach and then employing analytical methods.

The DC load line approach is summarized in Fig. 5-25. The procedure is very similar to that developed for the diode (Fig. 2-20). The open-circuit voltage V_{OC} is called the **collector-base cutoff voltage** $V_{CB(OFF)}$ since it lies in the BJT's cutoff region of operation. The short-circuit current I_{SH} is called the **collector saturation current** $I_{C(SAT)}$ since it is located at the edge of the BJT's saturation region of operation. The specific output V - I characteristic curve of interest depends on the emitter current.

Common-Base DC Load Line Analysis

1.) Obtain BJT's V - I Output Curve.

(The common base output curve is used since the BJT is in its common-base connection.)

2.) Find the open-circuit voltage.

[The voltage that would appear across the BJT's collector-base if it were an open-circuit is determined as shown in (c).]

$$V_{OC} = V_{CB(OFF)} = V_{CC}$$

3.) Find the short-circuit current.

[The current that would flow through the BJT's collector-base if it were a short circuit is determined as shown in (d)].

$$I_{SH} = I_{C(SAT)} = \frac{V_{CC}}{R_C}$$

4.) Locate $V_{CB(OFF)}$ and $I_{C(SAT)}$ on the V - I characteristic.

Connect the points with a straight line called the **DC Load Line**.

5.) Determine the emitter current.

Use the V - I curve in the family of V - I curves that matches the emitter current value.

6.) The intersection between the load line and the particular V - I curve of interest gives the dc operating point (called the Q point).

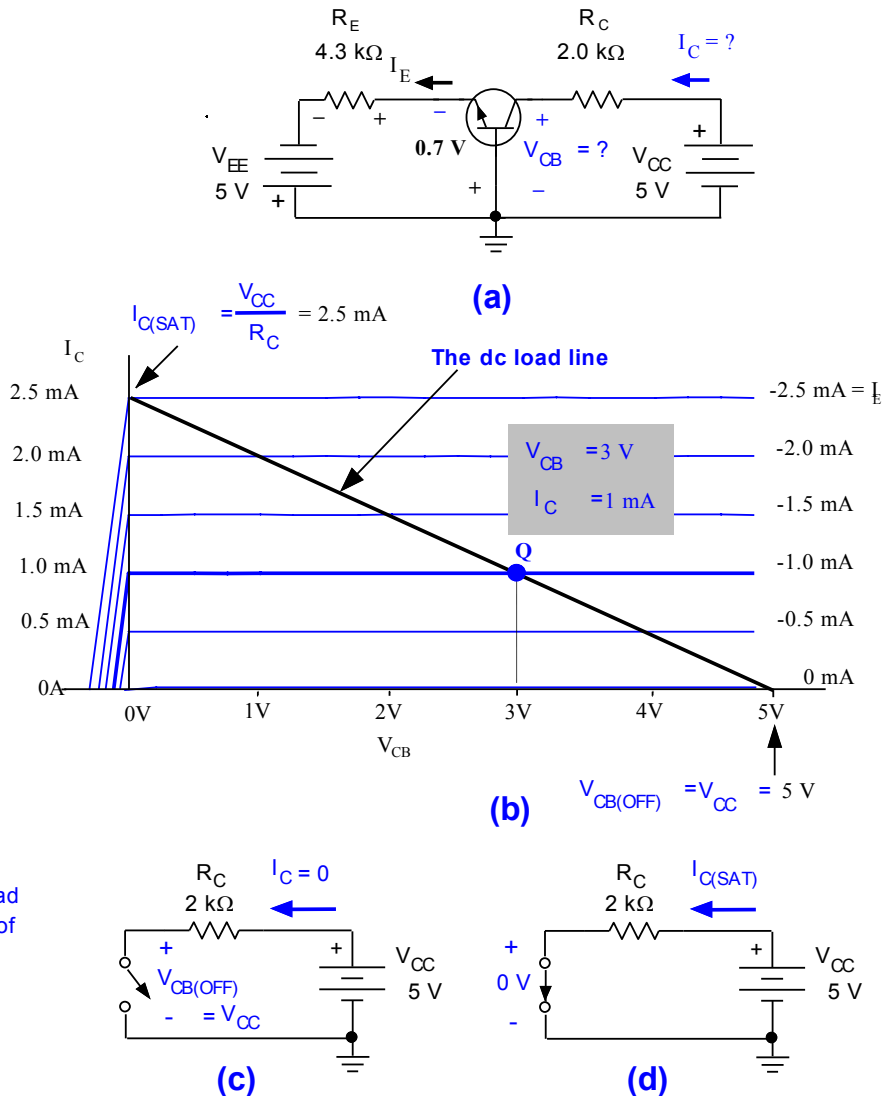


Figure 5-25.

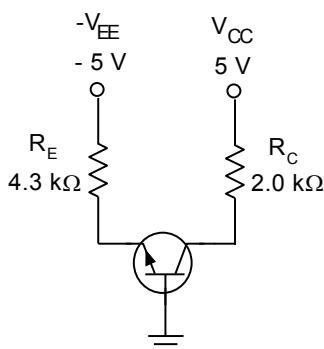
The intersection between the DC load line and that V - I curve yields the DC operating point (called the **Q -point**). By moving over to the collector current axis and down to the collector-base voltage axis, we can find the values for I_C and V_{CB} , respectively.

The DC load line approach is straightforward, and it can help us visualize BJT operation in a circuit. (For instance, if the emitter current is increased to 1.5 mA, the Q-point moves up, and this results in an increase in I_C to 1.5 mA, and a decrease in V_{CB} to 2 V.) However, it suffers from two disadvantages. First, we must obtain the BJT's V - I characteristic. This is often inconvenient. Second, since it is a graphical technique, we must be neat and read the scales carefully. This can be time consuming. An analytical approach is more efficient.

An analytical approach can be broken down to three fundamental steps. First, we analyze the input to find the emitter current I_E . Second, we transfer from the input circuit to the output circuit using the BJT's α_{DC} to find its collector current I_C . Third, we analyze the output. This is accomplished by using Kirchhoff's voltage law to determine the collector-to-base voltage V_{CB} . The analytical approach for a common-base transistor is summarized in Fig. 5-26.

The Analytical Approach to a Common-Base BJT Analysis

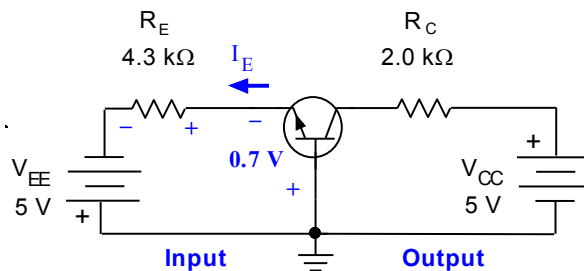
Given Circuit



(a)

Step 1: Analyze the Input

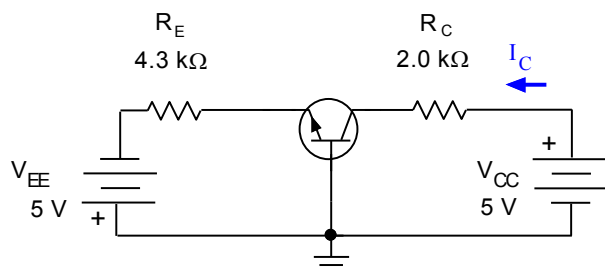
$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{5\text{ V} - 0.7\text{ V}}{4.3\text{ k}\Omega} = 1\text{ mA}$$



(b)

Step 2: Transfer from the Input to the Output

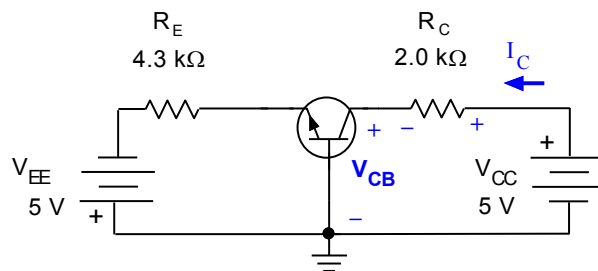
$$I_C = \alpha_{DC} I_E \cong I_E = 1\text{ mA}$$



(c)

Step 3: Analyze the Output

$$V_{CB} = V_{CC} - I_C R_C \cong 3\text{ V}$$



(d)

Figure 5-26.

Equation 5-13 was developed previously to determine the emitter current I_E as indicated in Fig. 5-26 (b). To transfer from the input side to the output, we use the BJT's α_{DC} . Specifically, Eq. 5-6 has been solved for I_C as shown in Fig. 5-26(c). Step 3, depicted in Fig. 5-26(d), requires the use of Kirchhoff's voltage law. The Kirchhoff's voltage law equation is solved for V_{CB} .

Starting from ground in Fig. 5-26(d), and writing in the direction of I_C , we obtain the Kirchhoff's voltage law equation below.

$$-V_{CC} + I_C R_C + V_{CB} = 0$$

Solving for V_{CB} produces Eq. 5-14.

$$V_{CB} = V_{CC} - I_C R_C \quad (5-14)$$

Example 5-7. Find the Q-point of the common-base transistor circuit given in Fig. 5-26(a). The BJT has an α_{DC} of 0.996. Also determine $I_{C(SAT)}$ and $V_{CB(OFF)}$.

Solution: First, we analyze the input to find I_E . [This is indicated in Fig. 5-26(b).]

$$I_E = \frac{V_{EE} - 0.7 \text{ V}}{R_E} = \frac{5 \text{ V} - 0.7 \text{ V}}{4.3 \text{ k}\Omega} = 1 \text{ mA}$$

Next, we determine I_C . [This is shown in Fig. 5-26(c).]

$$I_C = \alpha_{DC} I_E = (0.996)(1 \text{ mA}) = 0.996 \text{ mA} \cong 1 \text{ mA}$$

Because α_{DC} is very close to unity, the collector current is very nearly equal to I_E . Therefore, we shall approximate its value as 1 mA. Figure 5-26(d) shows the application of Eq. 5-14 to find V_{CB} .

$$V_{CB} = V_{CC} - I_C R_C \cong 5 \text{ V} - (1 \text{ mA})(2 \text{ k}\Omega) = 3 \text{ V}$$

The collector saturation current $I_{C(SAT)}$ and the collector-base cutoff voltage $V_{CB(OFF)}$ are defined in Fig. 5-25.

$$I_{C(SAT)} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{2 \text{ k}\Omega} = 2.5 \text{ mA}$$

$$V_{CB(OFF)} = V_{CC} = 5 \text{ V}$$

$I_{C(SAT)}$ is the largest DC collector current the BJT can experience while $V_{CB(OFF)}$ is the largest DC collector-base voltage the BJT will have to withstand. These quantities are useful when determining the ratings a BJT should possess for a given application.

Analyzing a Common-Emitter BJT Amplifier

The analysis of a common-emitter BJT amplifier is similar to the analysis of the common-base BJT amplifier. Again, one analysis option is to employ the DC load line. The DC load line procedure is described in Fig. 5-27. In Fig. 5-27(a) the common-emitter BJT circuit is shown. The *base bias supply* called V_{BB} . The base-emitter p - n junction is forward biased. If the BJT is a silicon unit, the base-emitter voltage drop V_{BE} is assumed 0.7 V. We use Kirchhoff's voltage law to develop an equation for the base current I_B . Starting at ground in Fig. 5-27(a) and writing the direction of the base current, we obtain the Kirchhoff's voltage law equation.

$$-V_{BB} + I_B R_B + 0.7 \text{ V} = 0$$

Solving the equation for I_B produces Eq. 5-15.

Common-Emitter DC Load Line Analysis

1.) Obtain BJT's V-I Output Curve.
[The common emitter output curve is used since the BJT is in its common-emitter connection.]

2.) Find the open-circuit voltage.
[The voltage that would appear across the BJT's collector-emitter if it were an open-circuit is determined as shown in (c)].

$$V_{OC} = V_{CE(OFF)} = V_{CC}$$

3.) Find the short-circuit current.

[The current that would flow through the BJT's collector-emitter if it were a short circuit is determined as shown in (d)].

$$I_{SH} = I_{C(SAT)} = \frac{V_{CC}}{R_C}$$

4.) Locate $V_{CE(OFF)}$ and $I_{C(SAT)}$ on the V-I characteristic. Connect the points with a straight line called the **DC Load Line**.

5.) Determine the base current. Use the V-I curve in the family of V-I curves that matches the base current value.

$$I_B = \frac{V_{BB} - 0.7 \text{ V}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega} = 10 \mu\text{A}$$

6.) The intersection between the load line and the particular V-I curve of interest gives the dc operating point (called the Q point).

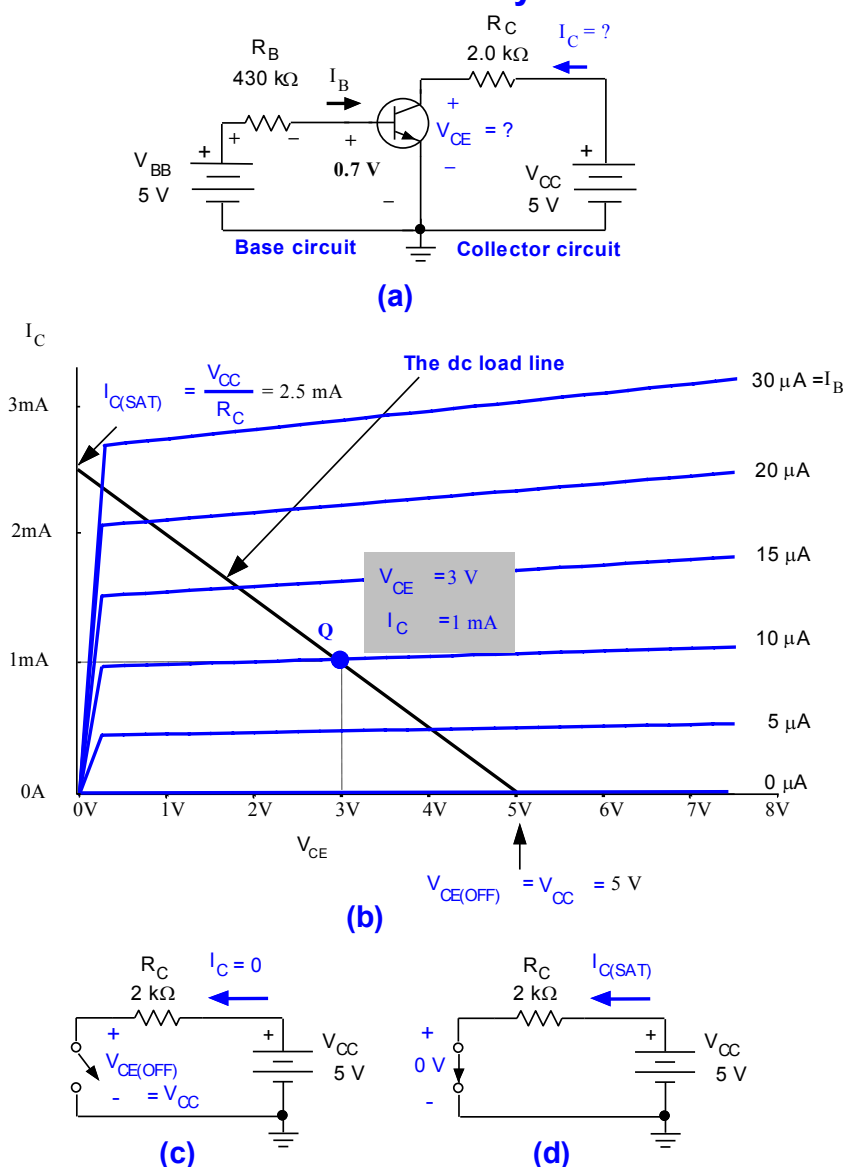


Figure 5-27.

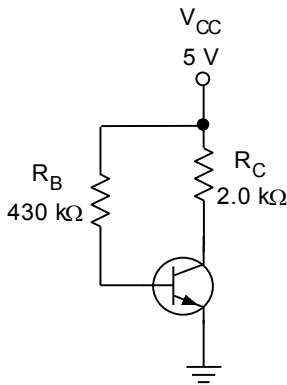
$$I_B = \frac{V_{BB} - 0.7 \text{ V}}{R_B}$$

(5-15)

The *preferred* analysis method for a common-emitter BJT is shown in Fig. 5-28. We invoke the same three-step process. Recall that the base terminal serves as the input to a common-emitter BJT while its collector is its output terminal.

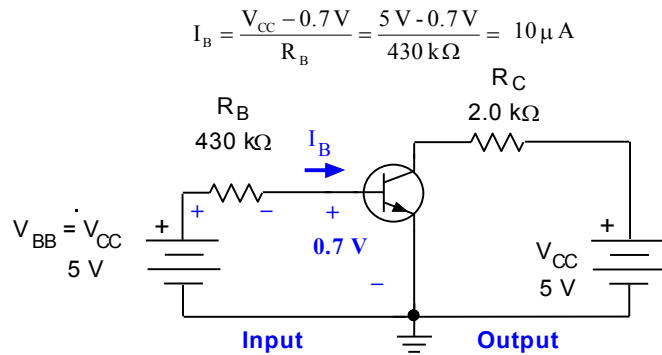
A Common Emitter BJT Analysis

Given Circuit



(a)

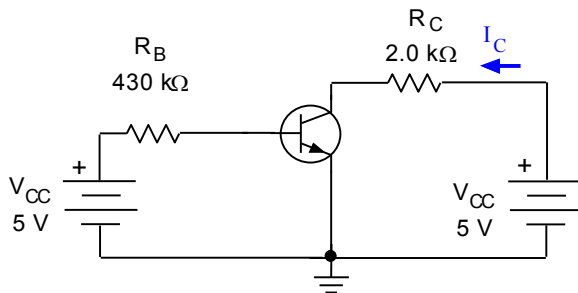
Step 1: Analyze the Input



(b)

Step 2: Transfer from the Input to the Output

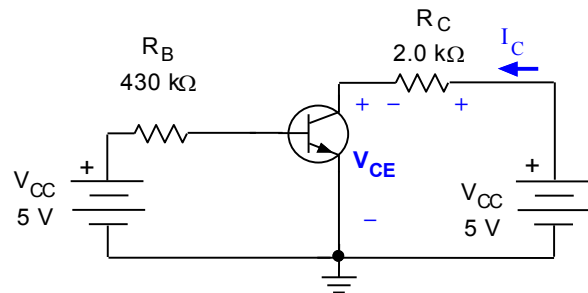
$$I_C = \beta_{DC} I_B = (100)(10 \mu\text{A}) = 1 \text{ mA}$$



(c)

Step 3: Analyze the Output

$$V_{CE} = V_{CC} - I_C R_C = 5 \text{ V} - (1 \text{ mA})(2 \text{ k}\Omega) = 3 \text{ V}$$



(d)

Figure 5-28.

In Fig. 5-28(a) the common-emitter BJT circuit is shown. The circuit may be redrawn as indicated in Fig. 5-28(b). The collector bias supply V_{CC} also serves as the base bias supply V_{BB} . Equation 5-15 is again used to find the base current I_B . The second step in the analysis requires the use of the BJT's common-emitter current gain β_{DC} . This is shown in Fig. 5-28(c). Equation 5-5 is solved for I_C . The third step requires finding the collector-to-emitter voltage V_{CE} . Again, we use Kirchhoff's voltage law to solve for V_{CE} . We start at ground in Fig. 5-28(d) and write in the direction of I_C .

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

Solving for V_{CE} yields Eq. 5-16.

$$V_{CE} = V_{CC} - I_C R_C \quad (5-16)$$

Example 5-8. Find the Q-point of the common-emitter transistor circuit given in Fig. 5-28(a). The BJT has a β_{DC} of 100. Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$.

Solution: First, we analyze the input to find I_B . This is indicated in Fig. 5-28(b). We use Eq. 5-15.

$$I_B = \frac{V_{CC} - 0.7 \text{ V}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega} = 10 \mu\text{A}$$

Next, we determine I_C . This is shown in Fig. 5-28(c).

$$I_C = \beta_{DC} I_B = (100)(10 \mu\text{A}) = 1 \text{ mA}$$

Figure 5-28(d) shows the application of Eq. 5-16 to find V_{CE} .

$$V_{CE} = V_{CC} - I_C R_C = 5 \text{ V} - (1 \text{ mA})(2 \text{ k}\Omega) = 3 \text{ V}$$

The collector saturation current $I_{C(SAT)}$ and the collector-emitter cutoff voltage $V_{CE(OFF)}$ are determined in the same manner as they were for the common-base BJT. The BJT is thought of as a closed switch between its collector and emitter. It drops no voltage and the current through this short circuit is called $I_{C(SAT)}$.

$$I_{C(SAT)} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{2 \text{ k}\Omega} = 2.5 \text{ mA}$$

The transistor behaves like an open switch when in cutoff. It passes no current. Consequently, no voltage is dropped across the collector resistor R_C . Since Kirchhoff's voltage law must be satisfied, the BJT drops all of the collector supply voltage V_{CC} . This is explained more fully in Section 5-10.

$$V_{CE(OFF)} = V_{CC} = 5 \text{ V}$$

Again, $I_{C(SAT)}$ is the largest DC collector current the BJT can experience while $V_{CE(OFF)}$ is the largest DC collector-emitter voltage the BJT will have to withstand. These quantities are useful when determining the ratings a BJT should possess for a given application.

5-9 The BJT Amplifier

A common-emitter BJT voltage amplifier is depicted in Fig. 5-29(a). This circuit is virtually identical to the circuit given in Fig. 5-28(a). However, two **coupling capacitors** C_1 and C_2 have been added. Their function is to isolate the BJT's DC bias while simultaneously allowing the AC signals to pass. **The coupling capacitors act like open circuits to DC and short circuits to AC.** All capacitors behave like open circuits in a DC circuit once they are charged. Consequently, the coupling capacitors are also called **DC blocking capacitors**. A capacitor's opposition to the flow of AC current is called its **capacitive reactance** (X_C). The capacitive reactance is measured in ohms and is given by Eq. 5-17. The frequency is f and C is the capacitance.

$$X_C = \frac{1}{2\pi f C} \quad (5-17)$$

The BJT Amplifier Signal Process

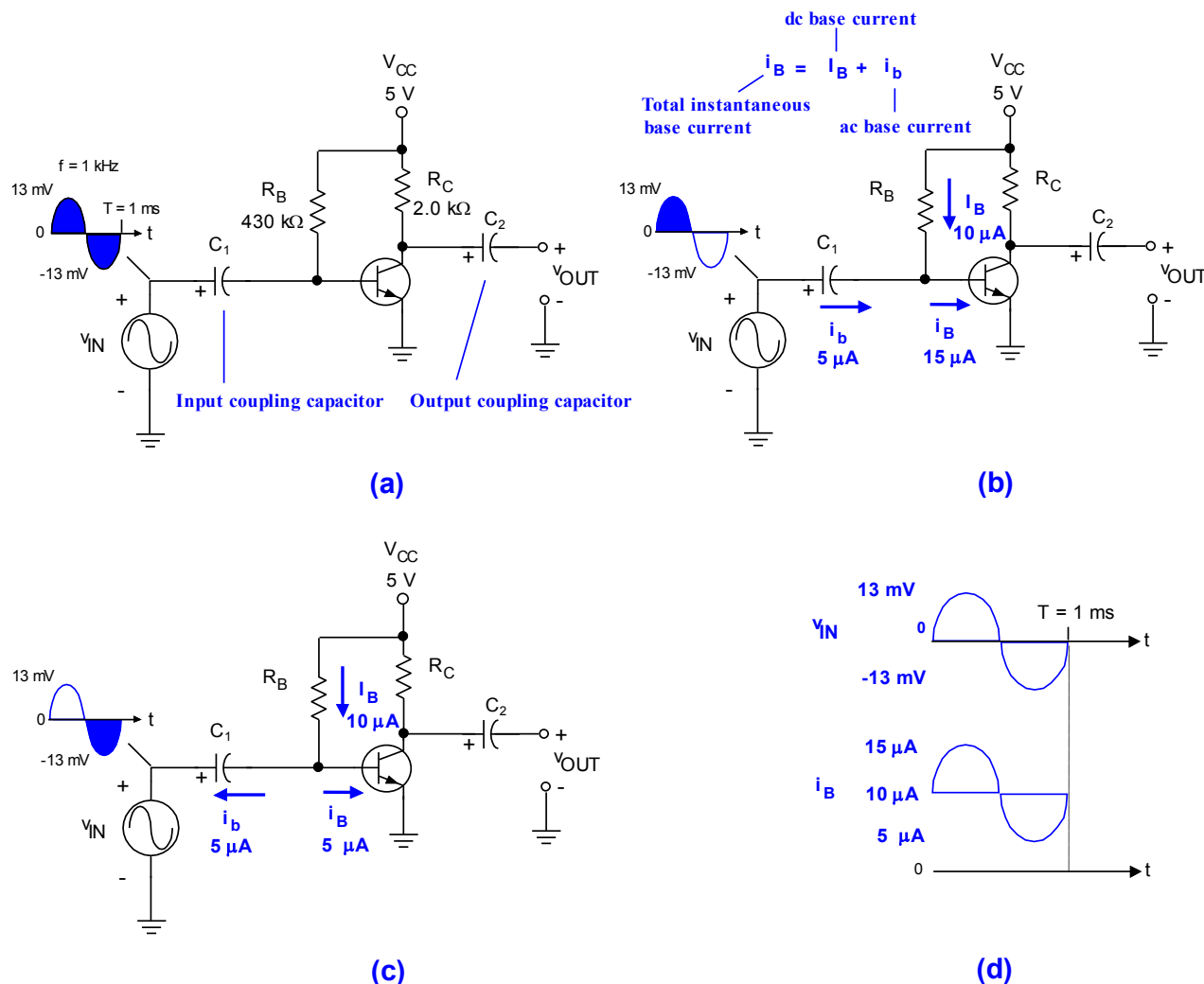


Figure 5-29.

For the capacitor to act like a short circuit, its capacitive reactance must be negligibly small at the lowest frequency of interest. For example, ***the audio frequency range is held to be from 20 Hz to 20 kHz.*** A coupling capacitor in a voltage amplifier designed to work over the entire audio frequency range should therefore have a small capacitive reactance at 20 Hz. This is accomplished by selecting a capacitor with a large enough capacitance (C).

The AC input signal (v_{IN}) can be produced by a laboratory function (waveform) generator, a crystal microphone, or the audio output signal of an MP3/MP4 player. In Fig. 5-9(a) we see that it is a 1-kHz sine wave with a peak value of 13 mV. When the AC input is positive, it will inject an additional current into the BJT's base terminal. This is shown in Fig. 5-29(b). ***The transistor's total instantaneous base current (i_B) is the sum of its DC base current (I_B) and its AC base current (i_b).*** This is defined by Eq. 5-18.

$$i_B = I_B + i_b \quad (5-18)$$

The choice of upper- and lowercase letters is significant and standardized. ***DC current is denoted using a (capital) I and a capital subscript (e.g., I_B). Pure AC current is denoted by a (lowercase) i and a lowercase subscript (e.g., i_b). The total instantaneous current mixes the cases. Specifically, it is given by using a (lowercase) i and a capital subscript (e.g., i_B). The only other possibility (not shown here) is effective (or rms) base current. It is given by using a (capital) I and a lowercase subscript (e.g., I_b).*** This notation convention also applies to voltages and should be memorized.

As we examine Fig. 5-29(b) and (c), we see that the AC signal current adds to and subtracts from the DC base current. ***The base-emitter is always forward biased, but the amount of forward bias is controlled by the signal source.*** The total instantaneous base current is in phase with v_{IN} as shown in Fig. 5-29(d).

The transistor is assumed to have an AC current gain (β) of 100. The transistor's total instantaneous collector current (i_C) is 100 times the total instantaneous base current. This is defined by Eq. 5-19 and illustrated in Fig. 5-30.

$$i_C = \beta i_B \quad (5-19)$$

This means the collector current is in phase with the base current (and v_{IN}) as indicated in Fig. 5-30(c).

The BJT Amplifier and Collector Current

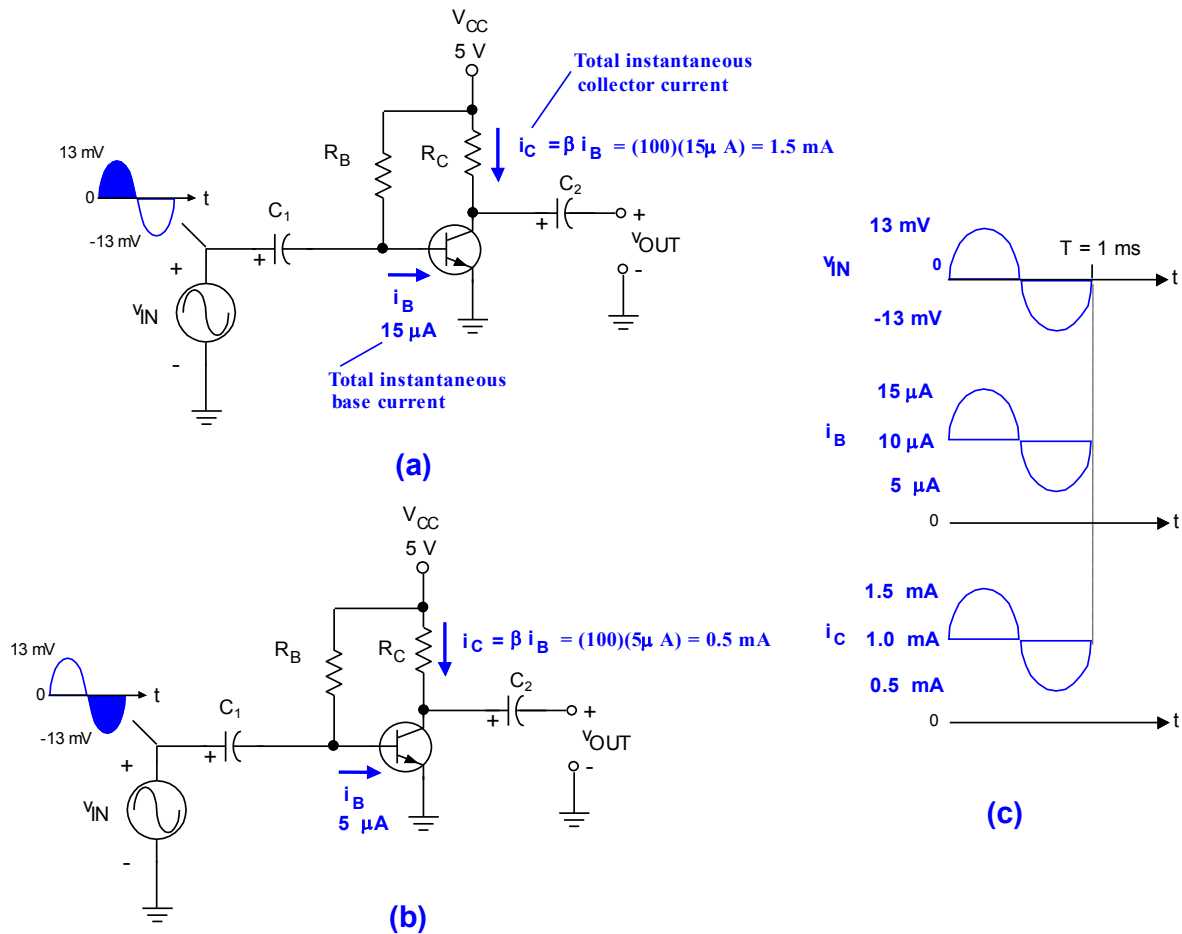


Figure 5-30.

The total instantaneous voltage drop across the collector resistor R_C is directly proportional to the total instantaneous collector current flowing through it. The voltage drop across the collector resistor plus the collector-emitter voltage drop must be equal to V_{CC} by Kirchhoff's voltage law. Consequently, the total instantaneous collector-emitter voltage v_{CE} is equal to V_{CC} minus the instantaneous voltage drop across the collector resistor. These relationships are provided by Eq. 5-20. Note the similarity between Eq. 5-20 and Eq. 5-16.

$$v_{CE} = V_{CC} - i_C R_C \quad (5-20)$$

Figure 5-31 illustrates the meaning of Eq. 5-20. **As the collector current increases, the collector-emitter voltage decreases. Conversely, as the collector current decreases, the collector-emitter voltage increases.**

This relationship is extremely important. It describes the fundamental operation of the common-emitter BJT. The collector-emitter voltage is 180° out of phase with respect to the input voltage V_{IN} as shown in Fig. 5-31(c). When the instantaneous collector current passes through its Q-point value of 1 mA, the instantaneous collector-emitter voltage is also equal to its Q-point value.

The BJT's collector is always more positive than the base in this example. This means the collector-base p - n junction is always reverse biased.

The BJT Amplifier and Collector-Emitter Voltage

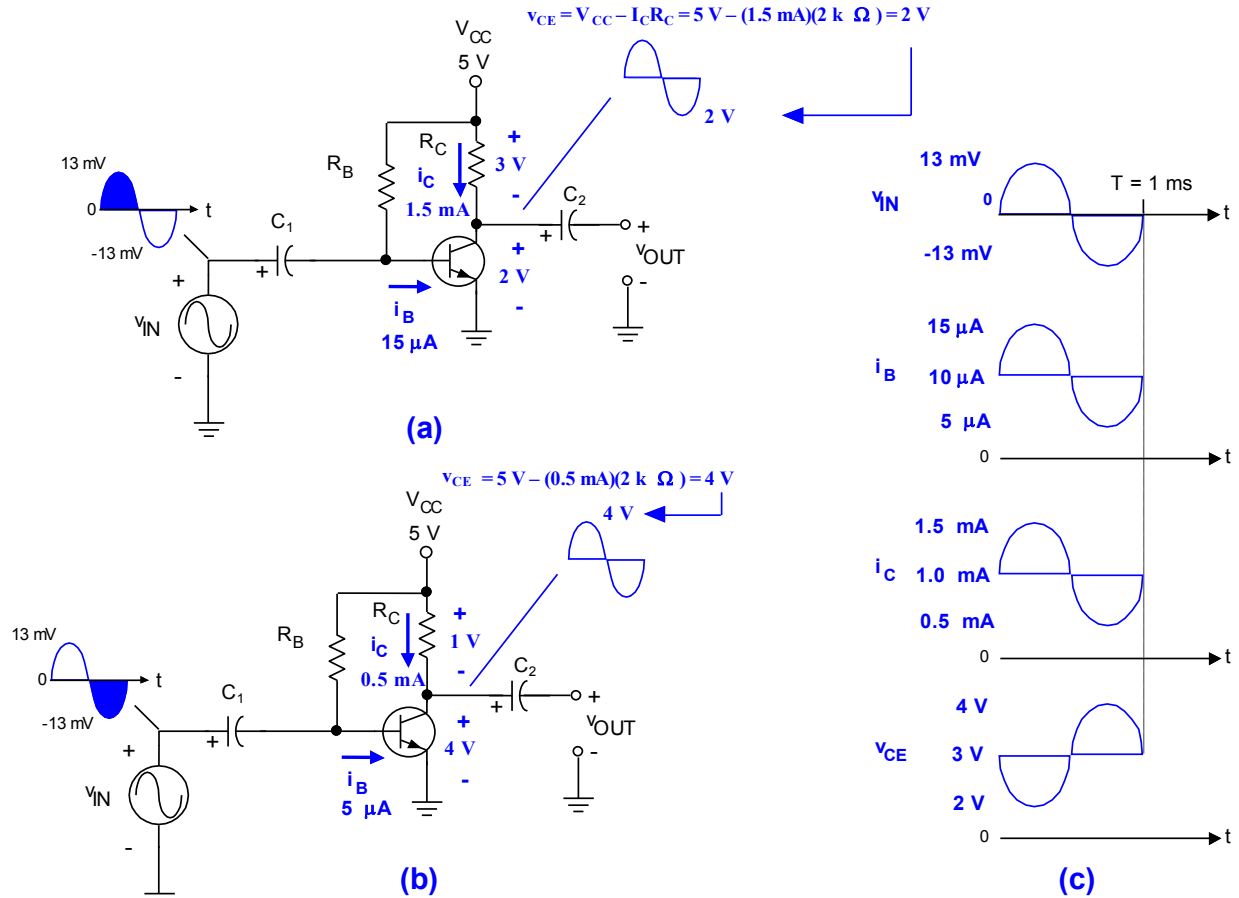


Figure 5-31.

Since the collector-emitter voltage is always positive, it can be viewed as a varying DC level. It may also be thought of as an AC sine wave riding on a DC level. The output coupling capacitor C_2 blocks the 3-V DC level. Consequently, the output of the amplifier is a 1-V peak AC sine wave as illustrated in Fig. 5-32.

The BJT Amplifier and Voltage Gain

- The output is 76.9 times larger than the input!
- This is voltage amplification.
- This 180 degrees of phase shift is NOT a problem.

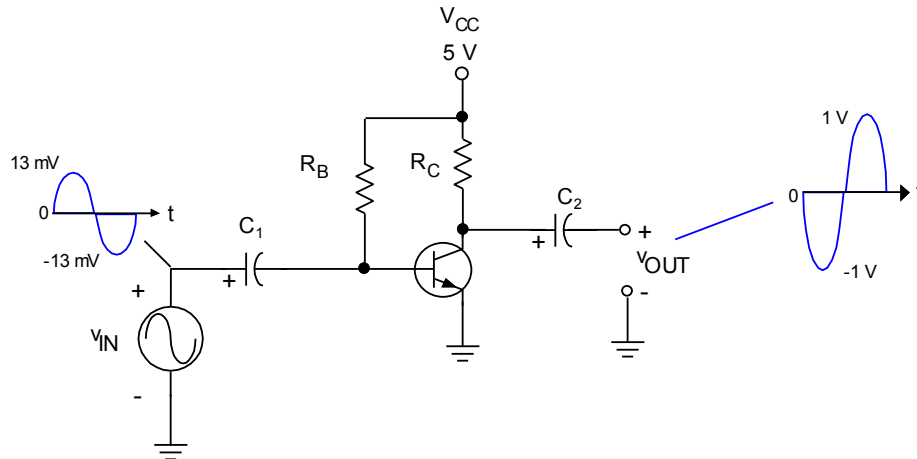


Figure 5-32.

The transistor has taken a small sine wave and made it larger without changing its shape. This is what linear amplification is all about. The 180° of phase shift, while significant, is not a problem. Because of this, the common-emitter amplifier is often described as an *inverting amplifier*. To describe the performance of a voltage amplifier, its **voltage gain** is determined. Voltage gain is defined by Eq. 5-21. The notation A_v suggests voltage **A**mplification.

$$A_v = \frac{v_{OUT}}{v_{IN}} \quad (5-21)$$

The voltage gain in Fig. 5-32 is determined using Eq. 5-21.

$$A_v = \frac{v_{OUT}}{v_{IN}} = \frac{1 \text{ V peak } \angle -180^\circ}{13 \text{ mV peak } \angle 0^\circ} = 76.9 \angle -180^\circ = -76.9$$

Remember that sine waves can be represented as phasors, and phasors have a magnitude and direction. They are often represented using *polar form notation*.⁴⁴ When dividing two phasors, we divide the magnitudes and subtract the denominator angle from the numerator angle. A phasor quantity with an angle of 180° can be represented by placing a minus sign in front of it. The minus sign merely indicates the phase relationship.

⁴⁴ Polar form notation has the form $A \angle \theta$ where A is the magnitude and θ is the angle (direction).

5-10 The Transistor Switch

As mentioned previously, when a BJT is in saturation (ON) it behaves like a closed switch. When a BJT is in cutoff (OFF) it acts like an open switch. This is depicted in Fig. 5-33.

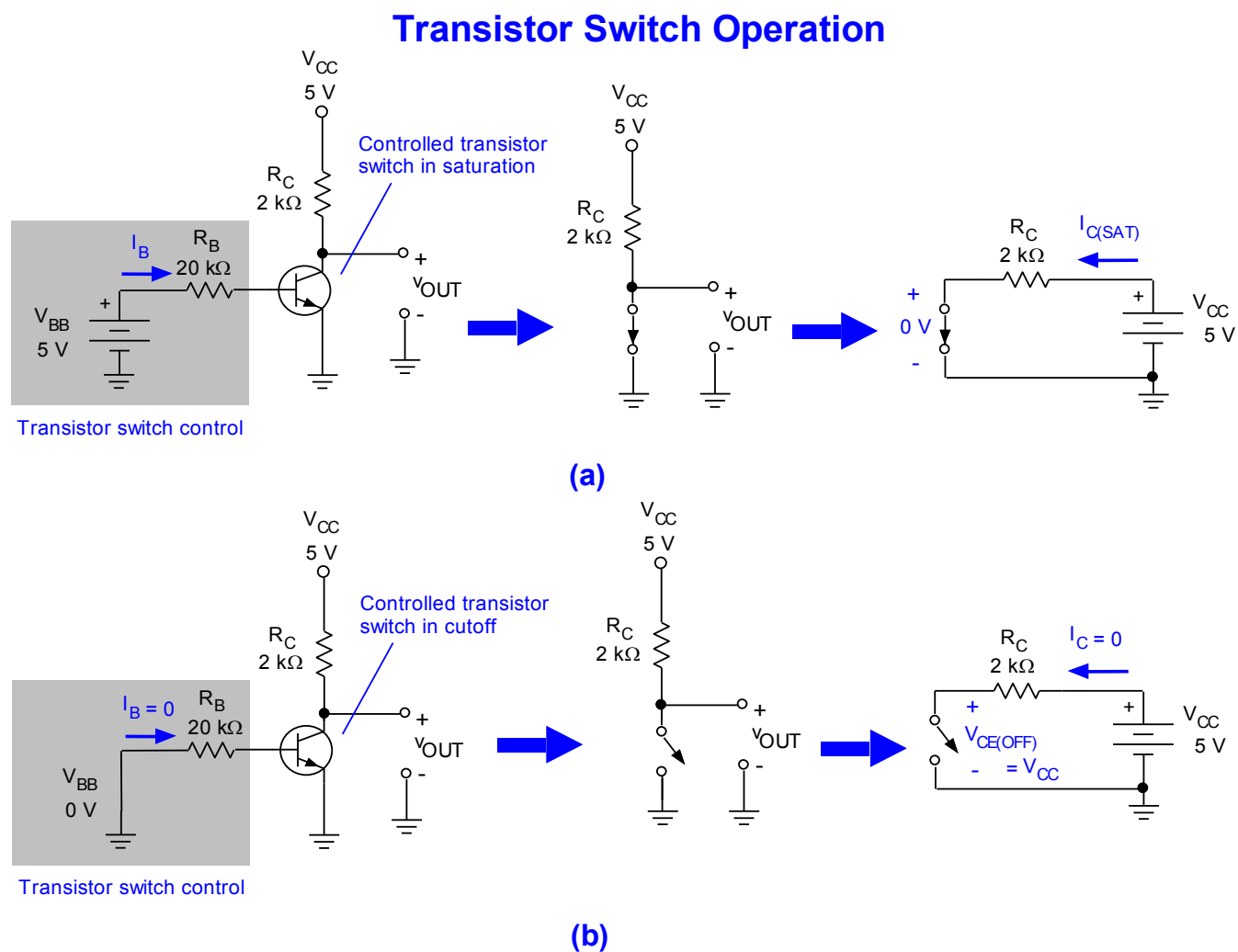


Figure 5-33.

Example 5-9. Perform a DC analysis of the transistor circuit given in Fig. 5-33(a). The BJT has a β_{DC} of 100. Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$. Repeat the analysis for Fig. 5-33(b).

Solution: First, we analyze the input to find I_B . We use Eq. 5-15, but the base bias supply is V_{BB} instead of V_{CC} .

$$I_B = \frac{V_{BB} - 0.7 \text{ V}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{20 \text{ k}\Omega} = 215 \mu\text{A}$$

Next, we determine I_C .

$$I_C = \beta_{DC} I_B = (100)(215 \mu\text{A}) = 21.5 \text{ mA}$$

We apply Eq. 5-16 to find V_{CE} .

$$V_{CE} = V_{CC} - I_C R_C = 5 \text{ V} - (21.5 \text{ mA})(2 \text{ k}\Omega) = -38 \text{ V}$$

Obviously, something is wrong. The collector-emitter voltage cannot be this large, and it certainly cannot become *negative*! The answer is the collector current cannot be 21.5 mA. The transistor's external circuit will limit I_C to $I_{C(SAT)}$.

$$I_{C(SAT)} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{2 \text{ k}\Omega} = 2.5 \text{ mA}$$

The BJT's collector-emitter voltage will be zero. The BJT's collector-emitter saturation voltage is denoted $V_{CE(SAT)}$.

$$V_{CE} = V_{CE(SAT)} = 0 \text{ V}$$

In Fig. 5-33(b) the BJT's base current is zero. This means its collector current must also be zero. The BJT is at the edge of its cutoff region. The transistor behaves like an open switch when in cutoff. It passes no current. Consequently, no voltage is dropped across the collector resistor R_C . Since Kirchhoff's voltage law must be satisfied, the BJT drops all of the collector supply voltage V_{CC} .

$$V_{CE(OFF)} = V_{CC} = 5 \text{ V}$$

A transistor in saturation has a **forced beta** β_F . The forced beta is the ratio of the BJT's collector current to its corresponding base current when the BJT is in saturation. The forced beta is given by Eq. 5-22.

$$\beta_F = \frac{I_{C(SAT)}}{I_B} \quad (5-22)$$

Example 5-10. Determine the forced beta for the BJT circuit given in Fig. 5-32(a).

Solution: From our work in Example 5-9, we know I_B is 215 μA and $I_{C(SAT)}$ is 2.5 mA. **All we must do is apply Eq. 5-22.**

$$\beta_F = \frac{I_{C(SAT)}}{I_B} = \frac{2.5 \text{ mA}}{215 \mu\text{A}} = 11.6$$

The forced beta is 11.6, which is much lower than the transistor's linear beta (β_{DC}) of 100.

When a transistor is taken to the verge of cutoff by reducing its base current to zero, the transistor's base terminal must *not* be allowed to *float*. A **floating input terminal is unconnected input terminal**.

A BJT with a floating input is depicted in Fig. 5-34(a). The BJT's leakage current (I_{CBO}) can cause the transistor to turn itself on. This will cause the BJT's power dissipation to increase. The increase in power dissipation produces a temperature rise. The rise in temperature produces additional minority carriers. The corresponding increase in leakage current causes additional base current, and the process continues. Remember this is called thermal runaway. The fix is simple. An additional resistor is tied between the BJT's base and emitter terminals. This resistor diverts some of the leakage current away from the BJT's base terminal. This prevents the BJT from turning itself on, and the BJT remains in cutoff. This is illustrated in Fig. 5-34(b).

Defeating Leakage Current

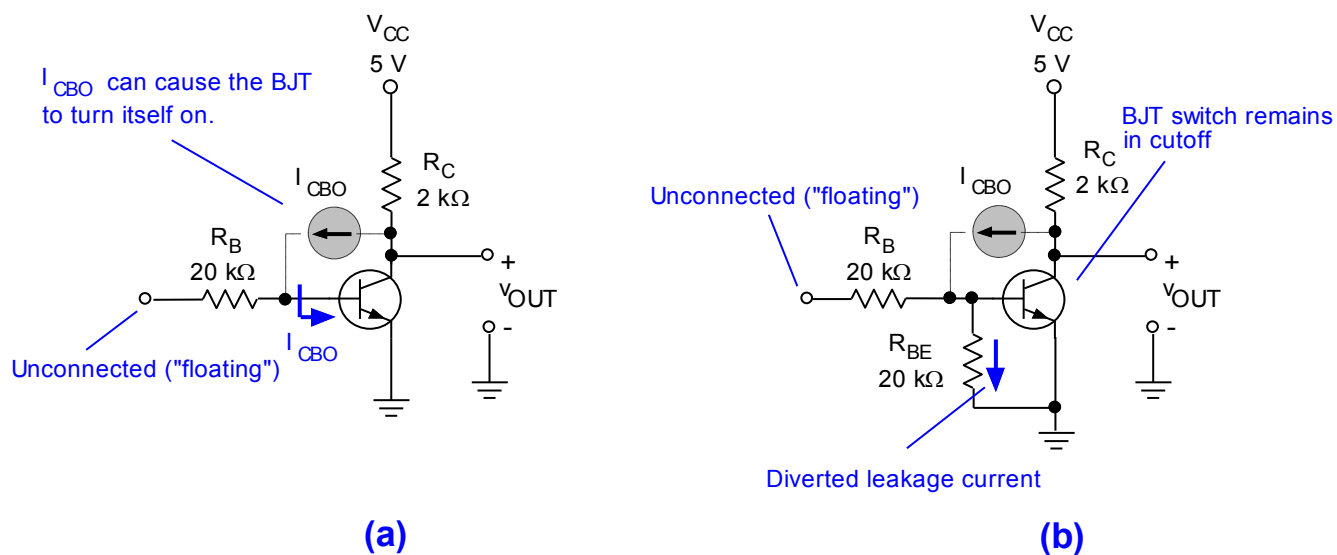


Figure 5-34.

The use of R_{BE} provides many advantages. It makes the BJT switch less susceptible to the effects of I_{CBO} , increases the BJT's voltage rating, and makes it switch faster. We shall investigate transistor switches in more detail as our work progresses.

5-11 The Clapper

The *Clapper* is the name we have given to a small toy robot. It spins when it "hears" a loud clap. Transistor switches are fundamental to its operation. It is an interesting way to learn about transistor switches. Quite often, technicians and engineers need to become familiar with circuits *without* analyzing them in detail. We use that approach here. Put away your calculator!

The block diagram of the Clapper is provided in Fig. 5-35. The loudspeaker is a *transducer*. A transducer is a device that converts one form of energy into another. In this case, the loudspeaker is used to convert sound (acoustical energy) into an electrical signal. The electrical signal produced

by the loudspeaker is used to trigger a timing circuit. The timing circuit controls a transistor that acts like a switch. This switch is used to control the DC power applied to the motor. The motor causes the Clapper to spin. When the loudspeaker detects a sharp sound (such as a clap) it triggers the timer. The timer turns on the transistor switch that applies power to the motor and the motor begins to run. When the timer times out (after a few seconds) the transistor switch opens which removes power from the motor which (of course) stops it.

An astute engineer or technologist might make the following observation: “Suppose the motor is mechanically noisy. Won’t that re-trigger the clapper? That means it will never stop. Sound triggers the action and motor acoustical noise could keep re-triggering it.” Simple questions such as this could save a company a great deal of money. If a design with a fundamental flaw progresses very far, the entire project could be scrapped. Questions are good. Initially, there are no stupid questions. Be critical in your observations and your thinking.

By the way, the circuit design provided in this project *is* immune to acoustical noise while it is timing out. The loudspeaker has also been isolated from mechanical vibrations [see Fig. 5-45]. It can only be re-triggered after it has timed out.

The Clapper Block Diagram

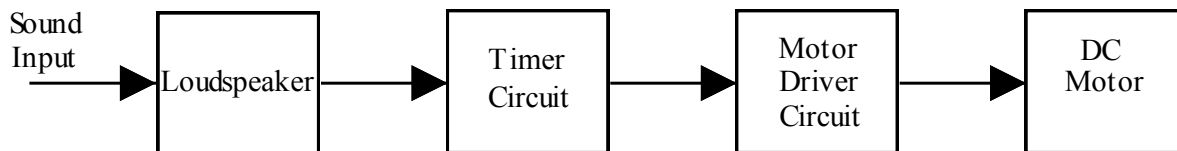
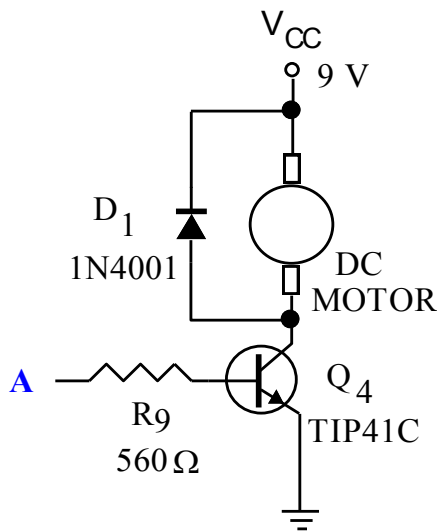


Figure 5-35.

We shall start our explanation of the Clapper circuitry by **starting with the motor** and working our way **backward toward the loudspeaker**. The motor and part of its drive circuit are shown in Fig. 5-36.

The Motor and Part of Its Drive Circuit



- When point A is at 9 V, transistor Q₄ is ON and the motor will run.
- When point A is at 0 V transistor Q₄ is OFF and the motor will stop running.
- Diode D₁ serves a protective function and is called a "free wheeling" diode.
- Transistor Q₄ is a plastic power transistor and is mounted to a heat sink.

Figure 5-36.

To help us contrast the differences between (analog) amplifier and (digital) switching applications, we define the terms *analog* and *digital* from a signal perspective. **Analog signals can assume an infinite number of possible values between two finite limits. Digital signals can only assume a finite number of possible values between two finite limits.** A transistor switch is a digital application of a transistor. For example, the input at point A in Fig. 5-36 is assumed to be either at 9 V or at 0 V. Thus, only two input states are possible ideally. When the input is at 9 V, it can be referred to as a HI input. When the input is at 0 V, it can be described as a LO input.

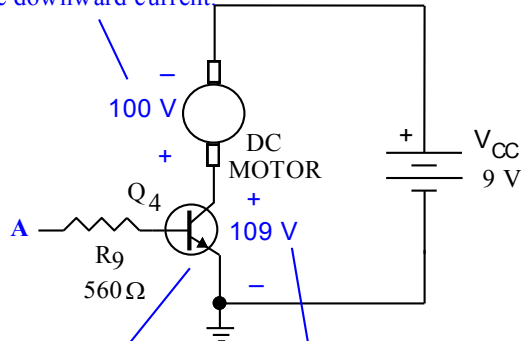
Transistor Q₄ is a plastic power transistor mounted to a heat sink. When point A is tied to 9 V (HI), the transistor turns on (ON) and acts like a closed switch. The motor will run. When point A is tied to ground (LO), transistor Q₄ is in cutoff (OFF), and it acts like an open switch. When transistor Q₄ goes into cutoff the motor will be de-energized. Diode D₁ is called a **free-wheeling diode**. The motor has a lot of inductance.⁴⁵ Current flows down through the motor when it is running. When Q₄ attempts to interrupt the motor's current, the motor's inductance will attempt to maintain the downward current by generating a large counter voltage. When this occurs, diode D₁ will conduct to help discharge the energy stored within the motor's inductance. The maximum voltage produced by the motor's inductance will be limited to one forward-biased diode drop. The diode action is illustrated in Fig. 5-37.

In Fig. 5-37(a), we see that without the diode, the BJT's collector-emitter voltage can rise to a large value. If the applied voltage exceeds the BJT's maximum voltage rating, the BJT can fail. The most common failure mode is for the BJT to fail with a collector-to-emitter short circuit, which means the motor will never turn off. Figure 5-37(b) shows how the diode protects the transistor. The diode's conduction limits the counter voltage to one diode voltage drop.

⁴⁵ Remember: Inductance is that circuit property which opposes a change in current and stores energy in a magnetic field.

The Free Wheeling Diode Operation

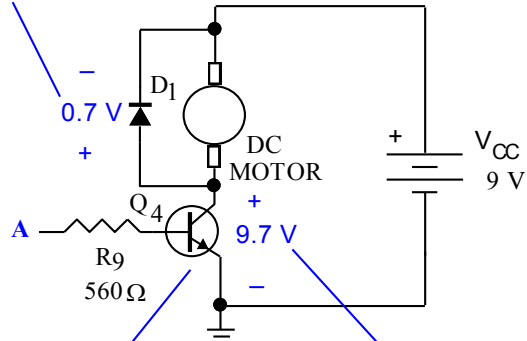
The motor's inductance produces a counter voltage to try to continue the downward current.



The BJT is turned OFF. The BJT must withstand the counter voltage plus V_{CC} .

(a)

The diode conducts to suppress the motor's counter voltage.



The BJT is turned OFF. Now the BJT must withstand V_{CC} plus one diode voltage drop.

(b)

Figure 5-37.

The balance of the motor drive circuit is provided in Fig. 5-38. Transistor Q_3 is a *pn*p device. Recall that the operation of a *pn*p BJT is identical to that of an *np*n BJT. However, the voltages and currents are *reversed*. When point B is taken to ground (LO), transistor Q_3 will turn on. Its emitter will be 0.7 V more positive than its base terminal. Base current will flow out of the base terminal and through resistor R_6 to ground. Q_3 's collector current will flow out of its collector and down through resistor R_8 and the LED.

The Complete Motor Driver Circuit

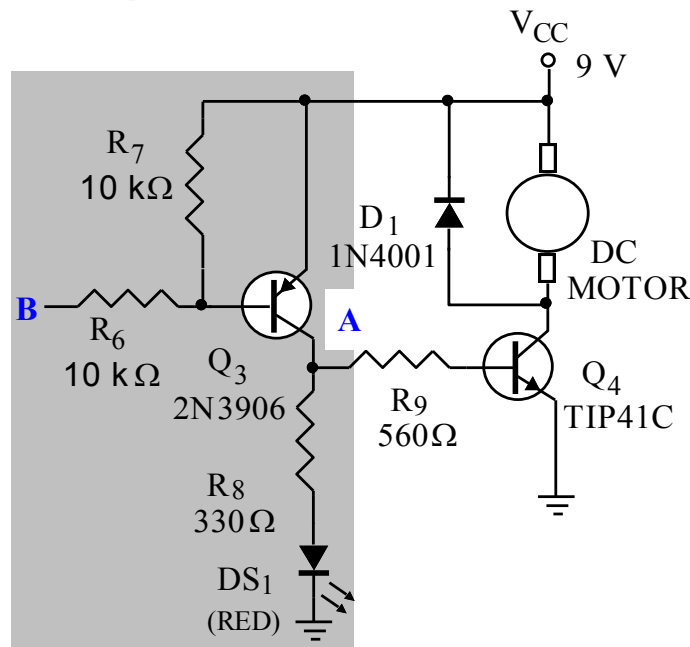


Figure 5-38.

Therefore, when Q_3 conducts, point A is effectively connected to the 9-V supply. This will cause the LED to illuminate, and transistor Q_4 to conduct. When transistor Q_4 conducts, the motor will run. When point B goes to 9 V (HI), the base and emitter terminals of transistor Q_3 will be at the *same* potential⁴⁶. Since its base-emitter receives no bias, transistor Q_3 will be OFF. Point A will be pulled to ground, the LED will be extinguished, and transistor Q_4 will be OFF, which removes power from the motor.

To summarize, when point B is LO, the LED will be illuminated, and the motor will run. When point B is HI, the LED will be extinguished, and the motor will not run. The LED indicates when the motor is being commanded to run. This can be a useful diagnostic aid should the motor become stalled due to a mechanical problem, or a weak battery.

The timer circuitry employs two separate transistor switches, and a capacitor. We add transistor switch Q_2 to our composite schematic diagram in Fig. 5-39. When point C is HI transistor Q_2 is ON. When transistor Q_2 is ON, point B is taken to ground (LO). This turns Q_3 ON. When Q_3 is ON, the LED is illuminated, Q_4 is ON, and the motor is energized.

When point C is LO, Q_2 is OFF. This means point B is HI. Consequently, Q_3 is OFF, the LED is extinguished, Q_4 is OFF, and the motor is de-energized.

Transistor Q_2 is Added.

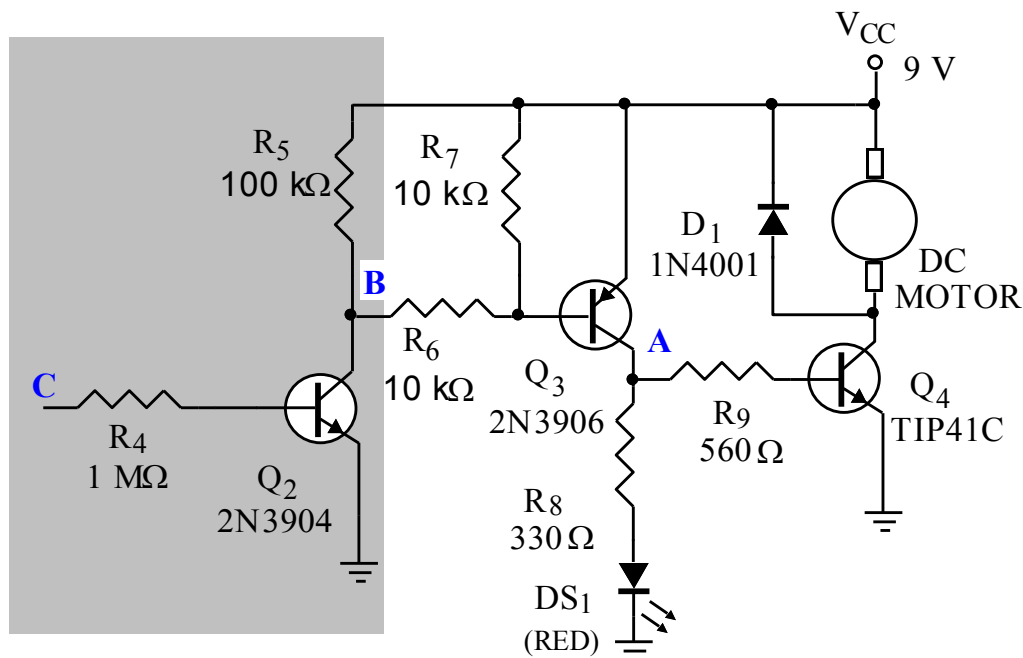


Figure 5-39.

⁴⁶ Same potential (with respect to ground) means there is no voltage difference between the base and emitter terminals. That means the voltage across the base-emitter *pn* junction.

Transistor Q_1 is included as shown in Fig. 5-40. While transistor Q_1 and its associated bias resistors R_1 and R_2 , look like they form a common-emitter amplifier, they do *not*! The forced beta (β_F) is 23.9. However, the 2N3904's minimum DC beta (β_{DC}) is 40. This places transistor Q_1 into saturation. Consequently, point C is LO, point B is HI, point A is LO, and both the LED and the motor are de-energized. If the base-emitter bias of transistor Q_1 is *removed*, the BJT will go into cutoff. This means point C will be HI, point B will be LO, transistor Q_3 will be ON, point A will be HI, and both the LED and the motor will be energized.

Transistor Q_1 is Added.

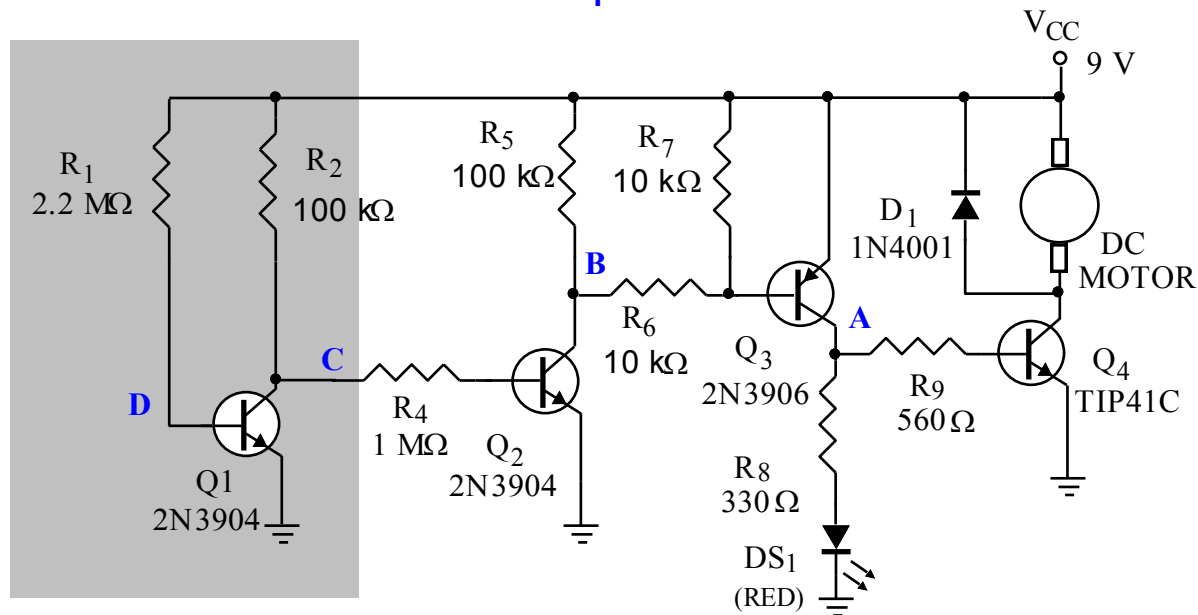


Figure 5-40.

The forward bias across the base-emitter terminals of transistor Q_1 , can be removed by the AC signal produced by a loudspeaker. Our next step is to investigate the operation of the loudspeaker. Its behavior is described in Fig. 5-41.

A loudspeaker is normally used to convert electrical energy into acoustical energy. However, in this project we are adapting a low-cost loudspeaker to serve as a microphone.⁴⁷

When an electrical conductor moves through a magnetic field, a voltage is induced in it. (This is the fundamental principle underlying the operation of an electric generator.) Therefore, since the voice coil is attached to the vibrating paper cone, it moves through the magnetic field produced by the stationary permanent magnet. Consequently, a voltage that is proportional to the movement of the paper cone is developed in the voice coil. The result is we end up with an electrical signal that represents the sounds detected by the loudspeaker.

⁴⁷ Historically, this was done quite often in the now ancient intercom systems.

Operation of the Loudspeaker as a Microphone.

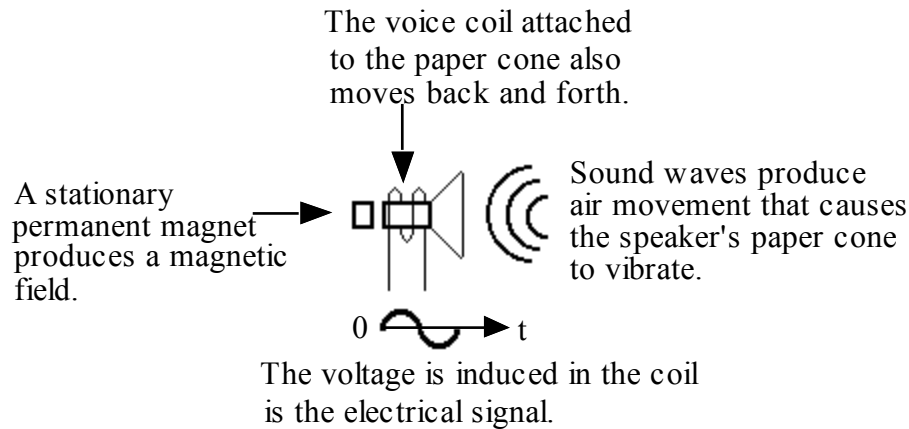


Figure 5-41.

As can be seen in Fig. 5-41, sound produces an ac electrical output from the loudspeaker. When the signal is negative, it can be used to remove the forward bias from the base-emitter of transistor Q_1 . In fact, a loud clap in proximity will produce a rather nasty looking positive- and negative-going voltage spike. Consequently, the loudspeaker's output is connected across Q_1 's base-emitter terminals. Because electrical resistance of the voice coil is so low, a coupling capacitor is used to block the DC bias as shown in Fig. 5-42⁴⁸. Observe that C_1 is a polarized electrolytic capacitor.

The Loudspeaker is Added

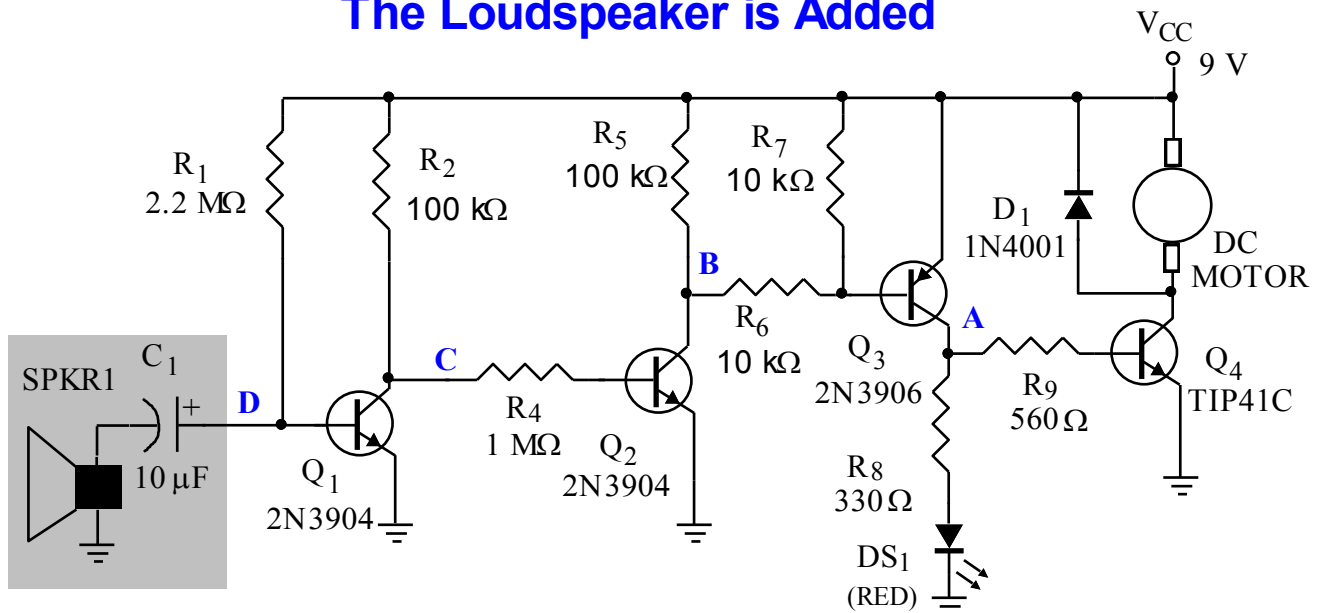


Figure 5-42.

⁴⁸ In general loudspeakers hate DC. It can cause their diaphragm (paper cone) to become pinned. It can also cause their voice coil to be burned out if the current is not limited to a safe value.

The last portion to be added is the timing capacitor. Refer to Fig. 5-43. Capacitor C_2 is another polarized aluminum electrolytic capacitor. In the resting state, transistor Q_1 is ON and transistor Q_2 is OFF. Point D is about 0.7 V above ground and point B is pulled to 9 V. Capacitor C_2 will charge through resistors R_5 and R_3 until the voltage across it is 8.3 V. The voltage polarity across the capacitor is shown in Fig. 5-44(a).

The Complete Clapper

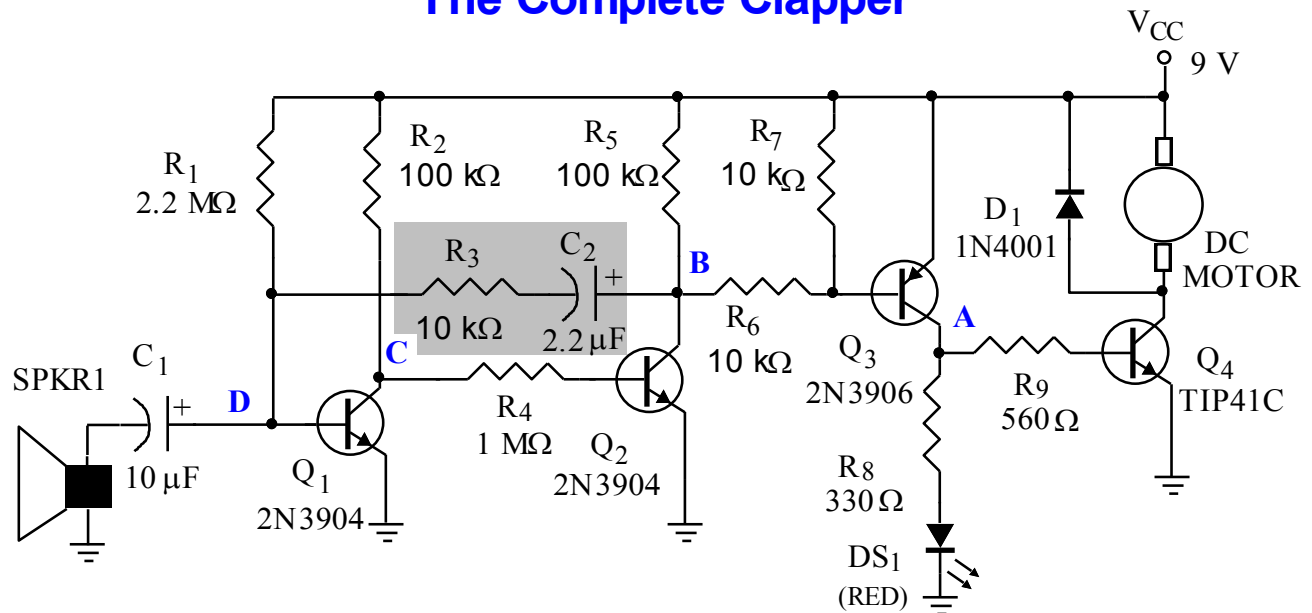


Figure 5-43.

When a clap is detected by the loudspeaker, a negative voltage spike will be developed between the base-emitter terminals of transistor Q_1 . This will cause Q_1 to go OFF. This means point C goes HI. This turns Q_2 ON. This results in the right end of C_2 being taken to ground through Q_2 . This is depicted in Fig. 5-44(b). The negative terminal of C_2 is tied to the base of Q_1 through resistor R_3 . This holds Q_1 OFF. Consequently, Q_3 is held ON, Q_4 is held ON, and both the LED and the motor remain energized. This condition is shown in Fig. 5-44(c).

This temporary condition lasts while capacitor C_2 charges toward V_{CC} through resistors R_1 and R_3 . When the voltage across the capacitor reaches nearly zero volts, the circuit will revert to its stable state. [Refer to Fig. 5-44(d).] This means Q_1 will turn ON, and transistors Q_2 , Q_3 , and Q_4 will all turn OFF. Subsequently, the LED and the motor will become de-energized.

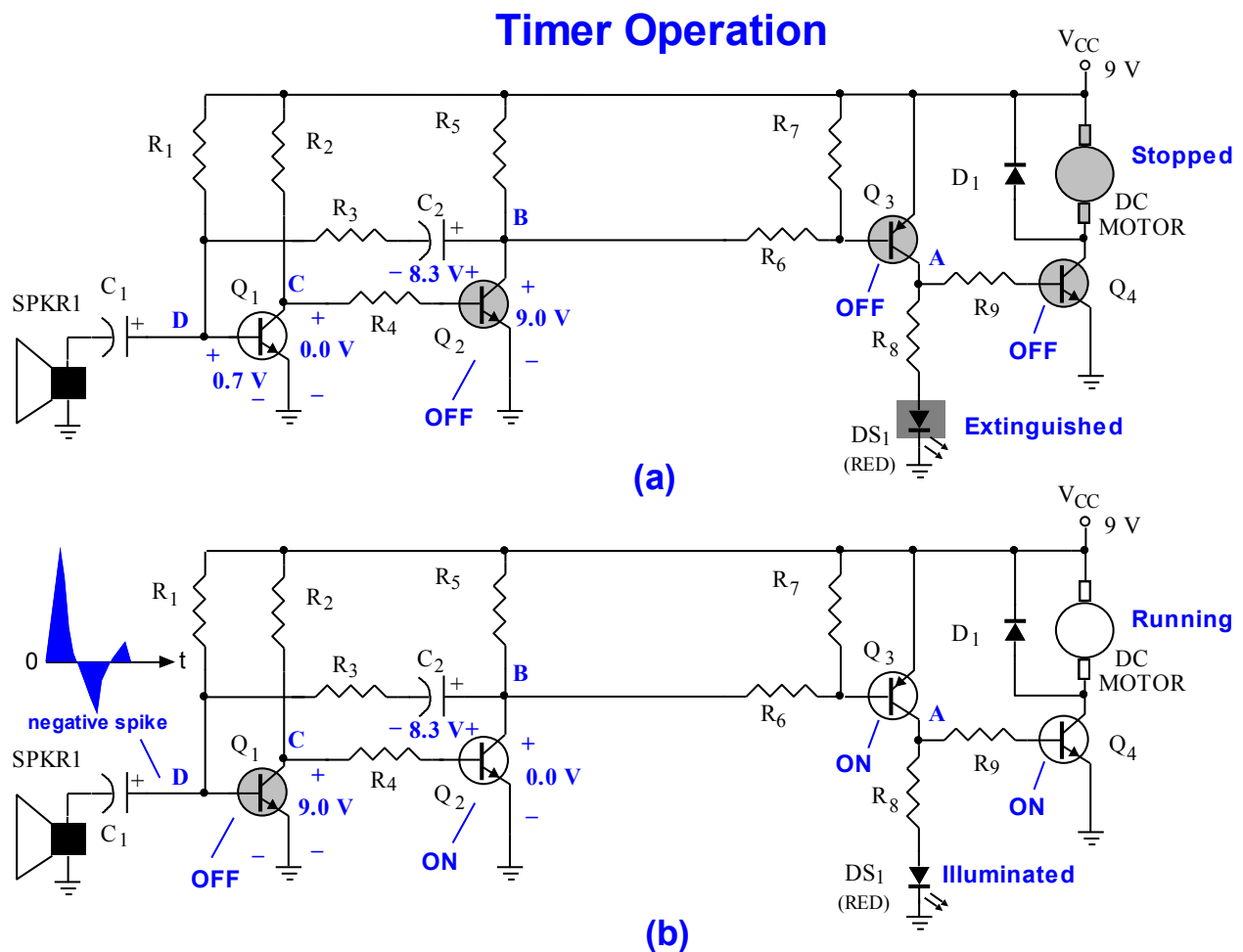


Figure 5-44.

Timer Operation (continued)

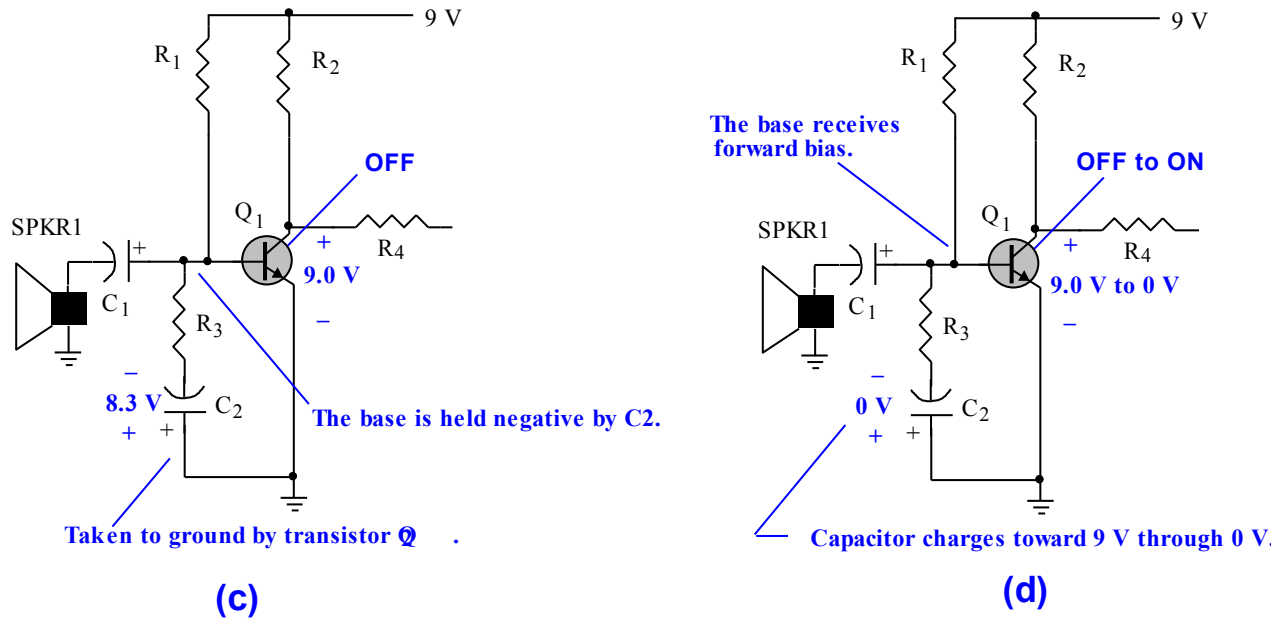


Figure 5-44 (continued).

The actual Clapper robot is shown in Fig. 5-45⁴⁹. The motor is geared down to provide adequate torque. The wheels are positioned such that the unit spins around in a circle when it runs.

The Clapper

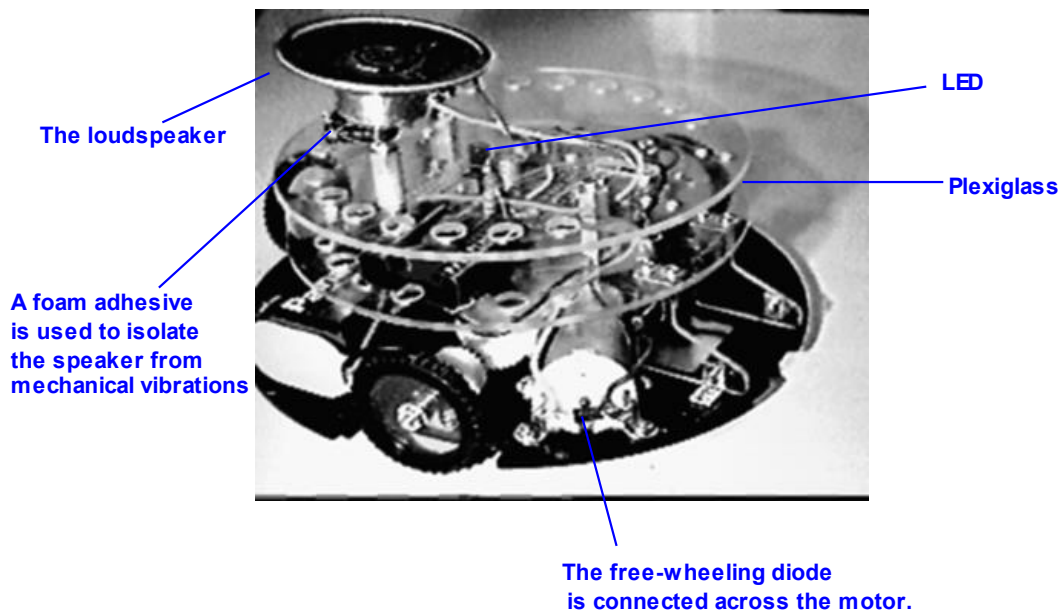


Figure 5-45.

⁴⁹ The Clapper was constructed by Mr. Steve Soenksen at Rock Valley College. Of course, this was when he *worked* there. He is still there but moved into management.

Problems for Chapter 5

Drill Problems

Section 5-1

- 5-1 In virtually all schematic symbols for electronic devices, the arrow points toward the _____ (*p*-type, *n*-type) material.
- 5-2 The largest region within a transistor is the _____ (base, collector, emitter) region.
- 5-3 The thinnest region within a transistor is the _____ (base, collector, emitter) region.
- 5-4 The most heavily doped region within a transistor is the _____ (base, collector, emitter) region.
- 5-5 A single *p-n* junction exists between the collector and emitter terminals of a bipolar junction transistor. True or False?
- 5-6 The n^- collector region is _____ (heavily, moderately, lightly) doped.

Section 5-2

- 5-7 *Donor* impurities are _____ (trivalent, tetravalent, pentavalent) atoms that contribute _____ (holes, electrons) to form a(an) _____ (*p*-, *n*-) type semiconductor.
- 5-8 *Acceptor* impurities are _____ (trivalent, tetravalent, pentavalent) atoms that contribute _____ (holes, electrons) to form a(an) _____ (*p*-, *n*-) type semiconductor.
- 5-9 In the depletion region that forms at a *p-n* junction, _____ (positive, negative) ions form on the *p*-side of the junction.
- 5-10 In the depletion region that forms at a *p-n* junction, _____ (positive, negative) ions form on the *n*-side of the junction.
- 5-11 A depletion region will extend *further* into a heavily doped semiconductor when compared to a lightly doped semiconductor. True or False?
- 5-12 The effective base region of a BJT is very _____ (wide, narrow).

Section 5-3

- 5-13 To be used as an amplifier, an *npn* BJT must have a _____ (forward-, reverse-biased) emitter-base *p-n* junction and a _____ (forward-, reverse-biased) collector-base *p-n* junction.
- 5-14 To be used as an amplifier, a *pnp* BJT must have a _____ (forward-, reverse-biased) emitter-base *p-n* junction and a _____ (forward-, reverse-biased) collector-base *p-n* junction.
- 5-15 Cite two reasons why the BJT base current is normally very small. Base your answers on the physical construction of the BJT.

- 5-16 A BJT has an I_E of 2.5 mA and an I_B of 100 μA . Find its corresponding I_C .
- 5-17 A BJT has an I_E of 1.5 mA and an I_C of 1.45 mA. Find its corresponding I_B .
- 5-18 A BJT has an I_C of 3.0 mA and an I_B of 0.02 mA. Find its corresponding I_E .
- 5-19 If V_{BE} is -0.4 V , what is V_{EB} ?
- 5-20 If V_{EB} is -0.65 V , what is V_{BE} ?
- 5-21 Name the two currents and the BJT terminal voltage that can be regarded to control the collector current I_C .
- 5-22 Explain (briefly) why the collector region is the largest of the three BJT regions.

Section 5-4

- 5-23 The *input* terminal of the common-collector BJT is its _____ (base, collector, or emitter) while its *output* terminal is its _____ (base, collector, or emitter).
- 5-24 The *input* terminal of the common-base BJT is its _____ (base, collector, or emitter) while its *output* terminal is its _____ (base, collector, or emitter).
- 5-25 The *input* terminal of the common-emitter BJT is its _____ (base, collector, or emitter) while its *output* terminal is its _____ (base, collector, or emitter).
- 5-26 A BJT has a β_{DC} of 200 and an I_C of 2 mA. Find its I_B , I_E , and α_{DC} .
- 5-27 A BJT has a β_{DC} of 150 and an I_B of 0.02 mA. Find its I_C , I_E , and α_{DC} .
- 5-28 A BJT has an α_{DC} of 0.997 and an I_E of 1.5 mA. Find its I_C , I_B , and β_{DC} .
- 5-29 A BJT has an α_{DC} of 0.980 and an I_C of 2 mA. Find its I_E , I_B , and β_{DC} .
- 5-30 A transistor has a base current (I_B) of 25 μA and an α_{DC} of 0.995. Determine its collector current (I_C).
- 5-31 A transistor has an emitter current (I_E) of 2.5 mA and a β_{DC} of 120. Determine its collector current (I_C).
- 5-32 In neat systematic detail, perform the necessary algebra to derive Eq. 5-8 from Eq. 5-7.

Section 5-5

- 5-33 A transistor has an α_{DC} of 0.997 and an I_E of 1.5 mA. Its collector-base leakage current I_{CBO} is 25 nA. Use Eq. 5-9 to determine the collector current. Is it reasonable to assume that I_{CBO} is negligible?
- 5-34 A transistor has an α_{DC} of 0.990 and an I_E of 0.5 mA. Its collector-base leakage current I_{CBO} is 15 nA. Use Eq. 5-9 to determine the collector current. Is it reasonable to assume that I_{CBO} is negligible?
- 5-35 A BJT has a β_{DC} of 200 and an I_{CBO} of 5 nA. Find its collector-emitter leakage current I_{CEO} .
- 5-36 A BJT has a β_{DC} of 150 and an I_{CBO} of 10 nA. Find its collector-emitter leakage current I_{CEO} .

- 5-37 A transistor has a β_{DC} of 120, a base current I_B of 25 μA and an I_{CEO} of 100 nA. Use Eq. 5-11 to determine the collector current. Is it reasonable to assume that I_{CEO} is negligible?
- 5-38 A transistor has a β_{DC} of 50, a base current I_B of 100 μA and an I_{CEO} of 20 nA. Use Eq. 5-11 to determine the collector current. Is it reasonable to assume that I_{CEO} is negligible?
- 5-39 The thermal runaway phenomenon explains why a BJT's collector current tends to _____ (increase, decrease) as the BJT's temperature is elevated.

Section 5-6

- 5-40 According the transistor convention, currents that flow out of a BJT are called _____ (positive, negative).
- 5-41 An *npn* transistor has a maximum collector current rating of 200 mA. A manufacturer's data sheet would list it as _____ (200 mA, -200 mA).
- 5-42 A *pnp* transistor has a maximum collector current rating of 60 mA. A manufacturer's data sheet would list it as _____ (60 mA, -60 mA).

Section 5-7

- 5-43 When a BJT is to be used as an *amplifier*, it is operated in its _____ (active, cutoff, saturation) region of operation.
- 5-44 When a BJT is operated in its _____ (active, cutoff, saturation) region of operation, it behaves like an *open* switch.
- 5-45 When a BJT is operated in its _____ (active, cutoff, saturation) region of operation, it behaves like a *closed* switch.
- 5-46 A BJT in its *active* region of operation has a _____ (forward-, reverse-) biased emitter-base *p-n* junction, and a _____ (forward-, reverse-) biased collector-base *p-n* junction.
- 5-47 A BJT in its *cutoff* region of operation has a _____ (forward-, reverse-) biased emitter-base *p-n* junction, and a _____ (forward-, reverse-) biased collector-base *p-n* junction.
- 5-48 A BJT in its *saturation* region of operation has a _____ (forward-, reverse-) biased emitter-base *p-n* junction, and a _____ (forward-, reverse-) biased collector-base *p-n* junction.
- 5-49 Modify the test circuit given in Fig. 5-14(a) so that it can be used to produce *the common-base input curves for an npn BJT*. Draw a neat schematic diagram. Indicate the polarities, and label it completely.
- 5-50 Modify the test circuit given in Fig. 5-15(a) so that it can be used to produce *the common-base output curves for a npn BJT*. Draw a neat schematic diagram. Indicate the polarities, and label it completely.
- 5-51 Modify the test circuit given in Fig. 5-18(a) so that it can be used to produce *the common-emitter input curves for a npn BJT*. Draw a neat schematic diagram. Indicate the polarities, and label it completely.

Section 5-8

- 5-52 Find the Q-point of the common-base transistor given in Fig. 5-46(a). Specifically, find I_E , I_C , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CB(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an α_{DC} of 0.997.
- 5-53 Find the Q-point of the common-base transistor given in Fig. 5-46(b). Specifically, find I_E , I_C , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CB(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an α_{DC} of 0.990.
- 5-54 Find the Q-point of the common-base transistor given in Fig. 5-46(c). Specifically, find I_E , I_C , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CB(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an α_{DC} of 0.97.
- 5-55 Find the Q-point of the common-base transistor given in Fig. 5-46(d). Specifically, find I_E , I_C , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CB(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an α_{DC} of 0.95.

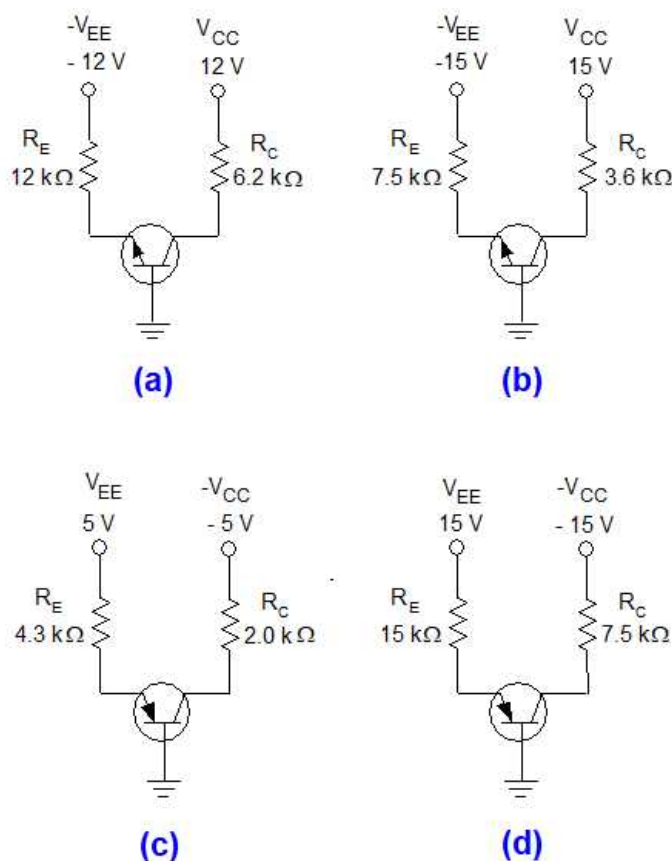


Figure 5-46.

- 5-56 Find the Q-point of the common-emitter transistor given in Fig. 5-47(a). Specifically, find I_B , I_C , V_{CE} , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an β_{DC} of 100.

- 5-57 Find the Q-point of the common-emitter transistor given in Fig. 5-47(b). Specifically, find I_B , I_C , V_{CE} , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an β_{DC} of 150.
- 5-58 Find the Q-point of the common-emitter transistor given in Fig. 5-47(c). Specifically, find I_B , I_C , V_{CE} , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an β_{DC} of 60.
- 5-59 Find the Q-point of the common-emitter transistor given in Fig. 5-47(d). Specifically, find I_B , I_C , V_{CE} , and V_{CB} . Also determine $I_{C(SAT)}$ and $V_{CE(OFF)}$. Indicate the actual conventional current directions on your schematic diagram. The BJT has an β_{DC} of 110.

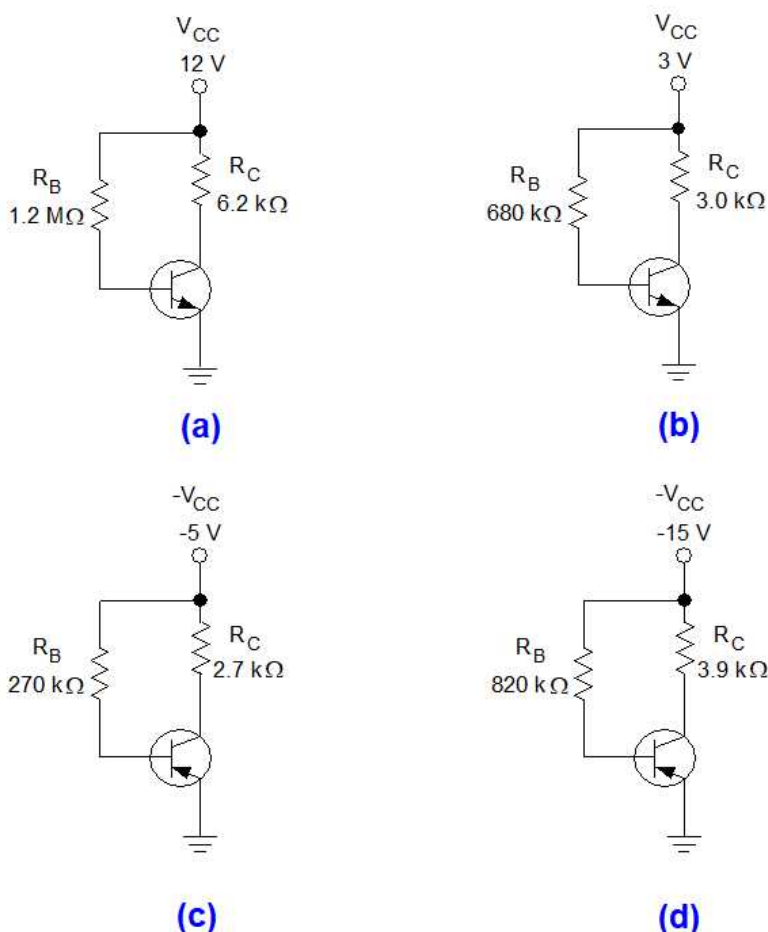


Figure 5-47.

Section 5-9

- 5-60 Explain the purpose of the input and output coupling capacitors found in amplifiers.
- 5-61 Capacitive reactance (X_C) varies _____ (directly, inversely) with frequency.
- 5-62 A common-emitter amplifier has an output voltage of 5 V peak and is shifted 180° with respect to its input voltage. Find its voltage gain (A_v) if its input signal is 40 mV peak.

- 5-63 A common-emitter amplifier has an output voltage of 1 V *peak-to-peak* and is shifted 180° with respect to its input voltage. Find its voltage gain (A_v) if its input signal is 20 mV *peak*.

Section 5-10

- 5-64 Determine the base current (I_B) and the collector saturation current ($I_{C(SAT)}$) for the BJT switch indicated in Fig. 5-48(a). What is the transistor's forced beta β_F ?
- 5-65 Determine the base current (I_B) and the collector saturation current ($I_{C(SAT)}$) for the BJT switch indicated in Fig. 5-48(b). What is the transistor's forced beta β_F ?
- 5-66 Determine the base current (I_B) and the collector saturation current ($I_{C(SAT)}$) for the BJT switch indicated in Fig. 5-48(c). What is the transistor's forced beta β_F ? The BJT is a silicon unit which means V_{BE} is assumed to be 0.7 V. What is the purpose of resistor R_{BE} ?

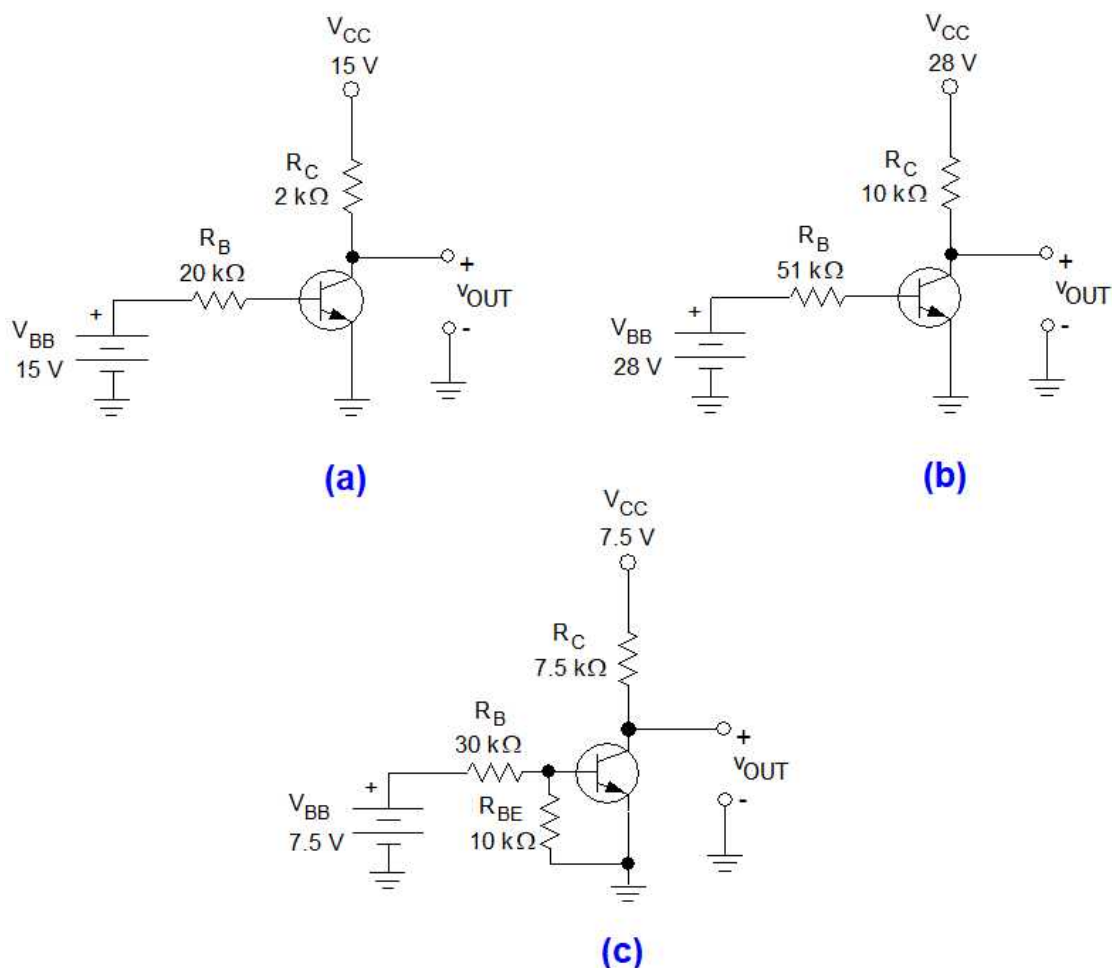


Figure 5-48.

Section 5-11

- 5-67 In general terms, contrast the differences between *analog* and *digital* signals.
- 5-68 In Fig. 5-37(a), assume the base-emitter voltage of the BJT goes from 9 V to 0 V. Determine V_{CB} if V_{CE} goes to 109 V.
- 5-69 Explain the purpose of diode D_I in Fig. 5-38. What is it called?
- 5-70 Refer to Fig. 5-39. If point C is HI, then point B will be _____ (HI, LO). Consequently, point A will be _____ (HI, LO) the LED will be _____ (illuminated, extinguished) and the motor _____ (will, will not) be running.
- 5-71 Refer to Fig. 5-40. If point D is 0.7 V, then point C will be _____ (HI, LO). Consequently, point B will be _____ (HI, LO) point A will be _____ (HI, LO) the LED will be _____ (illuminated, extinguished) and the motor _____ (will, will not) be running.
- 5-72 Name the three fundamental components of a loudspeaker. Explain (briefly) how a loudspeaker converts acoustical energy into electrical energy.

Design Problems

Section 5-8 Designs

- 5-73 The circuit given in Fig. 5-24(a) is to be modified. The supply voltages will remain at $\pm 5V$. However, the quiescent collector current is to be approximately 2 mA. The collector-base voltage is to be approximately $V_{CC}/2$. Determine the required values for R_E and R_C . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.
- 5-74 The circuit given in Fig. 5-24(a) is to be modified. The supply voltages will remain at $\pm 5V$. However, the quiescent collector current is to be approximately 0.25 mA. The collector-base voltage is to be approximately $V_{CC}/2$. Determine the required values for R_E and R_C . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.
- 5-75 The circuit given in Fig. 5-28(a) is to be modified. The supply voltage will remain at 5V. However, the quiescent collector current is to be approximately 0.25 mA. The collector-emitter voltage is to be approximately $V_{CC}/2$. The BJT has a β_{DC} of 150. Determine the required values for R_C and R_B . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.
- 5-76 The circuit given in Fig. 5-28(a) is to be modified. The supply voltage will remain at 5V. However, the quiescent collector current is to be approximately 2.5 mA. The collector-emitter voltage is to be approximately $V_{CC}/2$. The BJT has a β_{DC} of 120. Determine the required values for R_C and R_B . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.

Section 5-10 Designs

- 5-77 The transistor switch in Fig. 5-33(a) is to be modified. The supply voltages will remain at 5 V. The collector saturation current ($I_{C(SAT)}$) is to be approximately 2.5 mA and the forced beta (β_F) is to be 10. Determine the required values for R_C and R_B . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.
- 5-78 The transistor switch in Fig. 5-33(a) is to be modified. The supply voltage will remain at 5 V. The collector saturation current ($I_{C(SAT)}$) is to be approximately 5 mA and the forced beta (β_F) is to be 15. Determine the required values for R_C and R_B . Use an internet search engine or a smart phone app to determine the standard (5%-tolerance) resistor values. Specify the nearest standard value resistors in your design.

Troubleshooting Problems

When verifying the proper operation of transistor switches, jumpers may be used to test out the circuit. A jumper to V_{CC} may be used to force a point HI, while a jumper to ground may be used to force a point LO. Before installing *temporary* jumpers, we must *predict* the effect that a jumper will produce.

- 5-79 The Clapper circuit shown in Fig. 5-43 is non-functional. To check out the DC motor a jumper is to be installed between the collector of transistor Q_4 and ground. When this is done the motor should _____ (run, not run).
- 5-80 If a jumper is installed between the collector of transistor Q_4 and ground in Fig. 5-43, can transistor Q_4 be damaged? Explain. If diode D_1 has failed to become a short circuit, what will happen when the jumper is installed? If the diode is acting like a short, will this prevent the DC motor from running?
- 5-81 If power transistor Q_4 has failed to become a short circuit between its collector and emitter, what will be the condition of the DC motor?
- 5-82 If a jumper is installed between point B and ground in Fig. 5-43, can transistor Q_2 be damaged? Explain. If the circuitry to the right of point B is functioning properly, what will be the condition of the DC motor?
- 5-83 If we want to force point B in Fig. 5-43 HI by using a jumper, the best approach is to (a) tie point B to V_{CC} , or (b) tie the base of transistor Q_2 to ground. Explain your reasoning.

EDA Problems

- 5-84 Use Multisim to produce the family of *common-base output curves* for a 2N2222 *npn* BJT. Let V_{CB} vary from -0.8 V to 20 V in 0.1-V steps. Also let I_E vary from 0 to 10 mA in 1.0-mA steps.
- 5-85 Use Multisim to produce the family of *common-emitter output curves* for a 2N2222 *npn* BJT. Let V_{CE} vary from 0 to 15 V in 0.5-V steps. Also let I_B vary from 0 to 50 μ A in 10- μ A steps.

- 5-86 Use Multisim to verify the DC analysis presented in Example 5-7. Virtual multimeters should be used to display the DC voltages across the BJT and the collector current.
- 5-87 Use Multisim to verify the DC analysis presented in Example 5-8. Virtual multimeters should be used to display the DC voltages across the BJT and the collector current.

6

Field-Effect Transistors

Field-effect devices use an electric field to control the conductivity of a semiconductor. Field-effect transistors (FETs) are *active devices* that can be used as either amplifiers or switches. The first commercially available FETs were the *junction field-effect transistors (JFETs)*. The JFETs (first proposed by Shockley in 1947) were introduced after the BJTs in the 1960s. To circumvent the limitations of JFETs, semiconductor device manufacturers introduced the *metal-oxide semiconductor field-effect transistors (MOSFETs)*. The MOSFETs offered designers improved circuit performance, and even more capabilities. MOSFETs, in turn, were used to create *complementary metal-oxide semiconductor (CMOS)* digital and linear integrated circuits. In fact, the microprocessor owes its existence to this MOSFET technology. MOSFETs have found their way into power electronics in the form of *VMOS*. VMOS power devices are MOSFETs that have a *vertical* channel design. A relatively new power device is the *IGBT*. The IGBT acronym stands for *Insulated Gate Bipolar Transistor*. As its name implies, this device contains both a MOSFET and a BJT in a single package. High-frequency applications such as cellular telephones employ speedy *GASFETs* – *gallium-arsenide field-effect transistors*. With the rapid growth of FET-based devices and technology, we have left the era of the bipolar transistor and are in the MOS technology age. However, we still need to be comfortable with both technologies. To move toward that goal, in this chapter we present:

- The JFET Structure
- Operation of the JFET
- FET Configurations and V - I Curves
- The FET Transfer Equation
- The Depletion-Enhancement MOSFET
- Enhancement MOSFETs
- Finding the Q-Point
- The FET Signal Process and Applying Superposition
- CMOS – The Logical Choice for Linear
- MOSFET Latching Circuit
- Insulated Gate Bipolar Transistors

6-0 Study Objectives

After completing this chapter, you should be able to:

- Describe the basic structure of n -, and p -channel JFETs.

- Identify JFET schematic symbols.
- Explain the role of the JFET's drain, gate, and source terminals.
- Recognize the BJT/FET similarities.
- Identify the common-source, common-drain, and common-gate amplifier configurations.
- Explain the generation and interpretation of the drain, and transfer V - I characteristic curves.
- Use the FET transfer equation to calculate the drain current for a given gate-to-source voltage.
- Describe the operation of n -, and p -channel depletion-enhancement (DE-) MOSFETs
- Describe the operation of n -, and p -channel enhancement (E-) MOSFETs
- Identify the DE- and E-MOSFET schematic symbols.
- Find the Q-point for a fixed gate bias common-source JFET.
- Explain the JFET signal process and describe how a JFET produces voltage amplification.
- Explain the fundamental operation of CMOS.
- Analyze the operation of an E-MOSFET as a switch in a latching circuit.
- Describe the basic nature of IGBTs.

6-1 The JFET Structure

In Fig. 6-1(a) we see the cross section of an ***n-channel JFET***. The JFET structure has two n^+ regions: the ***source*** and the ***drain***. An n^- ***channel*** is doped in to connect the source and drain regions together⁵⁰. A p -type region is doped in above the channel, and the p^- substrate (underlying layer) exists below the channel.

⁵⁰ In case you have forgotten, n^+ indicates an n -type region that is heavily doped. The notation n^- means a n -type region that is doped lightly. You should feel a *minor* twinge of guilt. Next time, you will be eligible for a complete guilt spasm.

N-Channel Junction Field-Effect Transistor (JFET) Structure

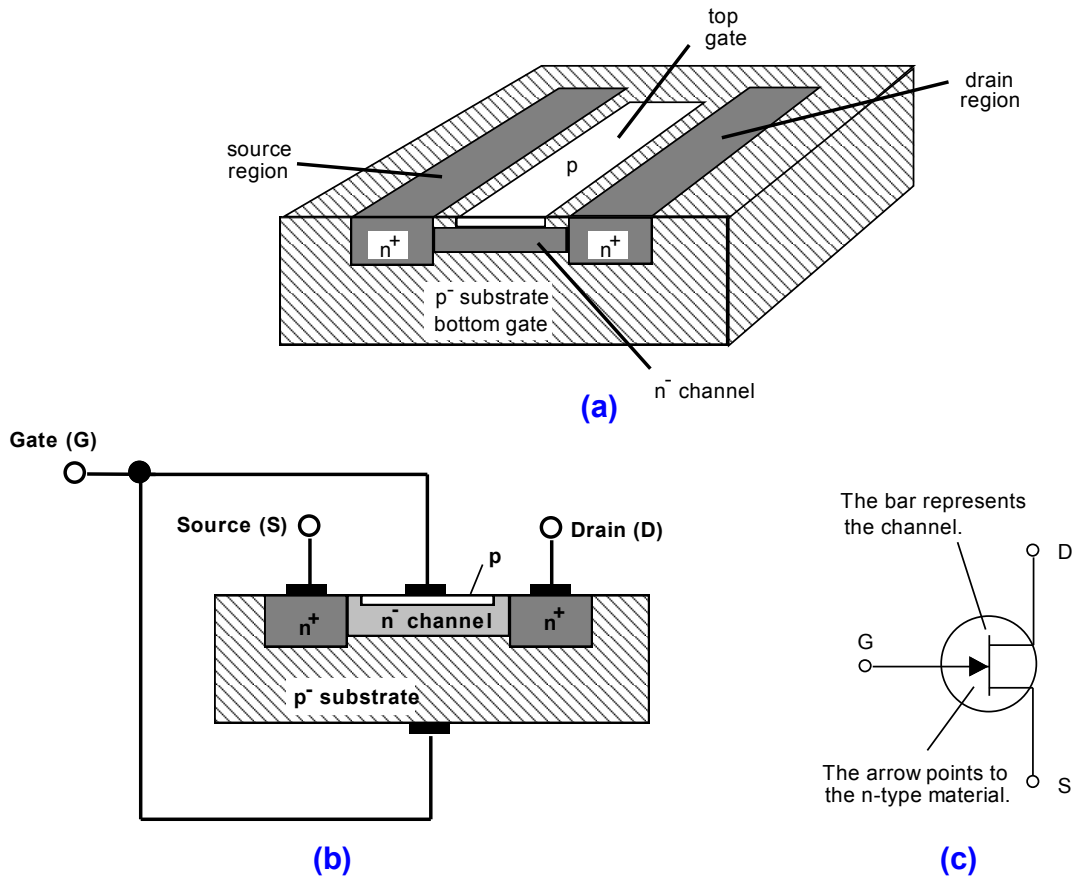


Figure 6-1

A two-dimensional pictorial of the n -channel JFET is shown in Fig. 6-1(b). The p -regions are connected electrically. Its schematic symbol is provided in Fig. 6-1(c). The vertical bar represents the channel, and the arrow (per usual) points to the n -type material. Its complement is the ***p-channel JFET***, whose cross section and schematic symbol are provided in Fig. 6-2(a), and (b), respectively. It is important to note that the JFET's three terminals are called the ***drain***, ***source***, and ***gate***.

P-Channel JFET Structure

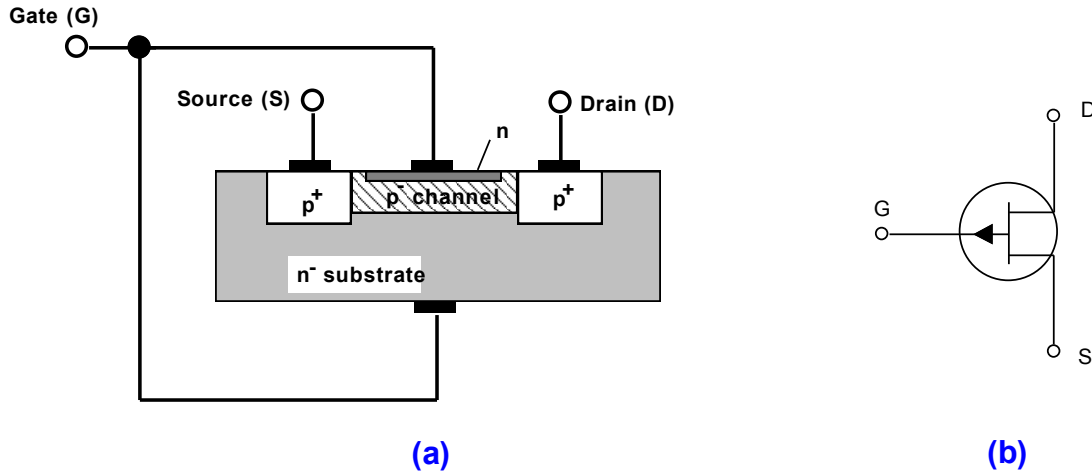


Figure 6-2

The JFET schematic symbols are symmetrical about the gate terminal. This reflects the symmetry in the actual JFET structure. *In fact, it is permissible to exchange the drain and source terminals in a circuit application – without affecting the circuit operation.*⁵¹

Figure 6-3 emphasizes the similarities between the JFET and the BJT. The JFET's drain terminal is very similar to the BJT's collector terminal. The gate is roughly analogous to the BJT's base terminal, and the source terminal is like the emitter terminal of the BJT. These similarities will become apparent as our work progresses. We shall also see that the *n*-channel JFET is like the *npn* BJT. The *p*-channel JFET has much in common with the *pnp* BJT. This is emphasized in Fig. 6-4.

JFETs are Similar to the BJTs

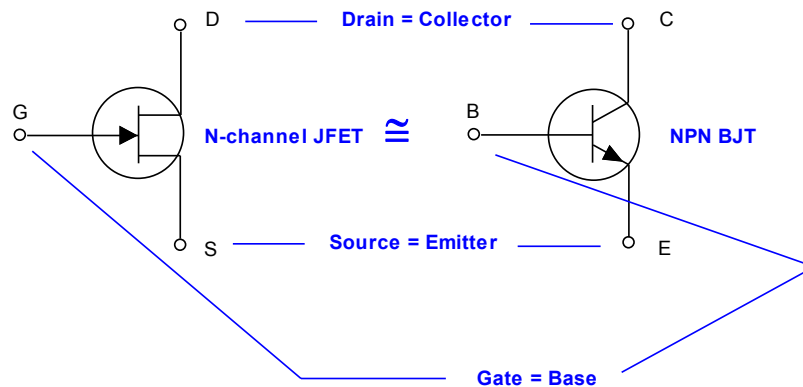


Figure 6-3

⁵¹ This is great news for drowsy lab students - the probability of successful laboratory experiments is improved.

P-Channel JFETs are Similar to PNP BJTs

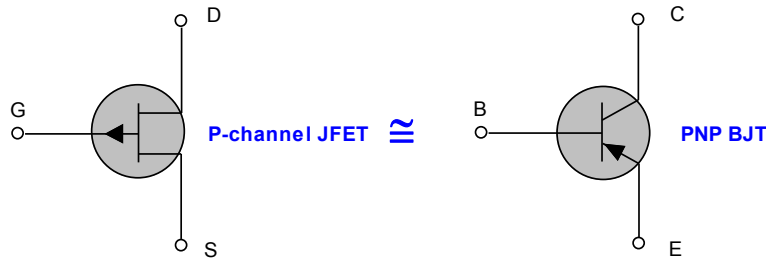


Figure 6-4

The *npn* BJT is generally preferred over the *pnp* BJT because it has better high-frequency performance. (Electrons have greater mobility than holes.) Similarly, the *n*-channel JFET is generally preferred over the *p*-channel JFET for the same reason. Consequently, we shall focus our discussion on the *n*-channel JFET. The thrust of our explanations may be extended to the *p*-channel device.

6-2 Operation of the JFET

As with any *p-n* junction, a depletion region forms at the interface. This is indicated in Fig. 6-5. The depletion region extends deeply into the lightly doped n^- channel and the p^- substrate. Subsequently, the depletion region penetrates only slightly into the heavily doped n^+ drain and source regions.

JFET Depletion Regions

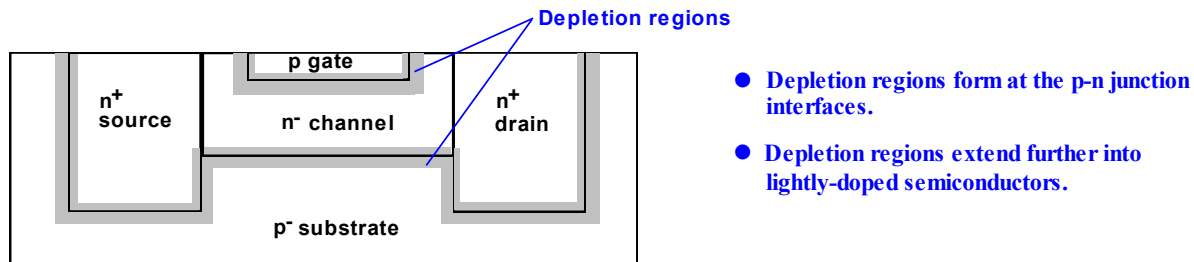


Figure 6-5

In Fig. 6-6, we see the source and the gate terminals have been tied to ground. An adjustable voltage source has been connected between the drain and ground. Its value will determine the drain-to-source voltage V_{DS} . Because the gate terminal has been tied directly to ground, V_{GS} will be zero volts.

Since the n^+ drain is positive and the (*p*-type) gate regions are tied to ground, the *p-n* junctions in the drain region are reverse-biased. The drain region in Fig. 6-6 has been enlarged to indicate this. For small to moderate values of V_{DS} , the reverse bias causes the depletion regions to widen as shown in Fig. 6-6. With the biasing shown in Fig. 6-6, electrons will enter the channel through the source terminal (S). The electrons will then flow through the channel and leave the JFET via the drain terminal (D). This too has been noted in Fig. 6-6.

JFET Depletion Regions and the Application of a Drain-to-Source Voltage

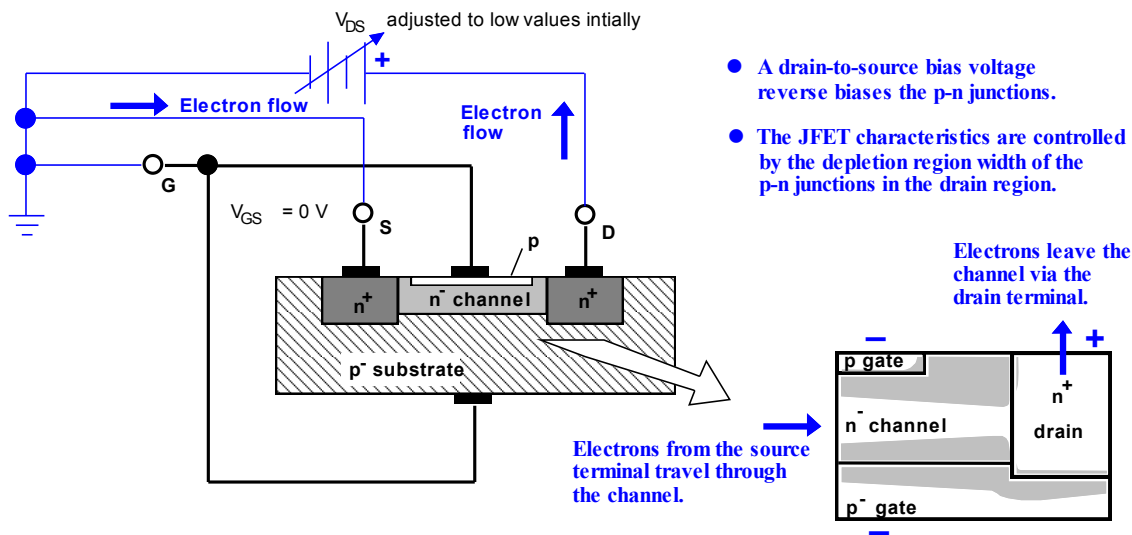


Figure 6-6

The JFET channel has a resistance, which can be expressed by the familiar resistance formula $R = \rho L/A$, where ρ is the resistivity in ohm-meters, L is the length in meters, and A is the cross-sectional area in meters². The channel can be dimensioned as shown in Fig. 6-7. It has a width W , a length L , and a thickness T . (The product WT produces the channel's cross-sectional area A .) **While the channel's length and width are constants, its thickness depends on the depletion region widths.** The channel's resistance R can be expressed in terms of the channel dimensions.

$$R = \rho_{\text{channel}} \frac{L}{A} = \rho_{\text{channel}} \frac{L}{WT} \quad (6-1)$$

The resistivity of the channel is given by ρ_{channel} . (The Greek letter ρ is called rho.) The resistivity is a function of the channel's doping level. For low-to-moderate values of V_{DS} , the channel thickness T , and therefore its resistance, are essentially *constant*. This is summarized in Fig. 6-8.

JFET Channel Dimensions

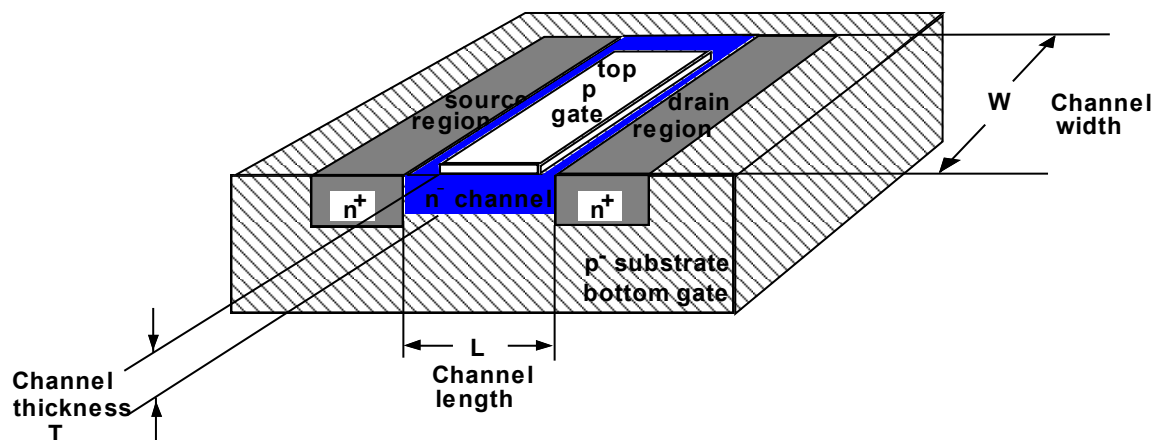
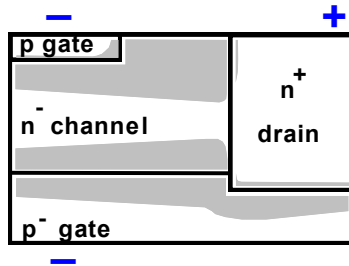


Figure 6-7.

JFET Channel Dimensions are Reasonably Constant at Low Values of Drain-to-Source Voltage



- The depletion region controls the channel thickness T .
- At low values of drain-to-source voltage, T is almost constant.
- This means the JFET resistance is essentially constant.
- This gives the JFET its linear, or ohmic, region of operation

Figure 6-8.

Figure 6-9 depicts a JFET's *drain characteristic curve*. The drain current I_D is placed on the vertical axis and the drain-to-source voltage V_{DS} lies on the horizontal axis. The gate-to-source voltage is the parameter. In this case, V_{GS} is zero [refer to Fig. 6-6]. At low values of V_{DS} , the V - I curve is linear as indicated in Fig. 6-9(a). This is called the **ohmic region**. As V_{DS} is increased, the depletion regions continue to widen. Ultimately, the depletion regions begin to touch. At this point, the V - I curve becomes non-linear, as shown in Fig. 6-9(b). Specifically, the dynamic resistance of the channel begins to increase. (This means the V - I curve is becoming *horizontal*.) We also see the JFET is entering its **constant-current region of operation**. This is called **pinch-off**. *A JFET in pinch-off is in its active (amplifying) region of operation.*

Drain V-I Characteristics

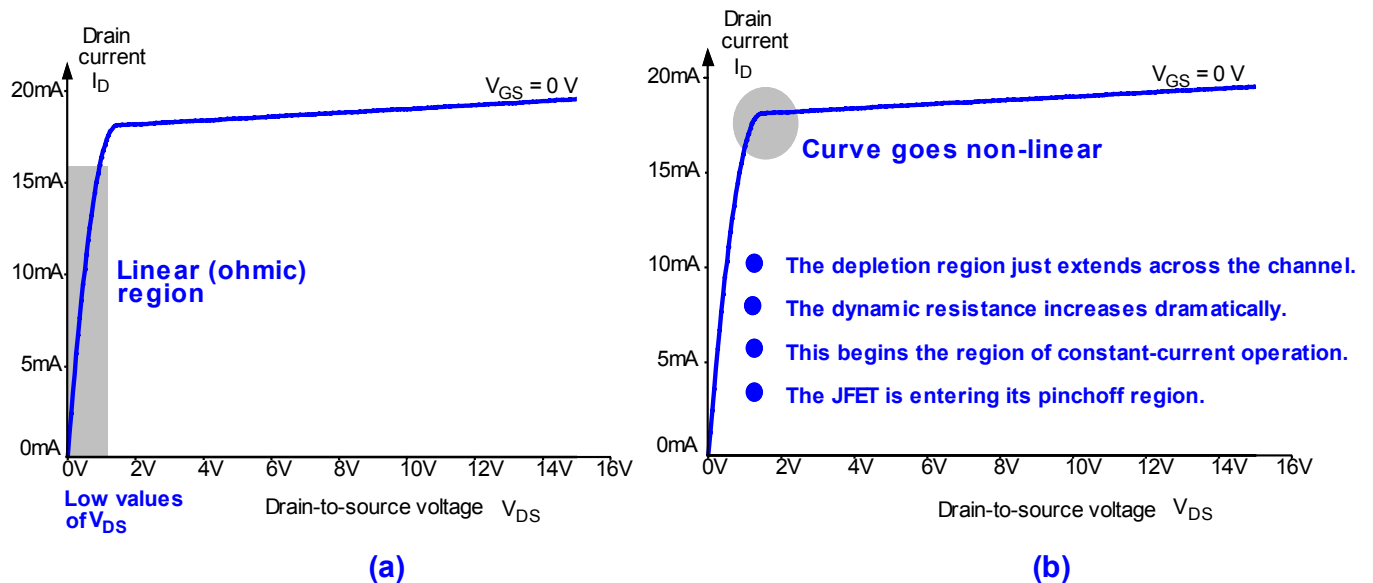


Figure 6-9.

In Fig. 6-10(a), we see that high-energy (conduction-band) electrons from the source region are swept across the depletion region to form drain current. When V_{GS} is equal to zero, and the JFET enters pinch-off, the corresponding drain current is called the **drain-to-source saturation current** I_{DSS} .

The required drain-to-source voltage required to place the JFET in pinch-off is called (appropriately) the **pinch-off voltage** V_P . The drain current is essentially constant when the JFET is in pinch-off. This occurs because there are a fixed number of available charge carriers within the channel, and they have a limited mobility. Consequently, the JFET is also described as being in its **saturation region** of operation. *This should not be confused with the “saturation” that can occur in an amplifier circuit, or a switch.*

The JFET in Pinchoff

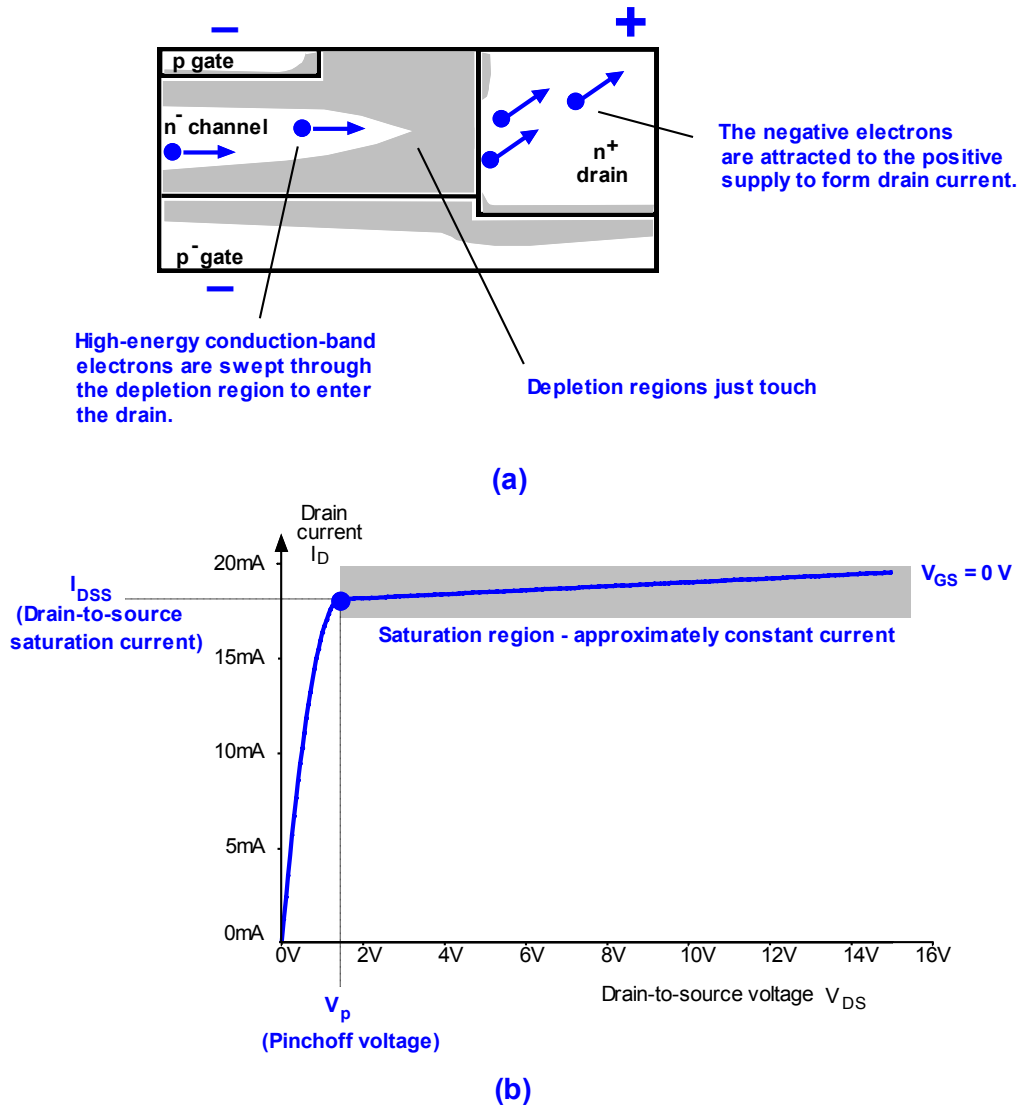


Figure 6-10.

The Effects Produced by a Negative V_{GS}

In Fig. 6-11(a), we see that the gate-to-source voltage V_{GS} has been biased to a negative voltage. This serves to reverse bias the $p-n$ junctions between the gate and the channel. The $p-n$ junctions between the gate and the drain, and the gate and the source regions are also reverse-biased. This

widens the depletion regions along the channel as illustrated in Fig. 6-11(b). Consequently, the thickness T will be reduced.

Effects of a Negative Gate-to-Source Bias Voltage

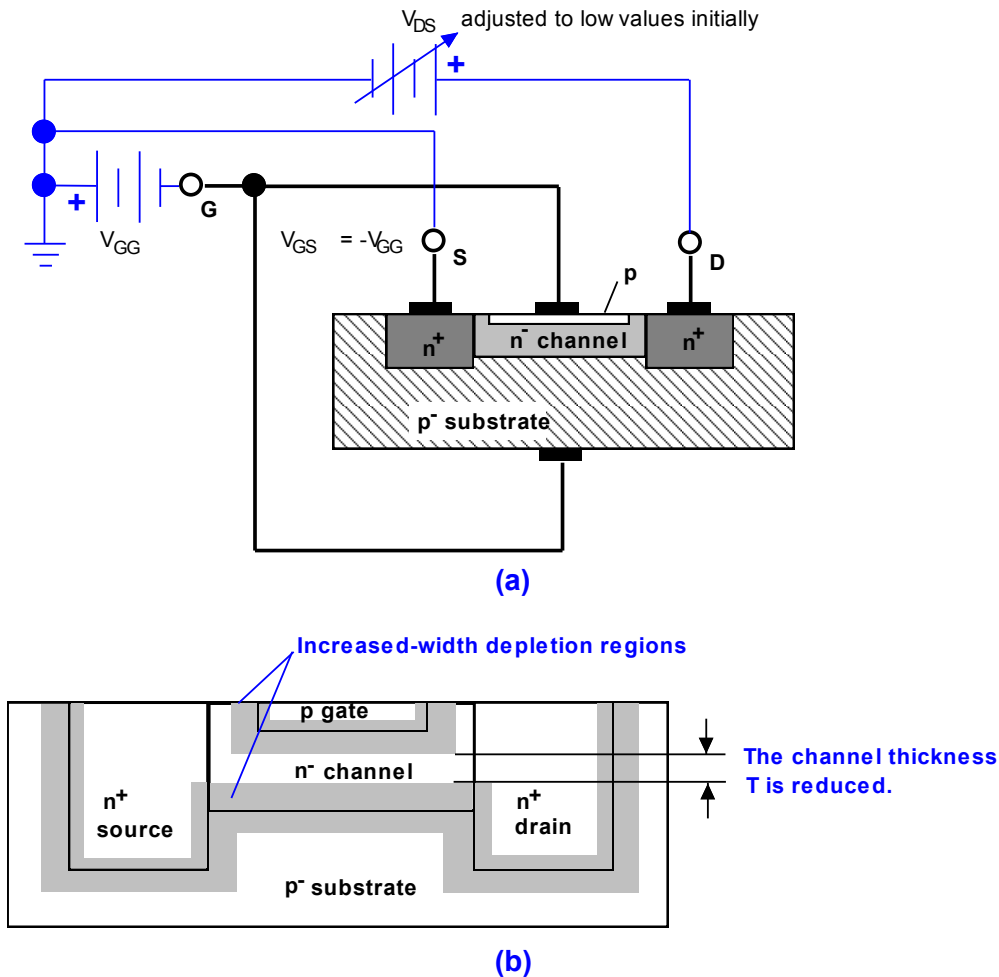
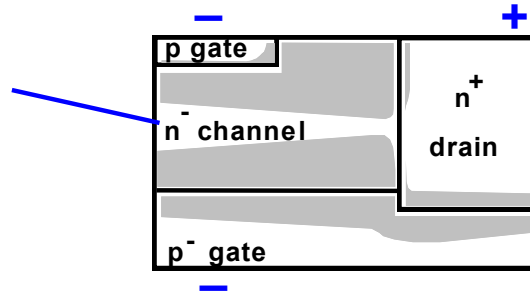


Figure 6-11.

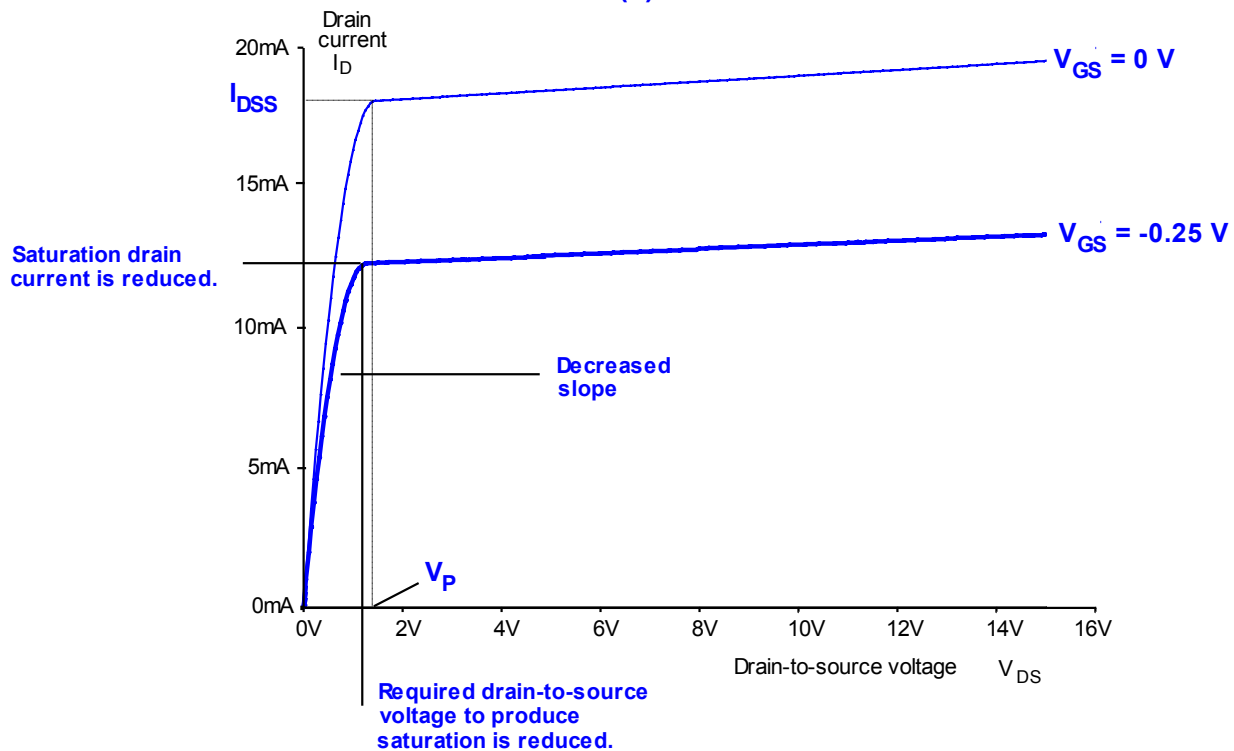
By inspection of Eq. 6-1, we can see that a *reduction* in T will *increase* the channel resistance R . Therefore, for low-to-moderate values of V_{DS} , the depletion regions will widen as indicated in Fig. 6-12(a). The increase in the channel resistance will produce the V - I curve with the slope shown in Fig. 6-12(b). The curve we developed when V_{GS} was zero volts has been included for reference.

Effects of a Negative Gate-to-Source Bias Voltage (continued)

- The narrower channel has a larger resistance, which means a smaller drain current for the same drain-to-source voltage.
- The narrower channel means there are less available charge carriers, which means the drain saturation current will be smaller.



(a)



(b)

Figure 6-12.

As V_{DS} is increased further, the depletion regions will continue to widen until the channel will again become pinched off. As Fig. 6-12(b) shows, once the JFET enters pinch-off (saturation), the drain current will become reasonably constant. The actual value of V_{DS} required to pinch off the channel is reduced from the value that was necessary when V_{GS} was zero volts. This has been indicated in Fig. 6-12(b). This occurs because of the reduced channel thickness produced by the negative value of V_{GS} . This is described in Fig. 6-13.

The Effect of a Negative Gate-to-Source Voltage on JFET Pinchoff

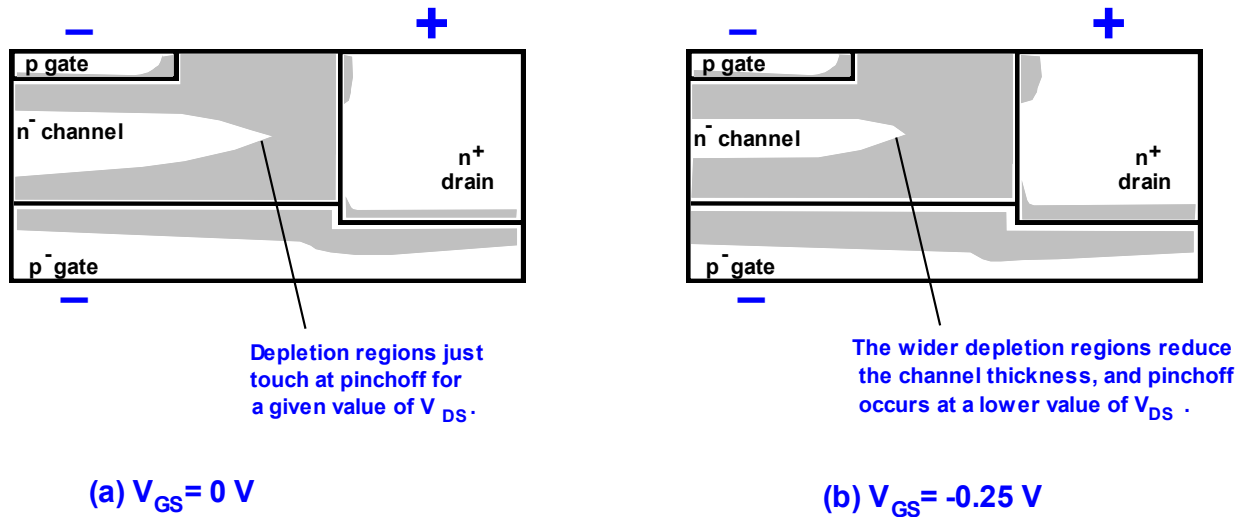
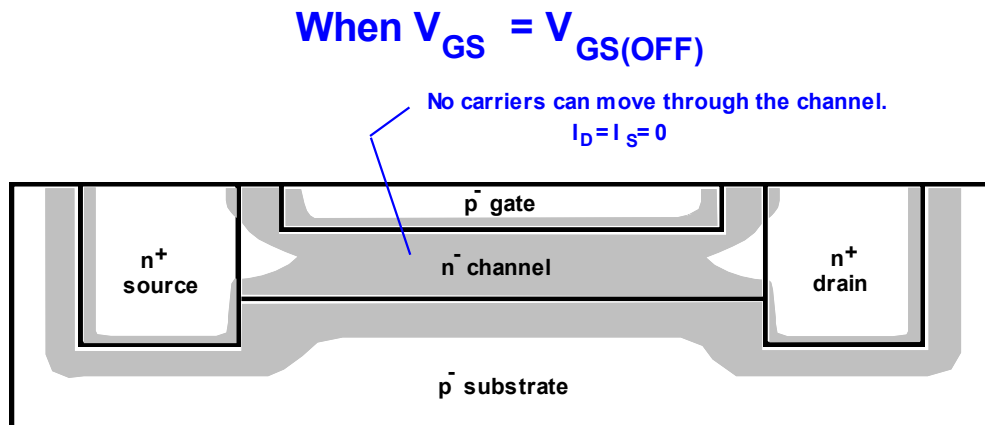


Figure 6-13.

If the magnitude of V_{GS} is increased to a value termed $V_{GS(OFF)}$, the depletion region widths will extend across the channel, as shown in Fig. 6-14. The channel will be devoid of charge carriers. Consequently, carrier movement through the channel will be blocked, and the drain and source currents will be reduced to approximately zero. Under this condition, the JFET is in *cutoff*. The JFET acts like an open switch when it is in cutoff. (This is just like the BJT!)



- The gate-to-source bias voltage is equal to $V_{GS(OFF)}$.
- The depletion regions widen to extend across the channel.
- No charge carriers will exist in the channel, which means the drain and source terminal currents will be zero.
- The JFET is in its cutoff region of operation.

Figure 6-14.

At this point, we can begin to describe the operation of the JFET more quantitatively. First, **since the gate-channel p-n junction is reverse-biased, this means the gate current must be nearly zero**. The charge carriers flow from the source region to the drain region through the channel. Obviously, **the drain current I_D must be equal to the source current I_S** . This relationship is given by Eq. 6-2.

$$I_D = I_S \quad (6-2)$$

The **magnitude of the gate-to-source cutoff voltage $V_{GS(OFF)}$ will be equal to the magnitude of the pinch-off voltage V_P** . This is stated by Eq. 6-3.

$$|V_{GS(OFF)}| = |V_P| \quad (6-3)$$

A JFET enters its pinch-off (constant-current) region of operation when its drain-to-gate voltage is equal to V_P . This is described in Fig. 6-15. Note that V_P is defined between the JFET's drain and gate terminals. We apply Kirchhoff's voltage law around the JFET. We start at the drain terminal and work our way around the JFET in a clockwise fashion.

$$V_{DS} - V_{GS} - V_P = 0$$

We solve for V_{DS} to obtain Eq. 6-4.

$$V_{DS} = V_P + V_{GS} \quad (6-4)$$

Equation 6-4 provides us with the value of V_{DS} required to place a given JFET in its constant-current region of operation. Note that for an n-channel JFET, V_{GS} tends to be *negative* values. The drain characteristic V - I curves are given in Fig. 6-16. The relationships defined by Eqs. 6-3 and 6-4 have been indicated in the figure.

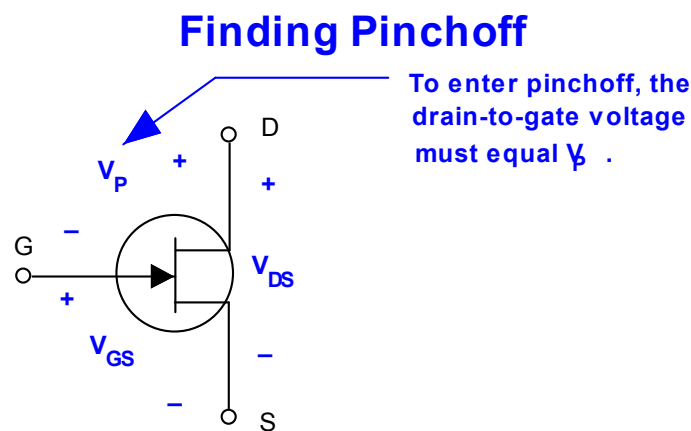


Figure 6-15.

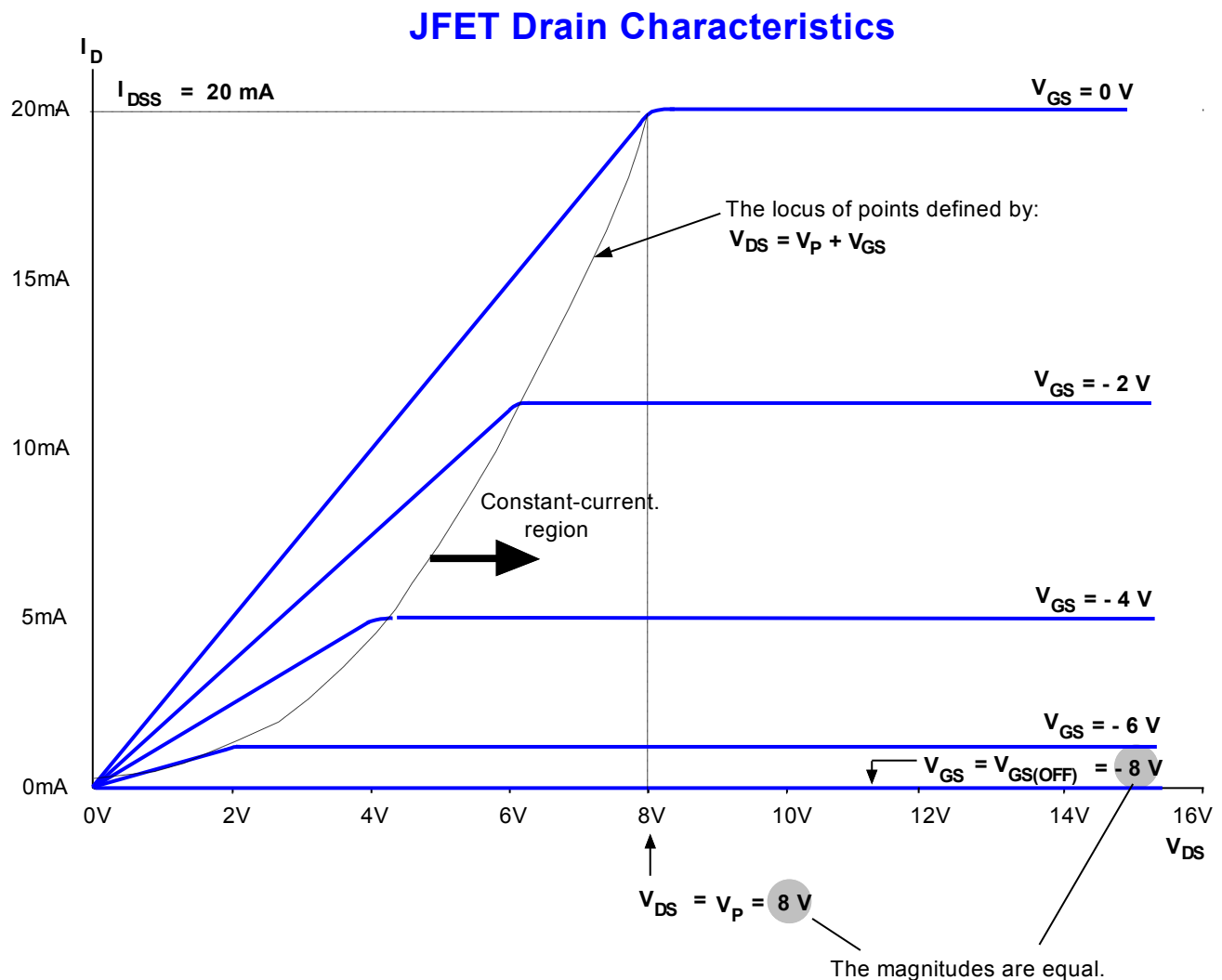


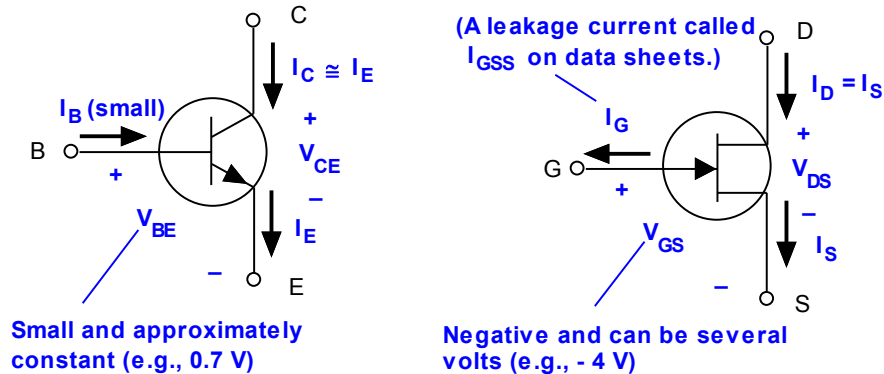
Figure 6-16.

Comparing the JFET to the BJT

The JFET is very similar to the BJT. The collector current of a BJT is almost equal to its emitter current. The drain current of a JFET is essentially the same as its source current. The BJT's base-emitter voltage controls its collector current. The JFET's gate-source voltage controls its drain current. A more detailed comparison is provided in Fig. 6-17. Conventional current directions have been indicated. Study it closely.

The BJT and the JFET Comparison

(Conventional current directions have been indicated.)



- A BJT can be thought of as a current-controlled or a voltage-controlled current source.
- The 0.7-V approximation of the base-emitter voltage simplifies analysis greatly.
- A JFET can only be thought of as a voltage-controlled current source.
- The large values of gate-source voltage complicate JFET analysis. No simple approximation exists.

Figure 6-17.

Example 6-1. An n -channel JFET has an I_{DSS} of 20 mA and a $V_{GS(OFF)}$ of -8 V. Assume that it is in pinch-off. What is its I_S when V_{GS} is zero volts? What is its pinch-off voltage V_P ? What is the *minimum* value of V_{DS} required to saturate the JFET if V_{GS} is -2 V?

Solution: The drain characteristics for this JFET are illustrated in Fig. 6-16. When a JFET is in *pinch-off*, it is also described as being *saturated*. The JFET is in its constant-current region of operation. When $V_{GS} = 0$ V, $I_D = I_{DSS} = 20$ mA, and Eq. 6-2 gives us the source current I_S .

$$I_S = I_D = 20 \text{ mA}$$

Generally, JFET device manufacturers provide $V_{GS(OFF)}$ on their data sheets. They expect *us* to know that the magnitude of $V_{GS(OFF)}$ is equal to the magnitude of the pinch-off voltage V_P . (This relationship is given by Eq. 6-3.)

$$\begin{aligned} |V_{GS(OFF)}| &= |V_P| \\ V_P &= |V_{GS(OFF)}| = |-8 \text{ V}| = 8 \text{ V} \end{aligned}$$

The minimum value of V_{DS} required to saturate the JFET for a V_{GS} of -2 V is provided by Eq. 6-4.

$$V_{DS} = V_P + V_{GS} = 8 \text{ V} + (-2 \text{ V}) = 8 \text{ V} - 2 \text{ V} = 6 \text{ V}$$

This result is shown in Fig. 6-16.

6-3 FET Configurations and V-/ Curves

Just as we saw that the BJT has three basic configurations, the same is true for the FETs (JFETs and MOSFETs). The **common-source**, **common drain**, and **common-gate** configurations have been given in Fig. 6-18. As with the BJT, the surest method for ascertaining the configuration is to determine the FET's signal input and output terminals with respect to ground. To assist us in our efforts, we have developed Table 6-1.

The three FET configurations have characteristics that are like the three corresponding BJT configurations. Therefore, we have also indicated the BJT-FET correspondence in Table 6-1. (The reader should study Table 6-1 carefully. It will assist us in our later work.)

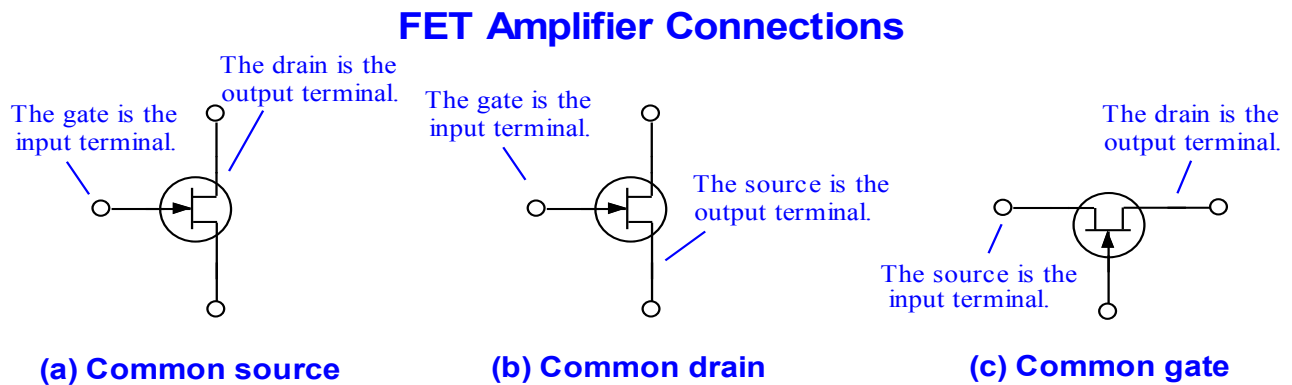


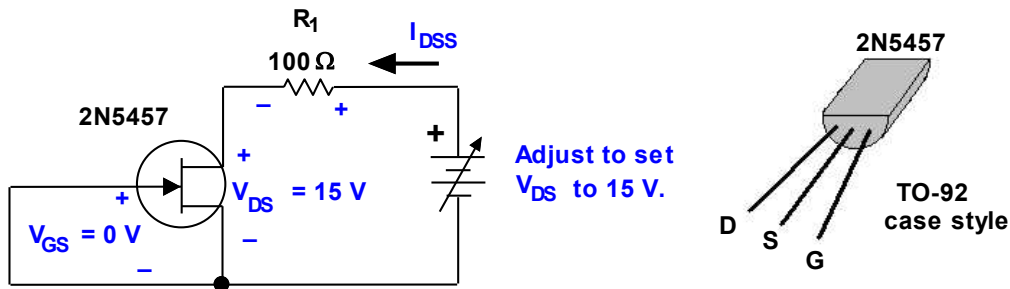
Figure 6-18.

Table 6-1. FET - BJT Configurations

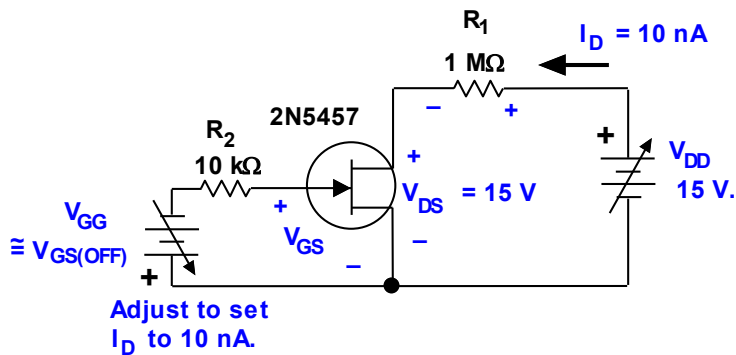
FET Configurations			Corresponding BJT Configurations		
Connection	Input Terminal	Output Terminal	Connection	Input Terminal	Output Terminal
Common Source	Gate	Drain	Common Emitter	Base	Collector
Common Drain	Gate	Source	Common Collector	Base	Emitter
Common Gate	Source	Drain	Common Base	Emitter	Collector

The common-emitter connection is the most popular choice for the BJT. Similarly, the common-source connection is the favored FET configuration. A simple test circuit for measuring I_{DSS} is given in Fig. 6-19(a). Resistor R_I is used to sense (measure) the drain current. The gate is shorted to the source to make $V_{GS} = 0$ V. The TO-92 package case style for the 2N5457 has also been indicated for ambitious students that may wish to construct the circuit. Figure 6-19(b) shows the test circuit to measure $V_{GS(OFF)}$. In theory, I_D is equal to zero when V_{GS} is set to $V_{GS(OFF)}$. In practice, a low current level of 10 nA with a V_{DS} of 15 V is used to establish the value of $V_{GS(OFF)}$. Notice that a large (1-M Ω) resistor is used to sense the very small drain current. The 10-k Ω resistor in series with the gate is to protect the JFET in the event the gate bias supply V_{GG} is accidentally reversed. (The gate-channel p - n junction would be *forward biased* in this event, and the gate is not designed to handle currents beyond 10 mA.) Also observe that the JFET's drain supply is labeled V_{DD} .

JFET Test Circuits



(a) The I_{DSS} test circuit.

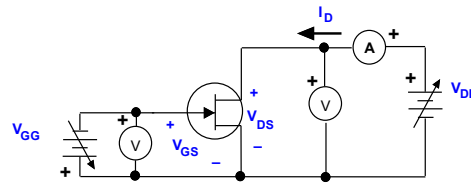


(b) The $V_{GS(OFF)}$ test circuit.

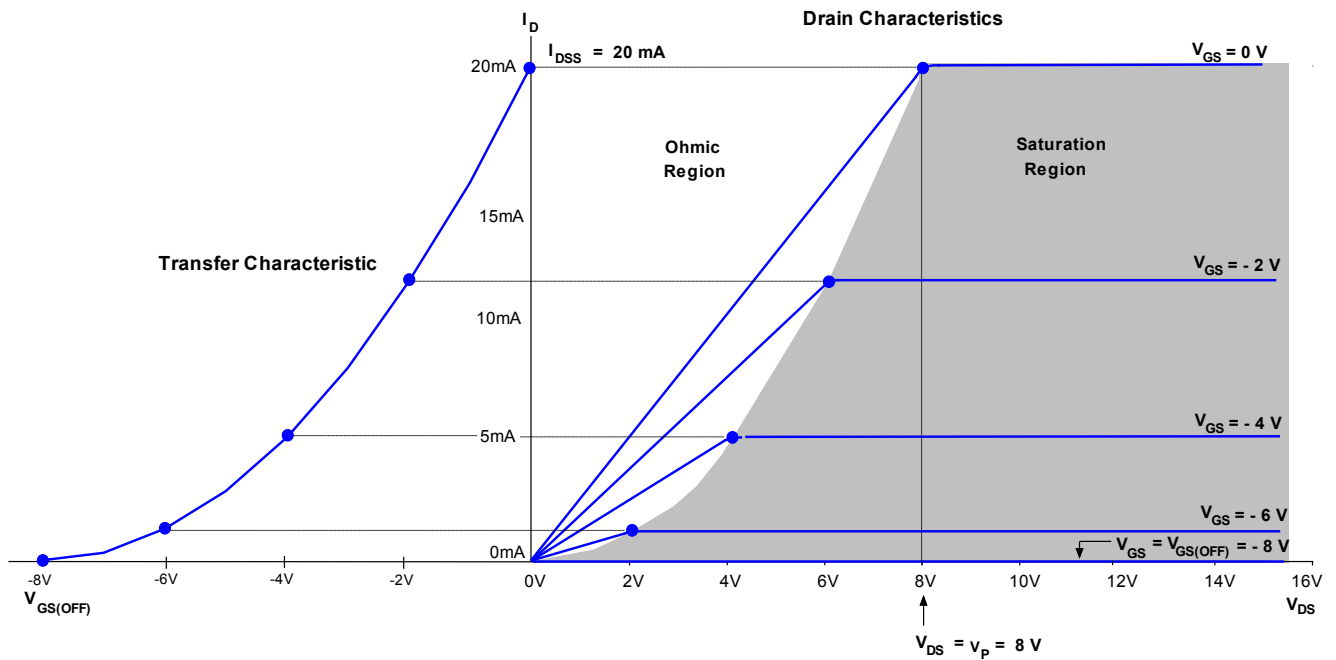
Figure 6-19.

The transistor convention also applies to FETs. This means that *conventional currents that flow into the FET are called positive, while currents that leave the FET are labeled negative.* A simple static test circuit for generating the common-source drain characteristics, and the common-source transfer characteristics is depicted in Fig. 6-20. The *transfer characteristics* show how the gate-source voltage controls the drain current.

JFET Common-Source V-I Curves



(a) The static test circuit.



(b) The V-I curves.

Figure 6-20.

While the circuit in Fig. 6-20(a) can be used to develop the V - I curves point-by-point, it is more efficient to generate them dynamically. A circuit that can be used to produce the common-source drain characteristics is provided in Fig. 6-21. The transformer serves as a floating AC voltage source⁵⁰. The diode half-wave rectifier drives the drain-source circuit with a positive pulsating DC voltage. The drain current is sensed via resistor R_I . This is connected to the oscilloscope's (inverted) vertical input. The oscilloscope's horizontal input is used to monitor the corresponding drain-source voltage. The gate DC supply V_{GG} is used to set convenient values of negative gate-source voltage. The drain characteristics are displayed on the oscilloscope. It is convenient to plug the transformer's primary into an autotransformer (which is an adjustable transformer). This provides an easy way to adjust the maximum values of the drain-source voltage. Resistor R_2 serves to protect the gate. If V_{GG} is accidentally reversed, the gate-channel p - n junction will be forward biased. R_2 is used to limit the maximum gate current to a safe value.

⁵⁰ A **floating input terminal** is not connected to anything. A **floating source** is not connected to ground.

A Test Circuit to Develop Common-Source Drain Curves Dynamically

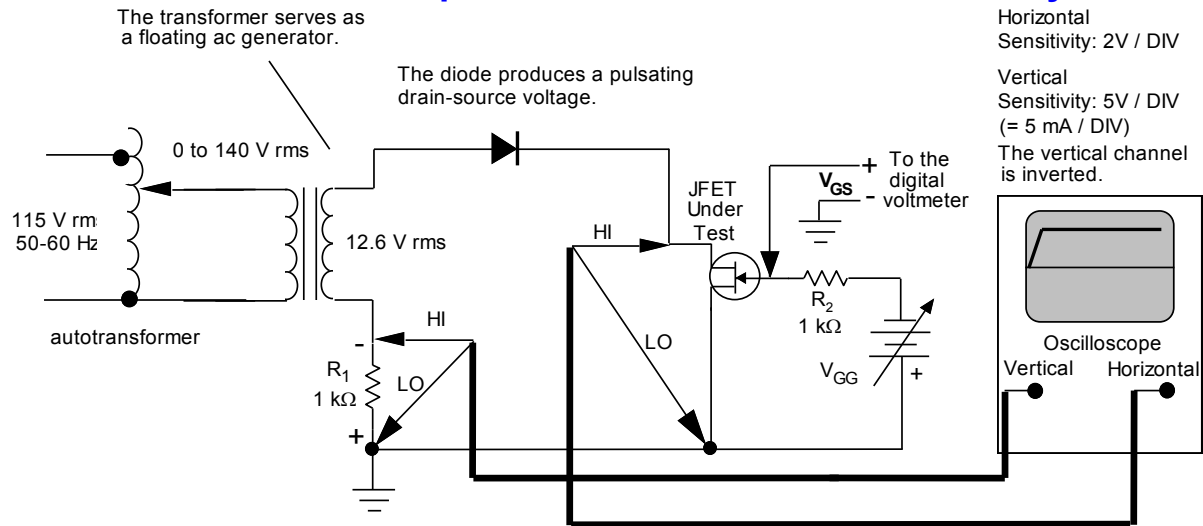


Figure 6-21.

A similar circuit can be used to produce the JFET's *transfer characteristic curve*. The test circuit is provided in Fig. 6-22. In this case, the diode rectifier is used to provide *negative* DC pulses to the gate-source circuit. The gate-to-source voltage is applied to the oscilloscope's horizontal input. Resistor R_2 is used to protect the gate from excessive current that will result from accidental forward bias. Resistor R_3 is used to pull the gate to ground when the diode is non-conducting. If resistor R_3 is omitted, the gate will build up a negative charge. Typically, this will move the JFET's operation to its cutoff region.⁵¹ The DC drain supply V_{DD} is floating. (This means it is not referenced to earth ground.) Resistor R_1 is used to sense the drain current. The voltage across it provides us with an indication of the drain current. Again, because the drain current flows *up* through resistor R_1 , it is necessary to invert the vertical channel used to measure the voltage across it. By using the autotransformer to adjust the transformer's primary voltage, the maximum negative value of the gate-to-source voltage can be adjusted.

⁵¹ In layman's terms, resistor R_3 permits the circuit to work. Without it, the circuit will not perform properly.

A Test Circuit to Develop Common-Source Transfer Curves Dynamically

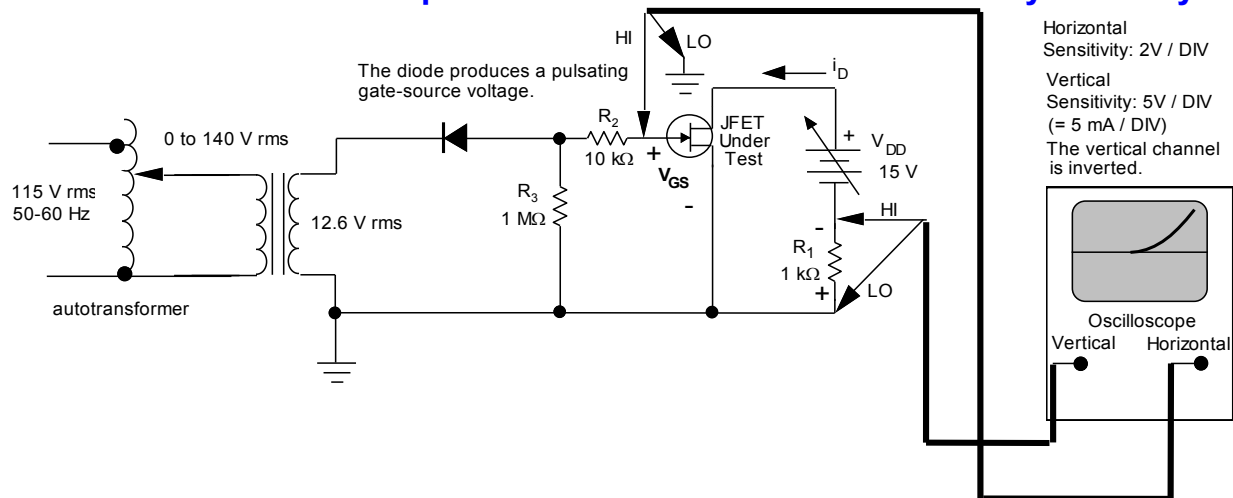


Figure 6-22.

Using EDA to Produce Drain Characteristics

By employing a nested DC sweep, Multisim can be used to produce the drain characteristics for a 2N5484 *n*-channel JFET. The model for this device is in **Transistor** → **JFET_N library** as shown in Fig. 6-23(a). The default parameters for the model of this JFET device include a $V_{GS(OFF)}$ of -1.278 V, and an I_{DSS} of about 3.53 mA. The schematic is shown in Fig. 6-23(b). The JFET schematic symbol used by Multisim is another valid version according to the standard (ANSI Y32.2)⁵² that governs electrical schematic symbols. To monitor the drain current we must attach a **current probe** which is also detailed in Fig. 6-23(b). The source labeled V_{DS} serves as the drain supply while the source V_{GS} is used to set the gate-to-source voltage.

⁵² ANSI is the American National Standards Institute which provides national, regional, and international standards. In this case, we look to ANSI Y32.2 to find the acceptable symbols for electrical and electronic devices.

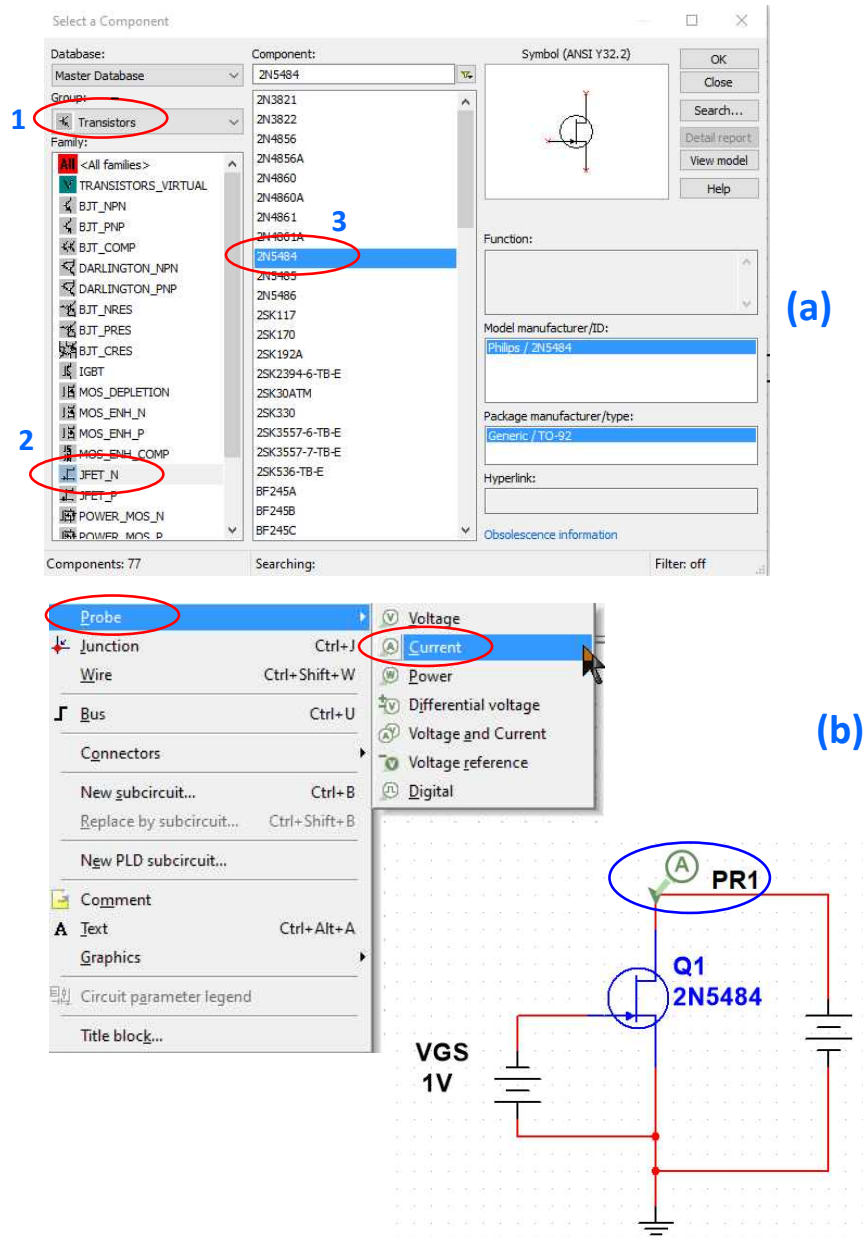


Figure 6-23.

Figure 6-23(c) shows us how to set up the nested DC sweep. Click on **Simulate** and then select **DC Sweep**. The drain-to-source voltage is swept from 0 to 15 V in steps of 0.5 V. The gate-to-source voltage is the parameter. It is swept from 0 to 1 V in steps of 0.25 V. The V_{GS} source is upside down to establish negative values of V_{GS} . Subsequently, a drain curve for V_{GS} values of 0, -0.25, -0.50, -0.75, and -1V will be produced. We want the drain current to be on the vertical axis. Figure 6-23(d) shows how to accomplish this. The current probe [IPR1]] is selected as the output variable.

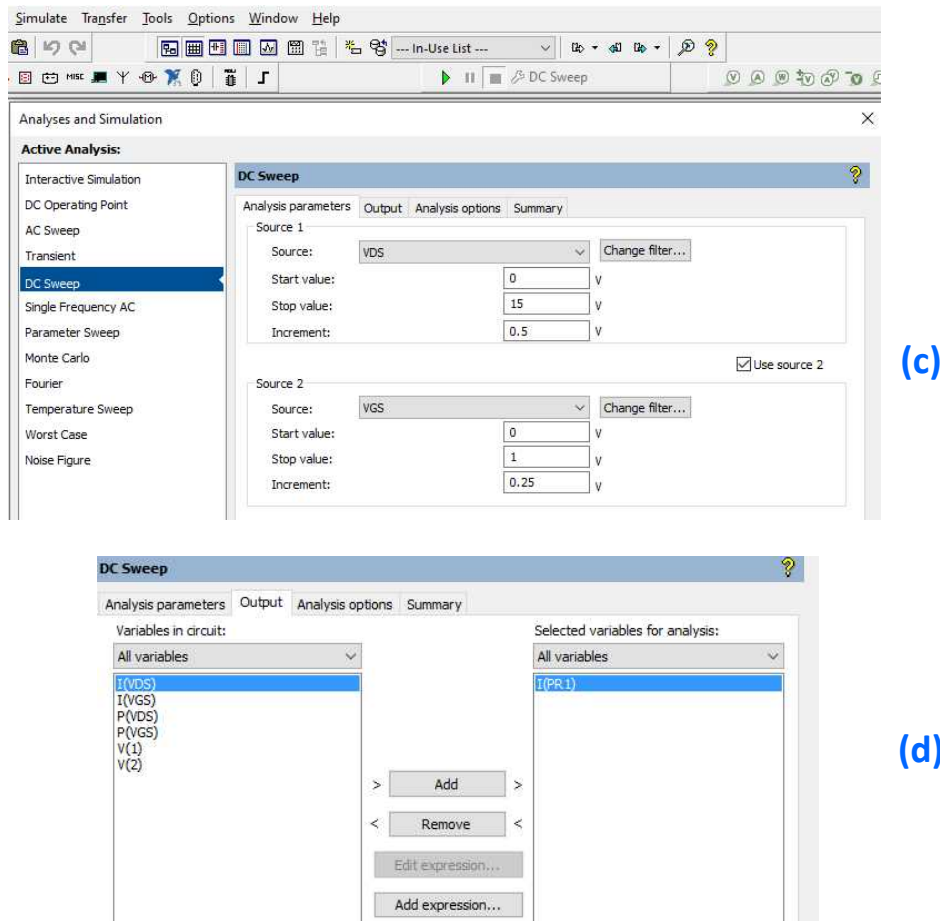
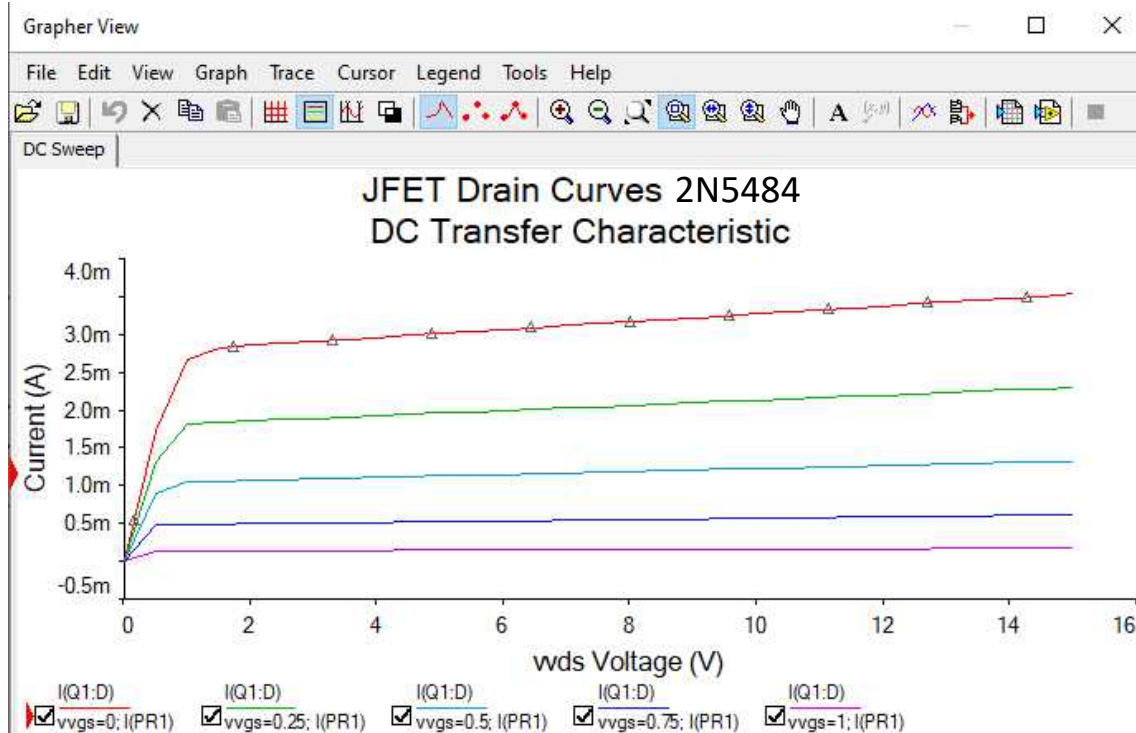


Figure 6-23 (continued).

We click on the **green arrow or Run** to generate the drain characteristics as shown in Fig. 6-23(e). The top red curve is produced when V_{GS} is held at 0 V. The green curve below it is generated with V_{GS} is held at -0.25 V. The legend defined along the bottom defines the V_{GS} values and the color of the corresponding curve.



(e)

Figure 6-23 (continued).

The advantage of being able to produce the drain characteristics using Multisim needs to be made clear. It provides us with insight, and a knowledge of the parameters employed in the library model. Generally, EDA tools are used to characterize circuit and system responses. The underlying assumption is the EDA user understands the device models, and the limitations inherent in any simulation. Being able to generate the V - I characteristics for a device model is one way of being able to better understand the employed model. We do *not* normally generate V - I curves.

6-4 The FET Transfer Equation

The FET is often described as being *a square-law device*. This characteristic gives the FET advantages over the BJT in some situations. We will not concern ourselves with these at this point. However, by referring to the FET as a square-law device, we mean that its drain current I_D is controlled by the square of its gate-to-source voltage V_{GS} . This is embodied in *the FET transfer equation*.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 \quad (6-5)$$

Equation 6-5⁵³ can be used to generate the transfer characteristic shown in Fig. 6-20(b). *This equation applies to the FET when it is in its constant-current (pinch-off or saturation) region of operation.* This is suggested in Fig. 6-20(b) by the dashed lines that project from the drain characteristic to the transfer characteristic.

Example 6-2. An n -channel JFET has an I_{DSS} of 12 mA and a $V_{GS(OFF)}$ of -6 V. Assume that it is in pinch-off. Make a sketch of its transfer characteristic curve.

Solution: Using the given parameters and Eq. 6-5, allows us to produce the transfer characteristic. We shall use V_{GS} values that range from 0 to -6 V in -1 -V steps. If $V_{GS} = 0$, we obtain the result below:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 = (12 \text{ mA}) \left[1 - \frac{0 \text{ V}}{-6 \text{ V}} \right]^2 = 12 \text{ mA}$$

This should make sense. If V_{GS} is equal to zero, the drain current I_D should be equal to I_{DSS} . Next, we let $V_{GS} = -1$ V.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 = (12 \text{ mA}) \left[1 - \frac{-1 \text{ V}}{-6 \text{ V}} \right]^2 = (12 \text{ mA}) [1 - 0.166667]^2 = 8.33 \text{ mA}$$

Other values of I_D are computed in a similar fashion. It is important to note that for $V_{GS} = V_{GS(OFF)} = -6$ V, we obtain an I_D of zero. The results of this example are presented in Fig. 6-24.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 = (12 \text{ mA}) \left[1 - \frac{-6 \text{ V}}{-6 \text{ V}} \right]^2 = (12 \text{ mA}) [0]^2 = 0 \text{ mA}$$

⁵³ Equation 6-5 applies to both the JFET and the Depletion Enhancement Metal Oxide Field Effect Transistor (DE-MOSFET) as is demonstrated in Section 6-7.

The JFET Transfer Characteristics Developed in Example 5-2

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2$$

V_{GS} (V)	I_D (mA)
0	12
-1	8.33
-2	5.33
-3	3.00
-4	1.33
-5	0.33
-6	0

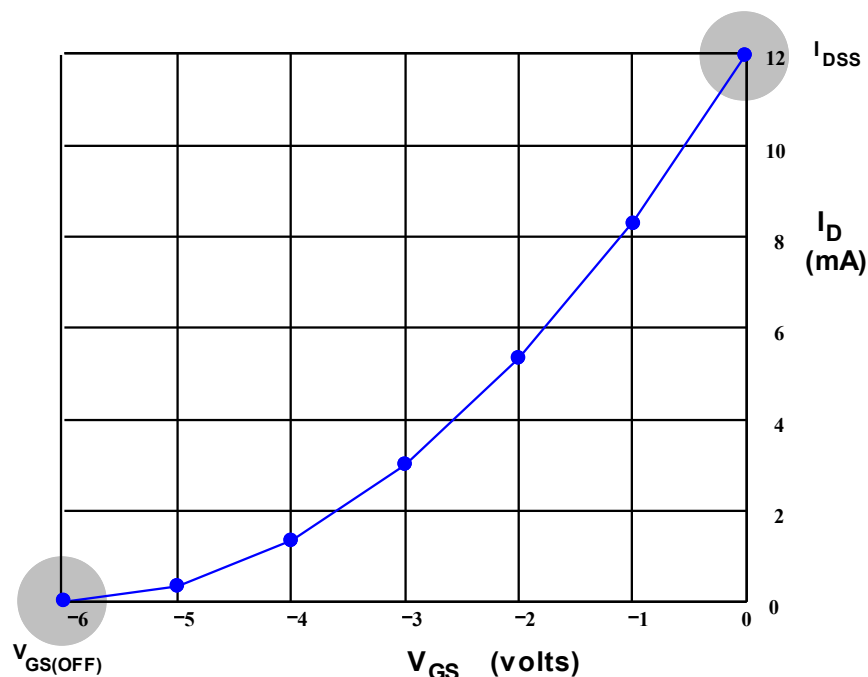


Figure 6-24.

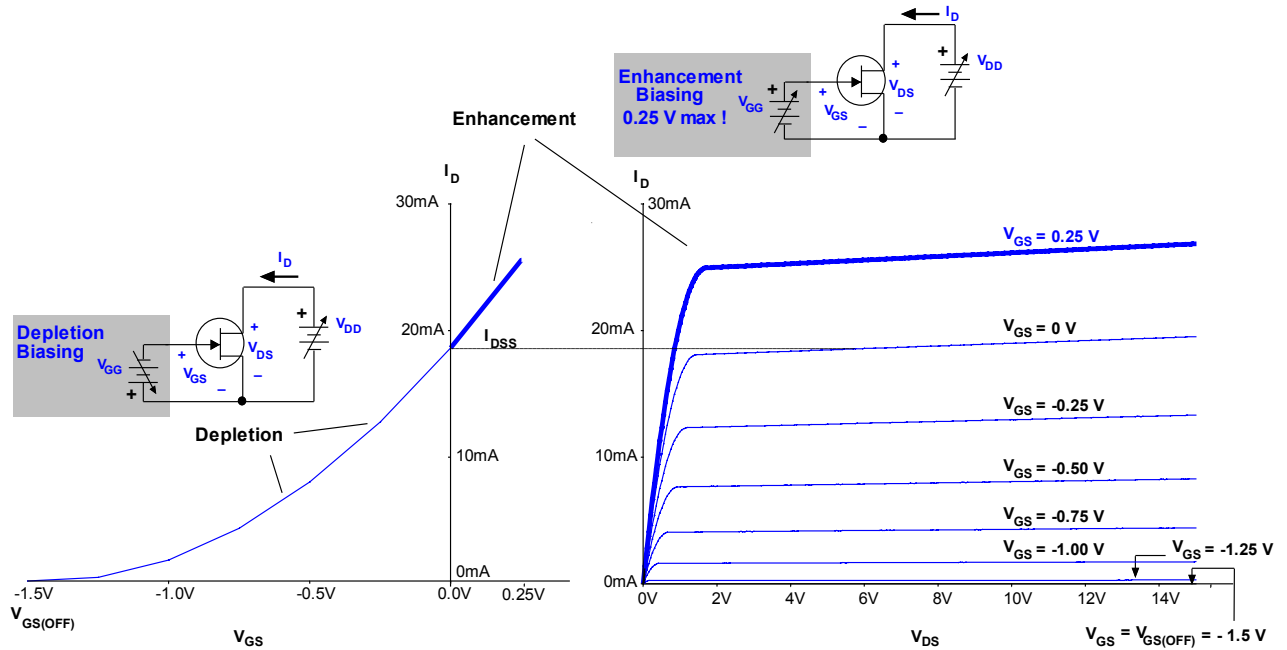
6-5 The Depletion-Enhancement MOSFET

Applying a negative V_{GS} to an n -channel JFET, increases the depletion region widths. The increase in the depletion regions reduces the thickness of the channel. This raises the channel resistance and reduces the number of available charge carriers. This produces a reduction in I_D . If we were to *reverse* the polarity of the gate bias supply V_{GG} to apply a *positive* V_{GS} , the p - n junctions between the gate and the channel would then be forward biased. Forward bias decreases the width of a depletion region and draws more charge carriers into the channel from the heavily doped (n^+) drain and source regions. This means ***the channel resistance will be less, and the drain current will increase beyond I_{DSS} .***

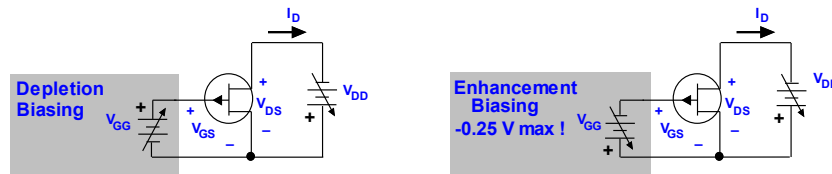
Thus, the JFET has two fundamental modes of operation: *depletion* and *enhancement*. Again, when an n -channel JFET has a negative value of V_{GS} , its drain current I_D is reduced. The reduction in I_D is attributed to the reduction (or depletion) in the number of available charge carriers within the channel. The JFET is in its ***depletion mode of operation***. When an n -channel JFET has a positive value of V_{GS} , its drain current I_D is increased. Again, it is the increase (or enhancement) in the number of charge carriers in the channel that raises I_D . The conductivity of the JFET's channel is increased, and the JFET is in its ***enhancement mode of operation***.

For reasons that will become apparent later, we do *not* want the gate current to rise to an appreciable value. Therefore, the forward bias of the silicon p - n junction is usually restricted to a maximum of 0.5 V. A more conservative 0.25-V limit is indicated in Fig. 6-25.

JFET Depletion-Enhancement Operation



(a) The n-channel JFET.



(b) The p-channel JFET.

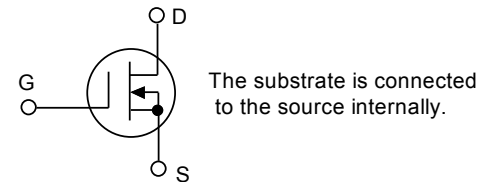
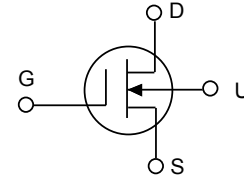
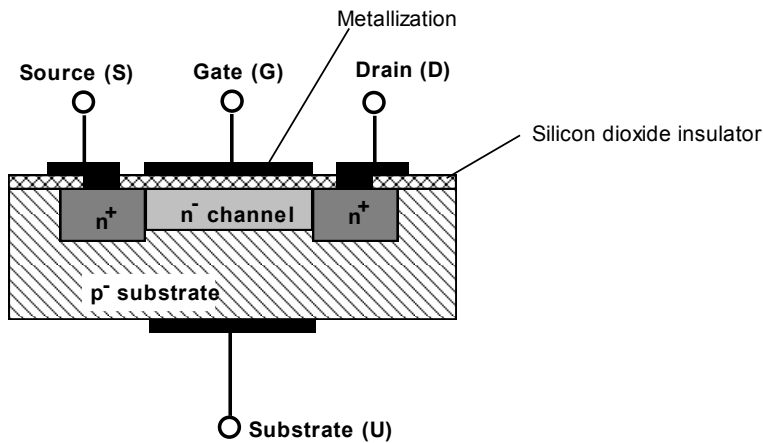
Figure 6-25.

Why Enhance?

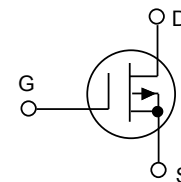
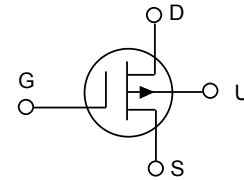
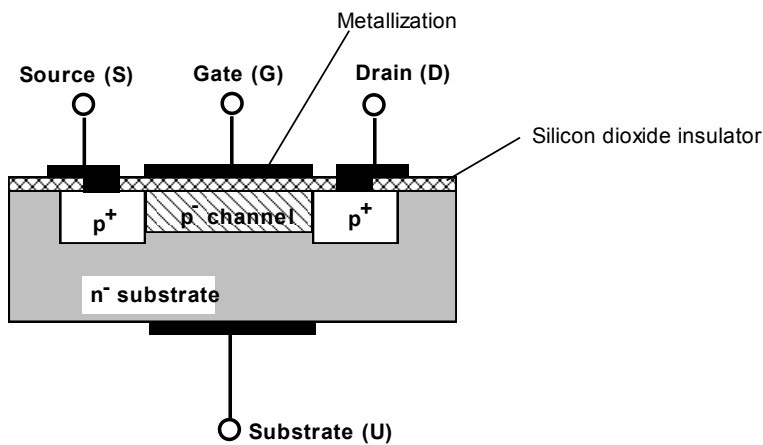
As we shall see in Chapter 8, the *greater* I_D is compared to I_{DSS} , the *greater* the voltage gain (A_v) will be. Yes, the *DC drain current* will affect the *AC voltage gain*! (Chapter 8 will also reveal the AC voltage gain of a BJT is directly proportional to its DC collector current.) In general, the higher the A_v , the better, and we see one of the advantages of being able to enhance the channel. However, the 0.25-V bias limit of a JFET limits its use in its enhancement mode of operation. Typically, the maximum gate current rating of a JFET is as low as 10 mA! If its gate current rating is exceeded, the JFET can fail. To overcome this limitation, the **depletion-enhancement metal oxide semiconductor FET** – the **DE-MOSFET** – was developed. Don't despair over this formidable acronym! Acronyms are used extensively in all technical communities. They *can* make life (and communication) easier.⁵⁴ The *n*- and *p*-channel DE-MOSFETs are described in Fig. 6-26.

⁵⁴ Knowledgeable, Accurate, Concise, Electrical Engineer, or *KACEE* was suggested by one of my students to be another useful acronym. By an astounding coincidence, the most talented student in the class was a Navy veteran named Kacee.

N- and P-Channel DE-MOSFETs



(a) The n-channel DE-MOSFET.



(b) The p-channel DE-MOSFET.

Figure 6-26.

The n -, and p -channel DE-MOSFET structures and schematic symbols are provided in Fig. 6-26. Note that some DE-MOSFETs have *four* terminals: the drain, gate, source, and *substrate*. In most applications, the substrate is tied to the source terminal. However, the substrate can be used as another (JFET-like) gate terminal. The schematic symbol suggests the equivalent capacitance that exists between the gate and the channel. (This will be explained shortly.) The vertical line represents the channel that connects the source and drain regions. The arrow points to the n -type material.

The silicon dioxide (SiO_2) layer is formed through a process called **passivation**. Pure heated oxygen is blown across the silicon. The resulting glass-like surface is an excellent electrical insulator. It also seals off the silicon to prevent contamination from the air, chemicals, or dopants.

Operation of a DE-MOSFET

The depletion mode of operation.

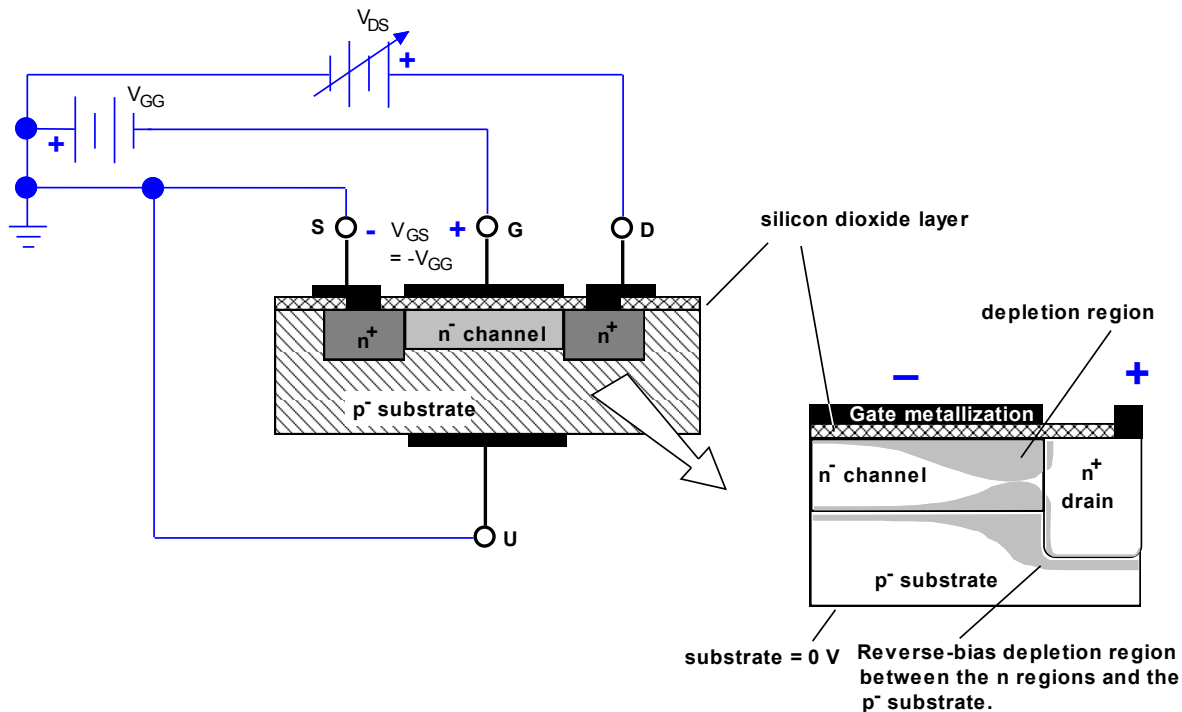


Figure 6-27.

The internal action of an n -channel DE-MOSFET is described in Fig. 6-27. Notice that V_{GS} is *negative*. Also observe that no p - n junction exists between the gate and the channel. The gate is electrically insulated by a very thin silicon dioxide (SiO_2) layer. The basic structure is very similar to a parallel-plate capacitor. The negative gate bias repels the negative electrons in the n^- channel. As a result, a depletion region forms to narrow the channel, reducing its conductivity. The reduction in the number of charge carriers in the channel raises its resistance in its ohmic region and lowers I_D in the saturation region. The process is very similar to the physical action in the JFET. In fact, we can make a generalized comparison. ***The JFET employs the electric field associated with a p - n junction to control the conductivity of its channel. The MOSFET utilizes the electric field associated with the capacitance between its gate and channel to control the conductivity of its channel.***

If we make V_{GS} positive, additional negative electrons will be drawn into the channel from the heavily doped n^+ source and drain regions. The additional electrons will increase the conductivity of the channel. The increase in the number of charge carriers in the channel lowers its resistance in its ohmic region and increases I_D in the saturation region. This is depicted in Fig. 6-28.

Operation of a DE-MOSFET

The enhancement mode of operation.

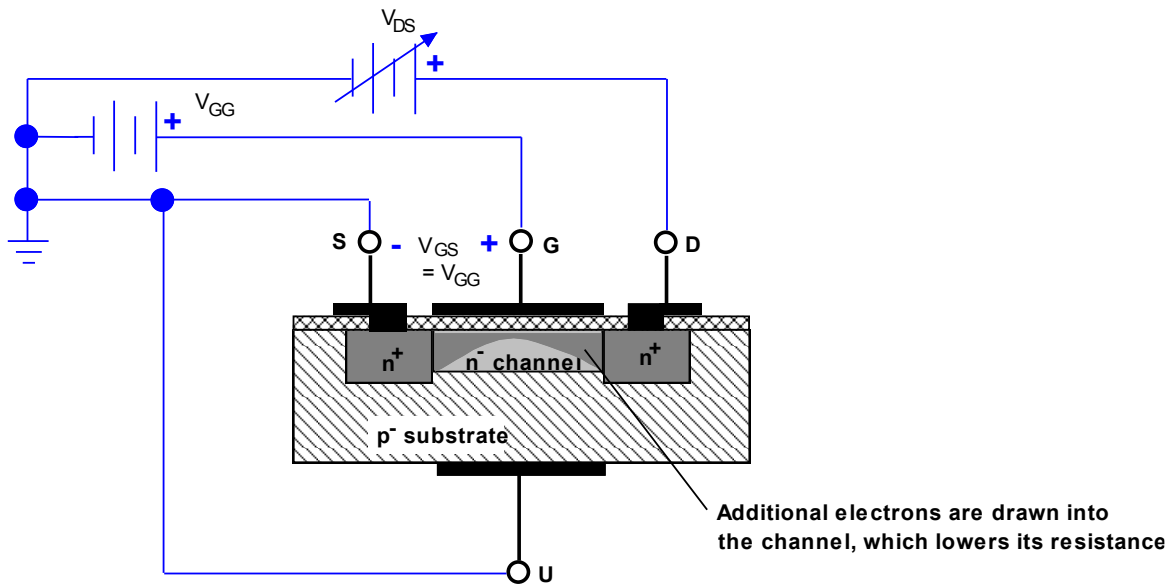


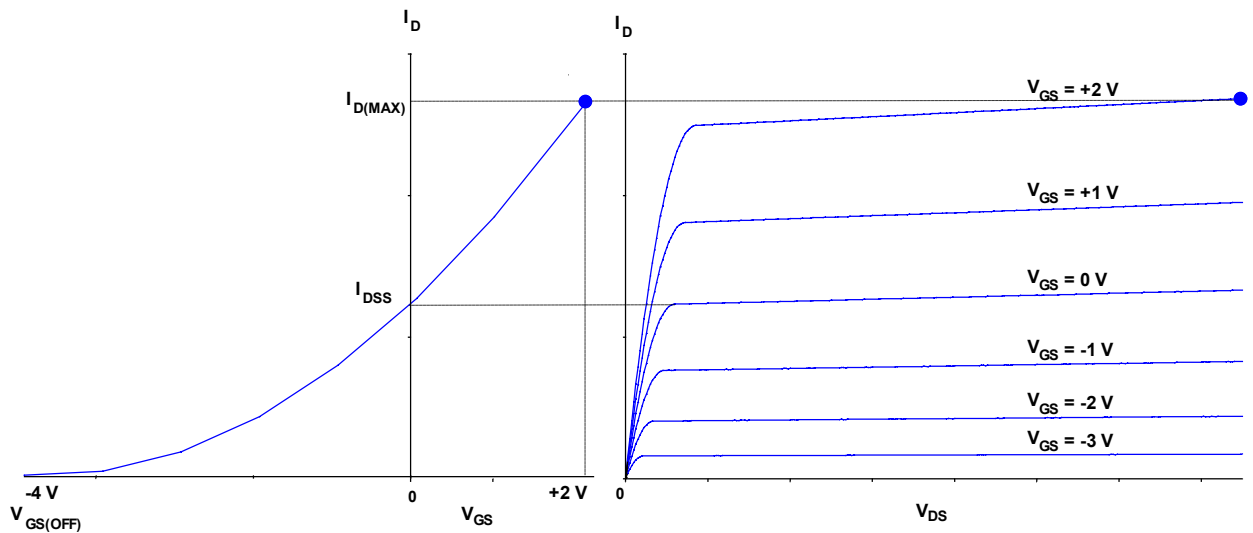
Figure 6-28.

Since we do not have to worry about turning on a p - n junction, V_{GS} can be much larger than the 0.25-V JFET limitation. However, since I_D can be increased **beyond** I_{DSS} , we must be careful not to exceed the maximum drain current limit $I_{D(MAX)}$. Refer to the V - I curves provided in Fig. 6-29. Typical curves for an n -channel DE-MOSFET and a p -channel DE-MOSFET are shown in Fig. 6-29(a) and (b), respectively. Since the drain current of a p -channel device flows out of its drain terminal, it is called *negative* by the transistor convention.

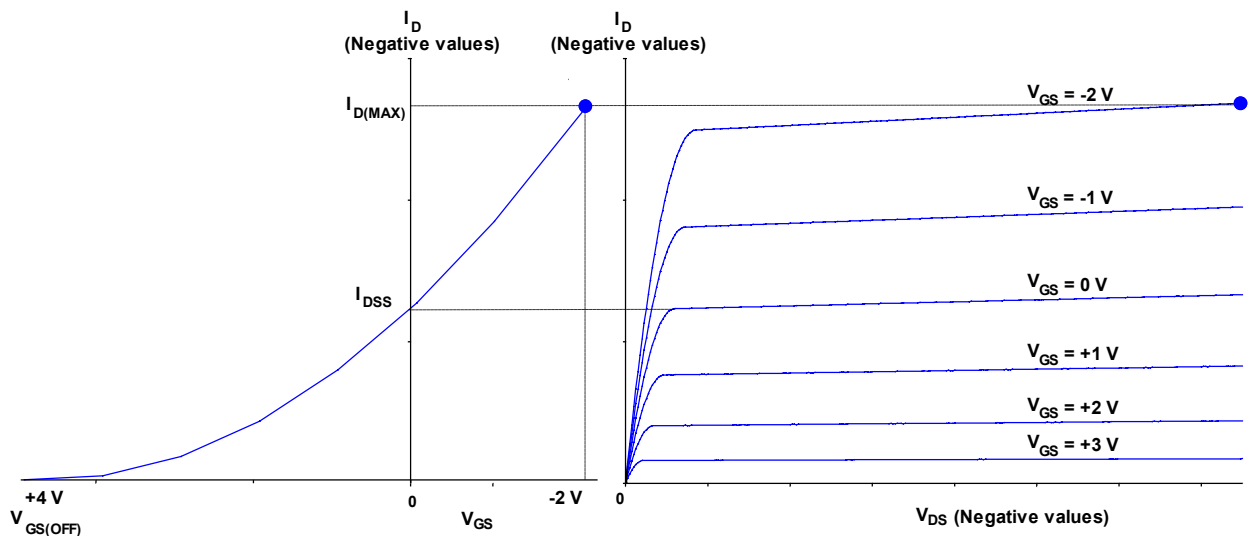
As a final comment we should note the gate leakage current (called I_{GSS}) for MOSFETs is much smaller than that of JFETs. The gate leakage current for JFETs is usually on the order of nanoamperes (nA), while the leakage current for MOSFETs is typically on the order of picoamperes (pA). Because the gate-to-source resistance of MOSFETs is so very large, it is possible that a large static charge can build on their gate terminals. If it exceeds about 100 V, the silicon dioxide (SiO_2) insulating layer may break down, destroying (or degrading) the MOSFET. Consequently, MOSFETs and MOSFET integrated circuits must be handled with caution. It is for that reason that MOSFETs are shipped in conductive foam carriers or with shorting rings around their leads to prevent inadvertent destruction due to static electricity.⁵⁵ This is called Electrostatic Discharge (ESD) protection.

⁵⁵ The mysterious failures of the early MOSFET devices were shown to be due to static discharge. Additional studies revealed that *all* solid-state devices are susceptible to damage produced by electrostatic discharge (ESD). Today, most solid-state devices, and printed circuit board assemblies are to be treated as ESD sensitive. Appropriate handling precautions must be used, such as the wearing of conductive wrist straps that are tied to ground, and the use of electrically grounded conductive mats at workstations.

DE-MOSFET V-I Curves



(a) The n-channel DE-MOSFET.



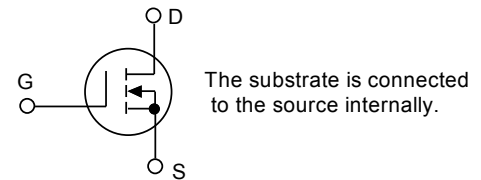
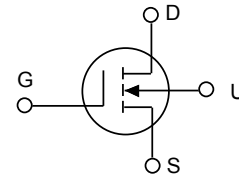
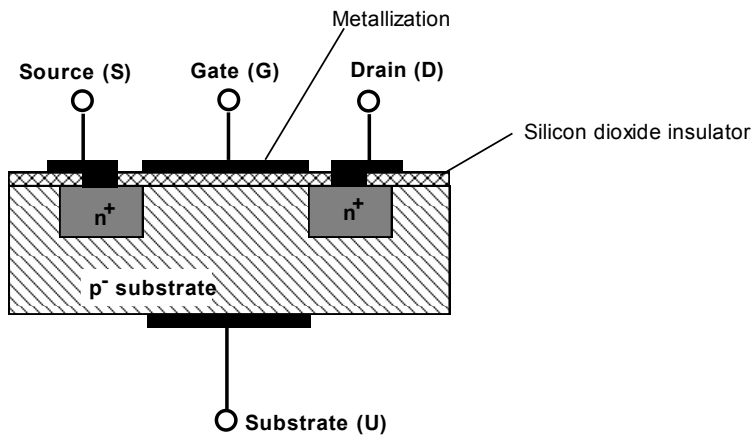
(b) The p-channel DE-MOSFET.

Figure 6-29.

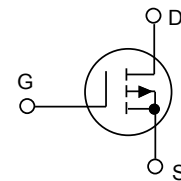
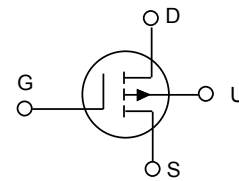
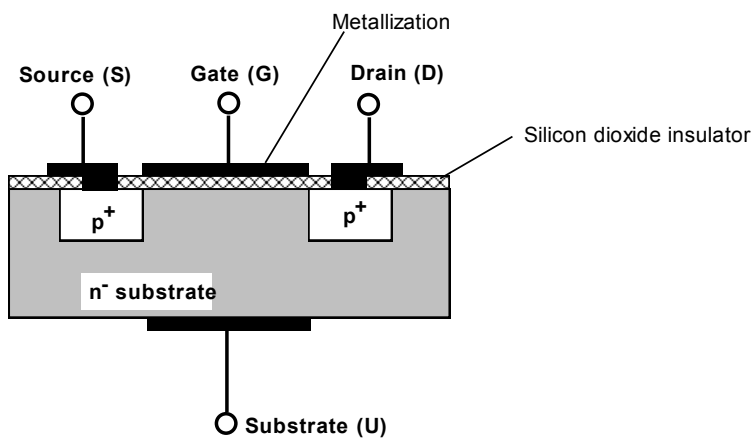
6-6 Enhancement MOSFETs

Figure 6-30(a) illustrates an *n-channel enhancement-only MOSFET (E-MOSFET)*. Its *p*-channel complement is shown in Fig. 6-30(b). Their schematic symbols are also given. The symbols are very similar to those for the DE-MOSFETs. However, there is one subtle, but very important difference – *dashed lines are used to represent the channels in the E-MOSFET symbols*. This is done to emphasize that *no* channels are doped into these MOSFET structures. As we shall see, the channels are induced electrically into these MOSFETs.

N- and P-Channel E-MOSFETs



(a) The n-channel E-MOSFET.



(b) The p-channel E-MOSFET.

Figure 6-30.

When V_{GS} is zero volts, the E-MOSFET has an I_D of approximately zero. The reason why this is so can be seen in Fig. 6-31(a). Effectively, we have two back-to-back diode junctions in series with some equivalent resistance. With a short circuit between the gate and source terminals, the drain p - n (diode-like) junctions are reverse biased regardless of the polarity of V_{DS} . Consequently, only a very small leakage current will flow between the drain and source terminals.

If V_{GS} is made positive, an electric field is formed in the gate region. The positive gate serves to attract minority carriers (electrons) from the p substrate and the n^+ drain and source regions. When the gate becomes sufficiently positive, enough minority carriers exist along the surface of the substrate to form an n -type channel between the source and drain regions. When this occurs, we have induced a channel by forming what is termed an ***inversion layer*** [see Fig. 6-31(b)].

Operation of the E-MOSFET

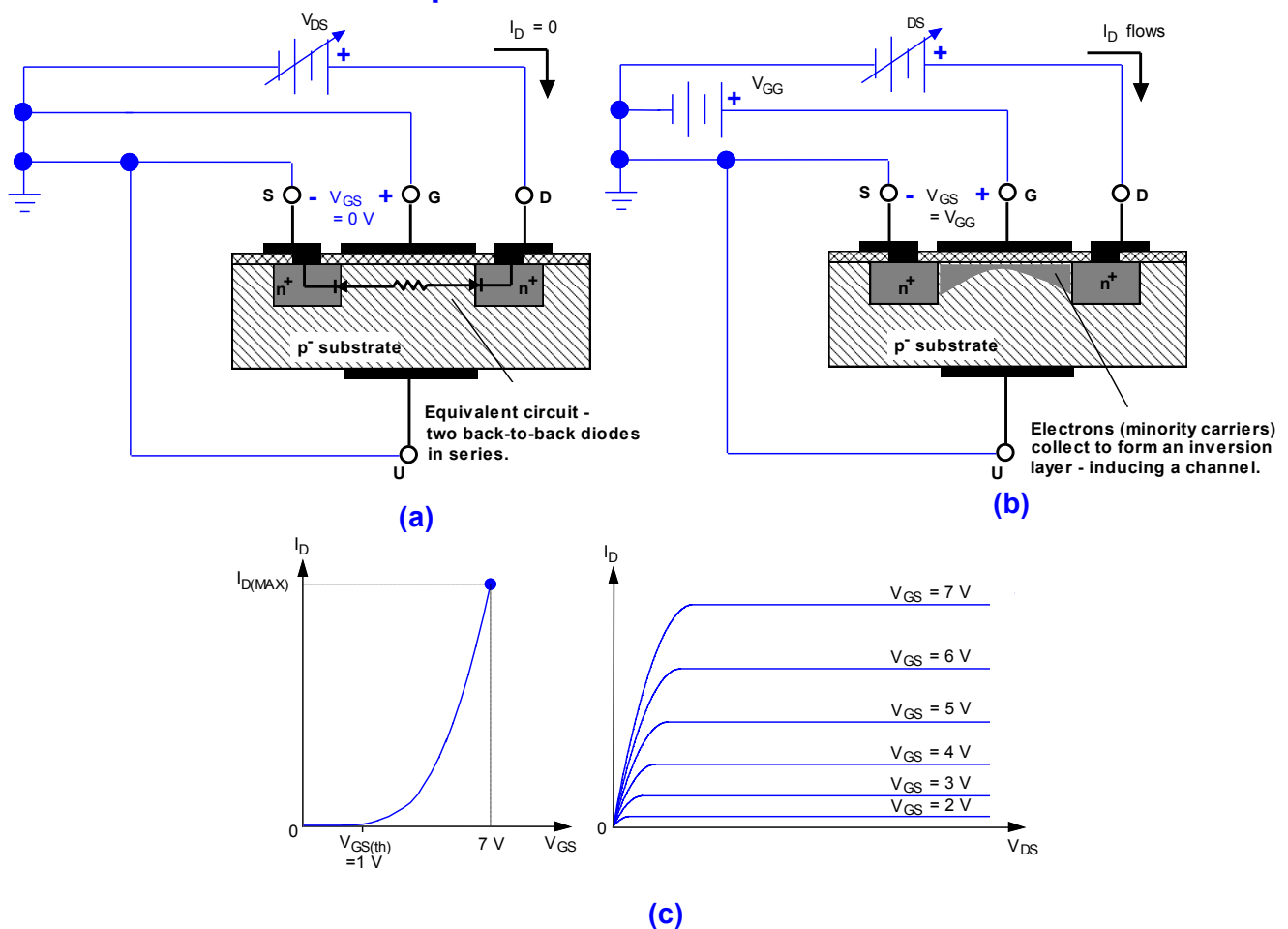


Figure 6-31.

The magnitude of V_{GS} required to form this inversion is termed the **gate-to-source threshold voltage** $V_{GS(th)}$. Manufacturers will typically indicate $V_{GS(th)}$ on their MOSFET data sheets. As V_{GS} is increased beyond $V_{GS(th)}$, I_D will begin to increase. The V - I curves for an n -channel E-MOSFET are depicted in Fig. 6-31(c).

The equation that describes the E-MOSFET's transfer characteristic does *not* obey Eq. 6-5. However, it does follow a similar “square-law type” of relationship. The equation for the transfer characteristic of an E-MOSFET is given by Eq. 6-6.

$$I_D = K[V_{GS} - V_{GS(th)}]^2 \quad (6-6)$$

where I_D is drain current of an E-MOSFET, K is a constant with units of amperes/volts², V_{GS} is the gate-to-source voltage, and $V_{GS(th)}$ is the gate-to-source threshold voltage.

While $V_{GS(th)}$ is generally published on the E-MOSFET data sheet, the constant K is *not*. However, the constant K can often be obtained *indirectly* from the manufacturer's data sheet. Consider Example 6-3.

Example 6-3. An n -channel E-MOSFET has a $V_{GS(th)}$ of 3.8 V and an $I_{D(ON)}$ of 10 mA when $V_{GS(ON)}$ is 8 V. Find its I_D when V_{GS} is 6 V.

Solution: First, we must use the given information and solve Eq. 6-6 to find K . (Both sides are divided by $[V_{GS} - V_{GS(th)}]^2$.)

$$K = \frac{I_D}{[V_{GS} - V_{GS(th)}]^2} = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_{GS(th)}]^2} = \frac{10 \text{ mA}}{[8 \text{ V} - 3.8 \text{ V}]^2} = 5.669 \times 10^{-4} \text{ A/V}^2 \cong 5.67 \times 10^{-4} \text{ A/V}^2$$

Now that we have determined K , we may use Eq. 6-6 to find I_D at the given V_{GS} .

$$I_D = K[V_{GS} - V_{GS(th)}]^2 = (5.669 \times 10^{-4})[6 \text{ V} - 3.8 \text{ V}]^2 = 2.744 \text{ mA} \cong 2.74 \text{ mA}$$

By inspection of Fig. 6-31(c), it should be clear that the parameters I_{DSS} and $V_{GS(OFF)}$ do not apply to the E-MOSFET. The E-MOSFET is very similar to the BJT in that it must be driven into conduction. Both the E-MOSFET and the BJT are described as being *normally-off devices*, while the JFETs and DE-MOSFETs are said to be *normally-on devices*. In this context, a device is normally off if it acts like an open switch with a controlling voltage (e.g., V_{GS} or V_{BE}) of zero. A device is normally on if it passes a current with a controlling voltage (e.g., V_{GS}) of zero.

6-7 Finding the Q-Point

As we have seen for the BJT, it is necessary to determine the Q-point. This is also the case for the FETs. The general procedure for the DC analysis of FET amplifiers is very similar to the procedure developed for the BJT. (Refer to Fig. 5-28 in Section 5-8.) Let us review and expand on the three-step procedure by contrasting the BJT with the FET.

1. **Analyze the input.** Apply Kirchhoff's voltage law around the input circuit to determine the controlling input quantity. For BJTs this means solving the resulting equation for I_B or I_E . However, for FETs we usually solve for V_{GS} .
2. **Transfer across the device.** For BJTs this is usually accomplished by using either β_{DC} or α_{DC} . However, with FETs we use its transfer equation. (This can be done analytically, or graphically.)
3. **Analyze the output.** Write a Kirchhoff's voltage law equation around the output circuit and solve for the output voltage. For BJTs, this may be either V_{CE} or V_{CB} . For FETs the output voltage is often V_{DS} .

Consider Fig. 6-32(a). The input signal is applied to the gate, and the output signal is extracted from the drain. This means we have a *common-source amplifier* (refer to Table 6-1). Capacitor C_1 is an input coupling capacitor. Capacitor C_2 serves as the output coupling capacitor. As we shall see in our later work, the gate resistor R_G is included for the benefit of DC bias stability and for the AC equivalent circuit. We have a drain supply V_{DD} and a gate bias supply V_{GG} . To perform the DC analysis, we regard the coupling capacitors as open circuits. For additional clarity, the DC supplies may be included in the DC equivalent circuit. This is done in Fig. 6-32(b). Note that the gate leakage current I_{GSS} has been indicated. Conventional current directions have been used for both I_{GSS} and I_D .

First, we write a Kirchhoff's voltage law equation around the input circuit.

$$V_{GG} - I_{GSS}R_G + V_{GS} = 0$$

We solve the equation for V_{GS} .

$$V_{GS} = -V_{GG} + I_{GSS}R_G$$

Typically, the leakage current I_{GSS} is so small the voltage drop across R_G is negligible. This gives rise to an approximation.

$V_{GS} \cong -V_{GG}$

 (6-7)

With a little thought, we can see that the gate-to-source bias voltage is fixed, or constant. Consequently, the FET circuit is employing **fixed gate bias**. The second step requires that we transfer from the input to the output by employing the transfer equation (Eq. 6-5). However, this requires information from the FET's data sheet. Specifically, we need to know the drain saturation current I_{DSS} and the gate-to-source cutoff voltage $V_{GS(OFF)}$. For convenience, Eq. 6-5 has been repeated below.

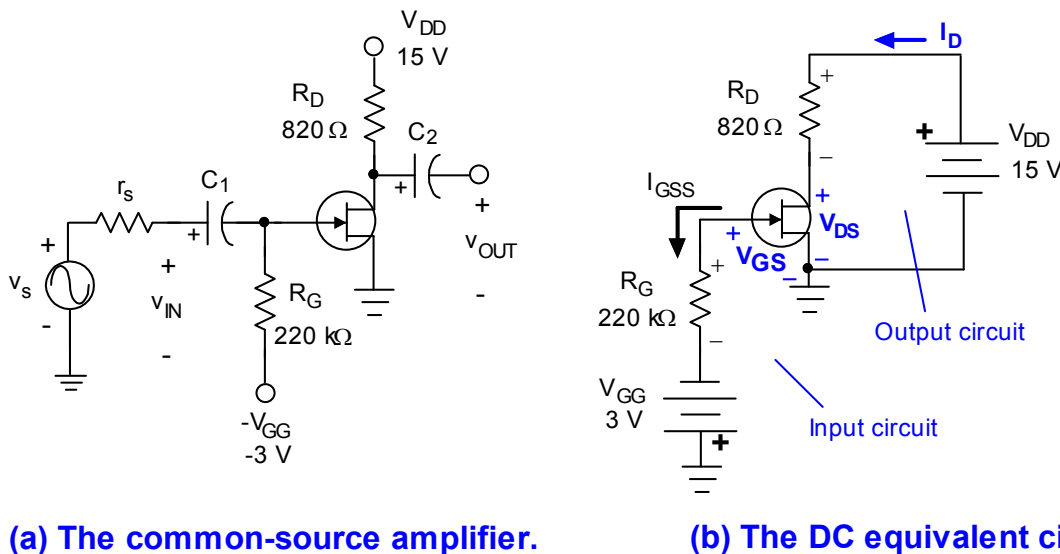
$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 \quad (6-5)$$

Equation 6-5 permits us to find I_D . The third step requires that we invoke Kirchhoff's voltage law and apply it to the output circuit. We solve it for V_{DS} .

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D \quad (6-8)$$

Finding the Q-Point of a Common-Source Amplifier



(a) The common-source amplifier.

(b) The DC equivalent circuit.

Figure 6-32.

Remember that voltage is *always* defined to be between two points. Consequently, V_{GS} means the voltage at the gate terminal relative to the source terminal. Similarly, V_{DS} is the voltage at the drain terminal relative to the source terminal. In Fig. 6-32(a) we see the source terminal is connected to ground. When a single subscript is used, it is implied the reference point is ground. This means V_G is the voltage at the gate terminal relative to ground and V_D is the voltage at the drain terminal relative to ground. Since the source terminal is connected to ground in this instance, $V_G = V_{GS}$, and $V_D = V_{DS}$.

Example 6-4. Perform a DC analysis of the common-source amplifier shown in Fig. 6-32(a). Specifically, determine V_{GS} , I_D , V_{DS} , V_G , and V_D .

Solution: With reference to the DC equivalent circuit shown in Fig. 6-32(b), we apply Eq. 6-7 to obtain the controlling input voltage V_{GS} .

$$V_{GS} = -V_{GG} = -3 \text{ V}$$

We transfer from the input circuit to the output circuit using Eq. 6-5. From the manufacturer's data sheets we learn that $I_{DSS} = 30 \text{ mA}$ and $V_{GS(OFF)} = -7 \text{ V}$.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 = (30 \text{ mA}) \left[1 - \frac{-3 \text{ V}}{-7 \text{ V}} \right]^2 = 9.796 \text{ mA} \cong 9.80 \text{ mA}$$

Analysis of the output circuit via Eq. 6-8 yields V_{DS} .

$$V_{DS} = V_{DD} - I_D R_D = 15 \text{ V} - (9.796 \text{ mA})(820 \Omega) = 6.967 \text{ V} \cong 6.97 \text{ V}$$

Since the source terminal is connected to ground, $V_G = V_{GS} = -3 \text{ V}$ and $V_D = V_{DS} = 6.97 \text{ V}$.

The Common-Source Amplifier for Example 5-5

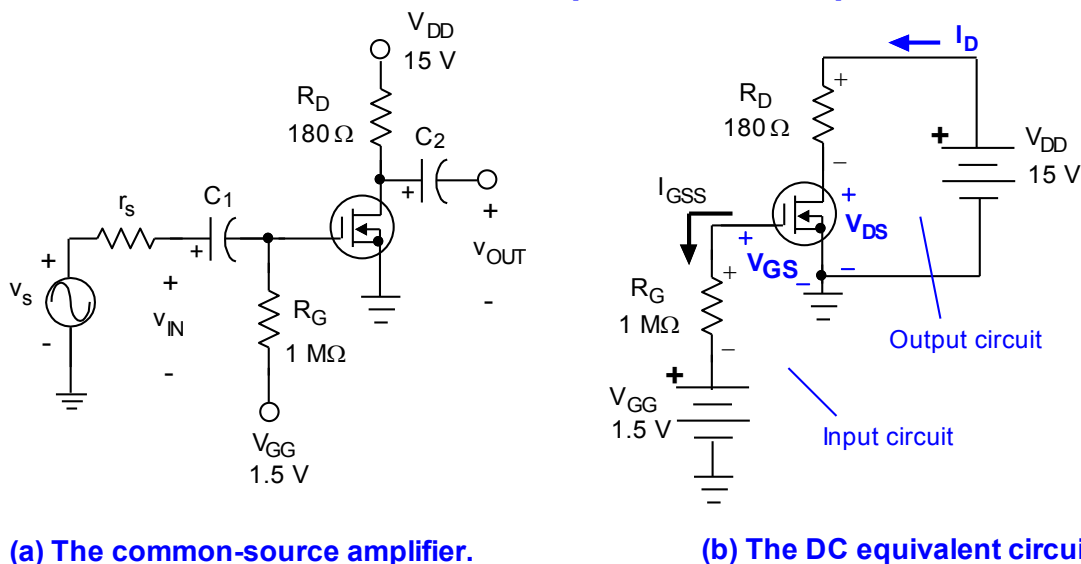


Figure 6-33.

Example 6-5. Perform a DC analysis of the common-source amplifier shown in Fig. 6-33(a). Specifically, determine V_{GS} , I_D , V_{DS} , V_G and V_D .

Solution: Observe that an n -channel DE-MOSFET is being used, and the gate bias supply V_{GG} has been *reversed*. With reference to the DC equivalent circuit shown in Fig. 6-28(b), we apply Eq. 6-7 to obtain the controlling input voltage V_{GS} .

$$V_{GS} = V_{GG} = 1.5 \text{ V}$$

A positive V_{GS} will enhance an n -channel DE-MOSFET. We transfer from the input circuit to the output circuit using Eq. 6-5. From the manufacturer's data sheets we learn that $I_{DSS} = 30 \text{ mA}$, $V_{GS(OFF)} = -7 \text{ V}$, and $I_{D(MAX)} = 75 \text{ mA}$.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 = (30 \text{ mA}) \left[1 - \frac{1.5 \text{ V}}{-7 \text{ V}} \right]^2 = (30 \text{ mA}) [1 + 0.2143]^2 = 44.23 \text{ mA} \cong 44.2 \text{ mA}$$

The drain current I_D has increased beyond I_{DSS} . However, the drain current is below the $I_{D(MAX)}$ rating of 75 mA. Analysis of the output circuit by Eq. 6-8 yields V_{DS} .

$$V_{DS} = V_{DD} - I_D R_D = 15 \text{ V} - (44.23 \text{ mA})(180 \Omega) = 7.038 \text{ V} \cong 7.04 \text{ V}$$

Since the source terminal is connected to ground, $V_G = V_{GS} = 1.5 \text{ V}$ and $V_D = V_{DS} = 7.04 \text{ V}$.

Circuit Saturation and Cutoff – It's Not Just for BJTs Anymore!

A common-emitter amplifier has a maximum collector current $I_{C(SAT)}$ and a maximum collector-emitter voltage $V_{CE(OFF)}$. These two conditions occur when the BJT enters saturation⁵⁶ and cutoff, respectively. In an identical fashion, an FET common-source amplifier has a maximum drain current called $I_{D(SAT)}$ and a maximum drain-to-source voltage called $V_{DS(OFF)}$. The circuit saturation and cutoff conditions are illustrated in Fig. 6-34. **In saturation, an FET (or a BJT) acts like a closed switch. In cutoff, an FET (or a BJT) acts like an open switch.** From Fig. 6-34(a), we obtain Eq. 6-9 for $I_{D(SAT)}$.

⁵⁶ When the JFET or DE-MOSFET **device** enters saturation, it is in its constant-current mode of operation. When a JFET or DE-MOSFET **circuit** enters saturation, it is in its non-linear region of operation.

$$I_{D(SAT)} = \frac{V_{DD}}{R_D}$$

(6-9)

Figure 6-34(b) helps us to determine $V_{DS(OFF)}$.

$$V_{DS(OFF)} = V_{DD}$$

(6-10)

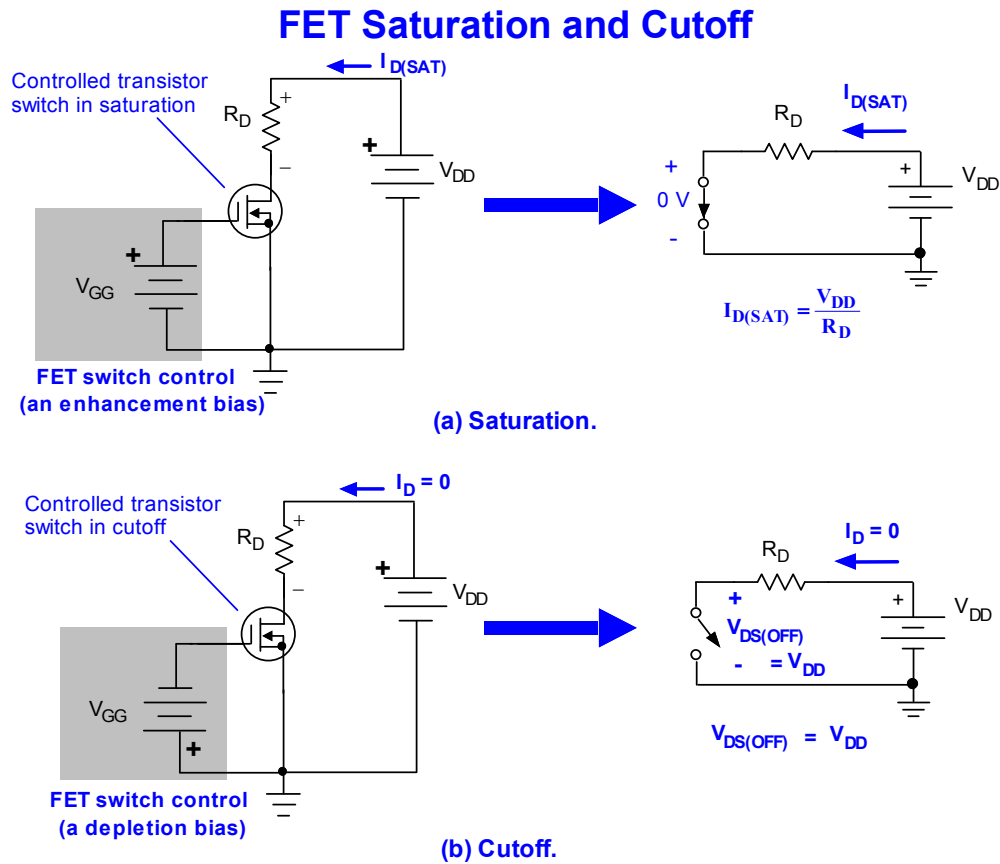


Figure 6-34.

Using EDA to Analyze an FET Bias Circuit

Multisim can be used to predict an FET's Q-point. We can use Multisim to analyze a common-source amplifier that employs a 2N5484 *n*-channel JFET. The model for the 2N5484 is in the Transistor. The DC power supplies are in the **Power Sources** library as shown in Fig. 6-35(a). The drain supply V_{DD} uses a DC power supply bus symbol. The V_{DD} symbol is to be interpreted as being the positive terminal of a 15-V DC power supply with its negative terminal connected to ground. This simplifies the schematic diagram and makes it easier to generate the netlist required for printed circuit boards. After the simulation is run, we arrive at the solution shown in Fig. 6-35(b). The results have been labeled V_{DS} and V_{GS} by placing text boxes. Use **Place** and select **Text**. You are encouraged to verify these results by Multisim and performing a DC analysis using the steps illustrated in Example 6-4.

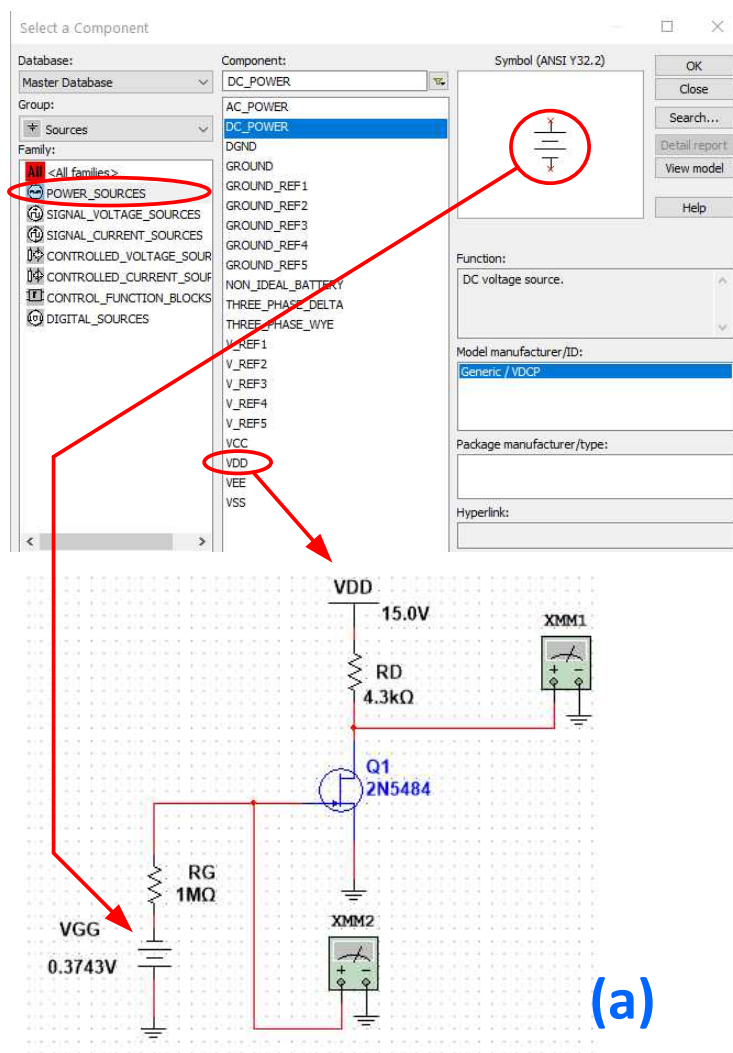


Figure 6-35.

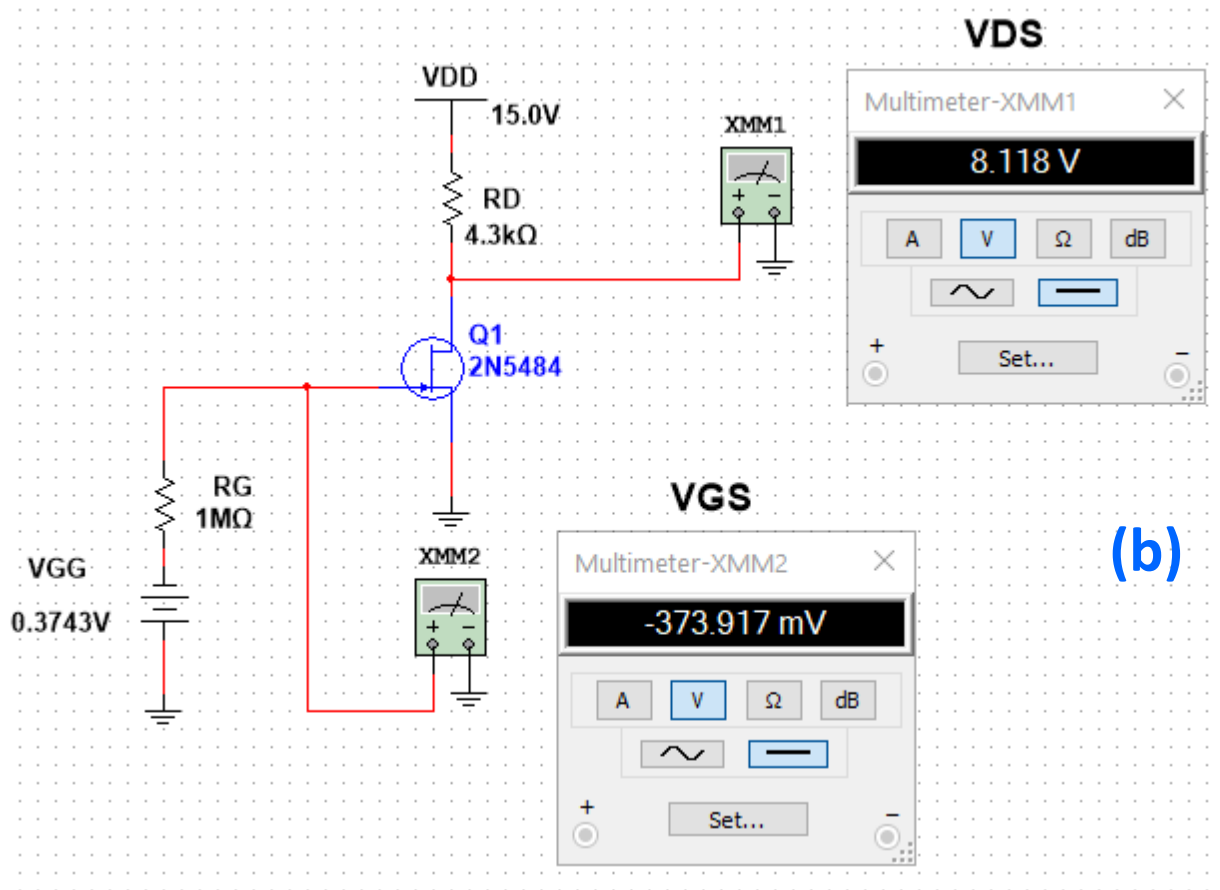


Figure 6-35 (continued).

6-8 The FET Signal Process and Applying Superposition

In Section 5-9 we traced the signal flow through a *common-emitter* BJT amplifier. (You may wish to review that section before proceeding.) Now we consider the FET equivalent – the *common-source* amplifier. To expedite our analysis, we shall draw on the ***principle of superposition***. Our future “serious” amplifier analyses will be based on the superposition theorem⁵⁷. In basic circuit analysis we are taught this method for analyzing multiple-source circuits. That is precisely the situation we have in our amplifier circuits. We have a DC voltage source that establishes the FET’s (or BJT’s) DC operating point and an AC voltage source (our signal) applied simultaneously.

⁵⁷ Many students issue either a long, sustained groan or a quick explicative on hearing this, but it will indeed make our work *much* easier.

To refresh ourselves, we state the superposition theorem:

The superposition theorem is used to analyze electric circuits in which there are two or more sources acting simultaneously to produce a net voltage or current. To find this unknown voltage or current by superposition, we find the component produced by each source, in turn with all other sources set to zero, and algebraically add the individual components to arrive at the net effect. The primary constraint upon the superposition theorem is that the *circuit must be linear*.

The superposition theorem permits us to perform separate DC and AC analyses. However, linearity is a requirement. This is accomplished by constraining the AC signals to be *small*. We postpone an in-depth investigation of the meaning of this requirement until Chapter 9 found in Volume Two. The use of superposition is explained in Fig. 6-36.

In Fig. 6-36(a) we see a JFET voltage amplifier – **analyzed previously in Example 6-4** – is being driven by an AC signal source. The AC signal source provides a 10-mV peak sinusoidal signal. Recall from Section 5-9 that the coupling capacitors act like open circuits to DC. This means the AC signal source is disconnected from the DC equivalent circuit. (This result is equivalent to setting the AC voltage source to zero and drawing the DC steady-state equivalent circuit.) The DC equivalent circuit and its analysis are summarized in Fig. 6-36(b).

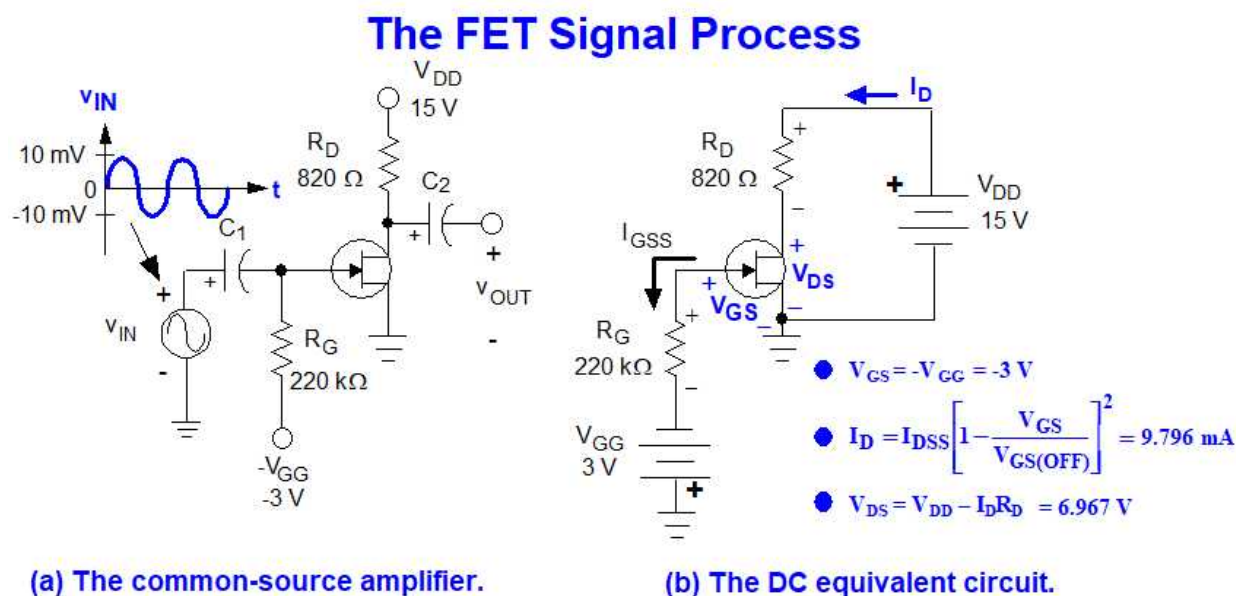
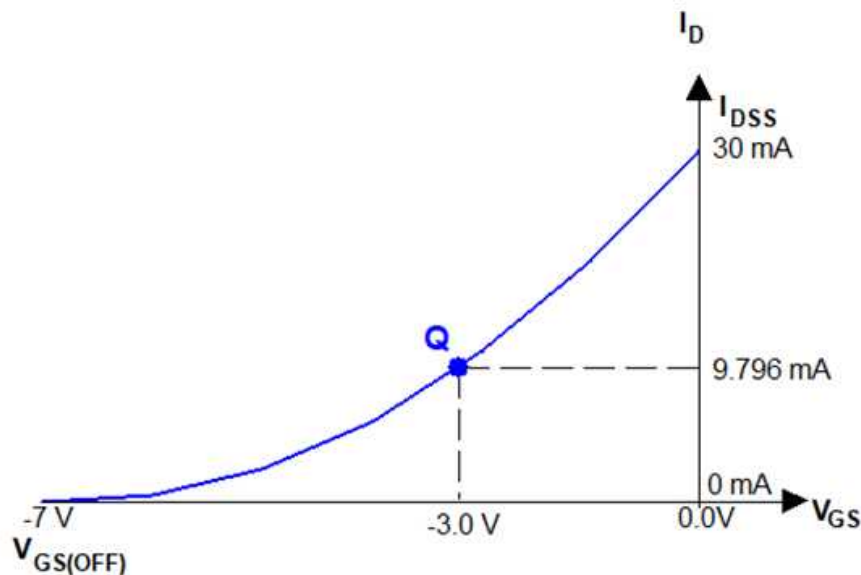


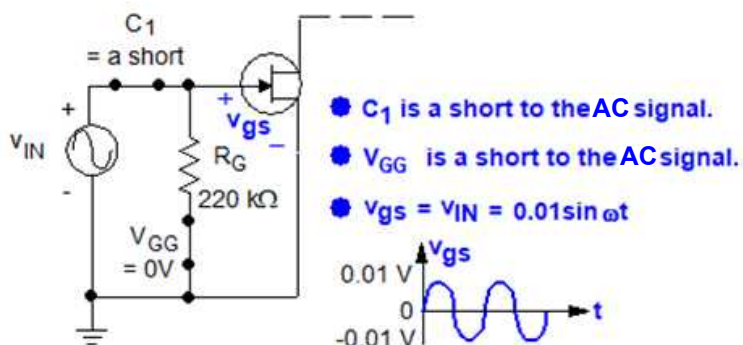
Figure 6-36.

The Q-point has been located graphically on the FET's transfer characteristic curve as indicated in Fig. 6-36(c). The *AC equivalent gate circuit* has been drawn in Fig. 6-36(d). **A DC voltage source (like V_{GG}) will act like a short circuit to an AC signal.** The DC voltage source V_{GG} connects from the bottom of resistor R_G and ground [see Fig. 6-36(b)]. By definition, a DC voltage source produces a constant voltage independent of the current through it. If we also recall that a capacitor opposes a change in voltage, then a DC voltage source must act like an infinitely-large capacitance. Since capacitive reactance $X_c = 1/(2\pi fC)$ it must indeed be zero. (Again, the net result is equivalent to applying the superposition theorem. When the AC voltage source is considered, and the DC voltage source is set to zero by replacing it with a short circuit.)

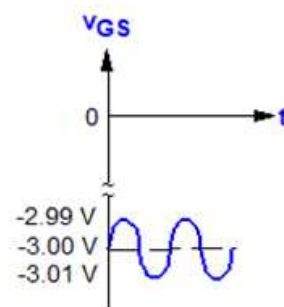
The AC input signal v_{IN} is given by $0.01\sin\omega t$. The last step in the application of the superposition theorem is to algebraically add the individual components produced by each of the sources acting alone. The signal source adds to and subtracts from V_{GG} . This is made evident by the application of the superposition theorem [see Fig. 6-36(e)].



(c) Locating the Q-point on the transfer characteristic.



(d) The AC equivalent input circuit.



(e) The total instantaneous gate voltage.

Figure 6-36 (continued).

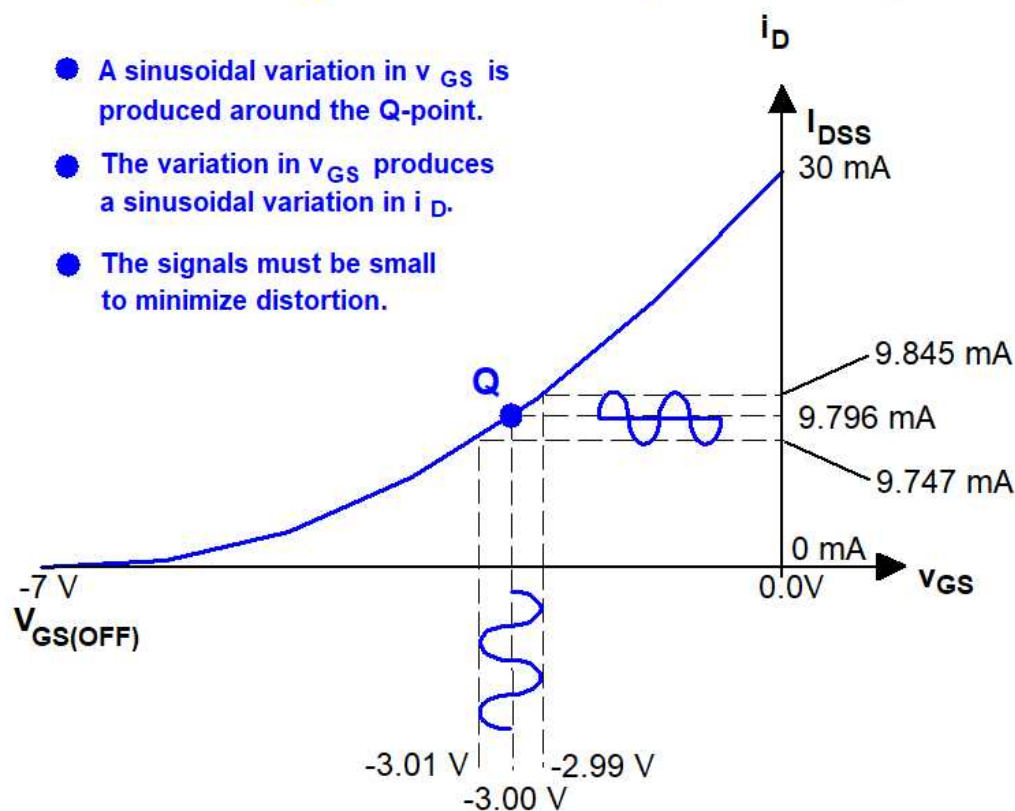
The total instantaneous gate-to-source voltage v_{GS} is defined by Eq. 6-11.

$$v_{GS} = V_{GS} + v_{gs} = -V_{GG} + v_{IN} = -3 + 0.01\sin\omega t \quad (6-11)$$

Where V_{GG} is the DC gate-to-source voltage and v_{gs} is the AC gate-to-source voltage. Note the signal is very small compared to the DC bias such that the total instantaneous gate-to-source voltage is *always* negative.

Now that we have analyzed the input, we must transfer across the FET to analyze the output circuit. The total instantaneous gate-to-source voltage v_{GS} controls the total instantaneous drain current i_D . This is illustrated in Fig. 6-37(a) using the FET's transfer characteristic curve. When v_{GS} is equal to -2.99 V, we have the maximum instantaneous drain current. When v_{GS} is -3.01 V, we have the minimum instantaneous drain current. Since the transfer characteristic is non-linear, the signal levels must be small to avoid significant distortion.

The FET Signal Process (continued)

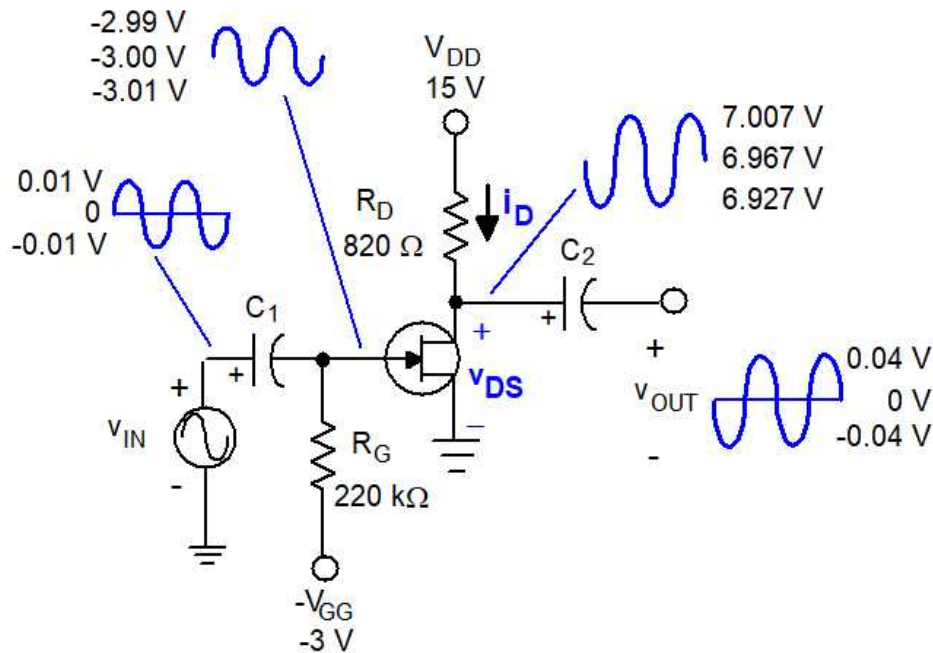


(a) Transferring across the FET.

Figure 6-37.

The instantaneous drain-to-source voltage v_{DS} can be determined by using Kirchhoff's voltage law. The resulting equation is *identical* to the relationship developed for the DC analysis.

$$v_{DS} = V_{DD} - i_D R_D$$



(b) The waveforms.

Figure 6-37 (continued).

When i_D is at its *maximum* value of 9.845 mA, v_{DS} is at its *minimum* value.

$$v_{DS} = V_{DD} - i_D R_D = 15 \text{ V} - (9.845 \text{ mA})(820 \Omega) = 6.927 \text{ V}$$

When i_D is at its *minimum* value of 9.747 mA, v_{DS} is at its *maximum* value.

$$v_{DS} = V_{DD} - i_D R_D = 15 \text{ V} - (9.747 \text{ mA})(820 \Omega) = 7.007 \text{ V}$$

The total instantaneous drain current is equal to I_D when the AC signal passes through zero. The various waveforms are illustrated in Fig. 6-37(b). The output coupling capacitor C_2 blocks the DC level at the drain. This means the output signal will be pure AC – positive and negative symmetrically about zero.⁵⁸ **Observe that the common-source amplifier shifts the phase of its input signal by 180°.** In this respect, it is *exactly* like its BJT counterpart the common-emitter amplifier.

The common-source amplifier provides an open-circuit voltage gain of -4 .

$$A_{v(oc)} = \frac{v_{OUT}}{v_{IN}} = \frac{40 \text{ mV peak } \angle -180^\circ}{10 \text{ mV peak } \angle 0^\circ} = 4 \angle -180^\circ = -4$$

⁵⁸ Rigorously, there must be some resistance to ground the right end of C_2 . In lab this can be accomplished by the equivalent resistance (usually 1 MΩ) of a direct-coupled oscilloscope. The output waveform will be observed to drift down as capacitor C_2 charges toward V_{DS} .

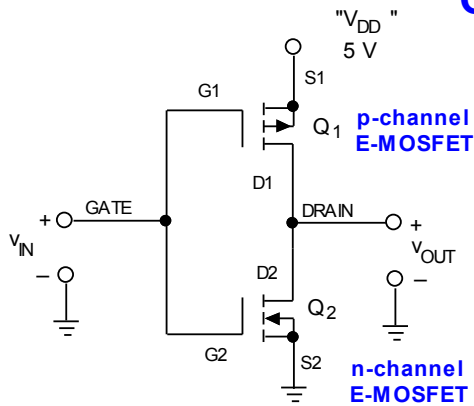
This voltage gain certainly is not nearly as large as the of voltage gain of 76.9 we obtained for the BJT common-emitter amplifier illustrated in Fig. 5-32. This is typical. ***In general, the voltage gain offered by FETs is not as large as the voltage gains provided by BJTs.*** We shall see more examples of this as our studies progress. Regardless of their rather “puny” voltage gains, FETs do offer several other performance advantages over BJTs. We shall also discover these in our later endeavors.

6-9 CMOS – The Logical Choice for Linear

When we have a p -channel E-MOSFET and an n -channel E-MOSFET configured as shown in Fig. 6-38(a), we have formed a new active device combination, which is described as a *complementary* MOSFET, or CMOS, pair. The basic circuit is found in digital logic inverters [Fig. 6-38(b)] and is also used as the typical output stage of a CMOS operational amplifier. Observe in Fig. 6-38(b) the inverter’s ***truth table*** has been supplied. When the input is a binary “0” (which corresponds to 0V and is also called low), the output is a binary “1” (which corresponds to 5 V and is also called high). The converse is also true. In digital logic only two values can occur - 0 or 1. Therefore, we can say ***the output of the inverter is always not equal to its input.*** Consequently, the logic inverter is also called a ***not gate***. The construction of a CMOS pair has been depicted in Fig. 6-38(c). CMOS initially started out as a technology restricted primarily to digital integrated-circuit functions. However, its use has been extended to encompass a wide range of new products. Typical digital integrated-circuit applications include logic gates, counters, registers, memories, and microprocessors. Linear integrated-circuits applications include audio filters, phase-locked loops, and operational amplifiers. We also find CMOS used in analog-digital functions, including analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

Let us take a brief look at how the fundamental CMOS “building block” shown in Fig. 6-38(a) operates. However, before we begin, let us recall two basic facts. First, a negative gate-to-source voltage is required to enhance a p -channel E-MOSFET, and second, a positive gate-to-source voltage is required to enhance an n -channel E-MOSFET.

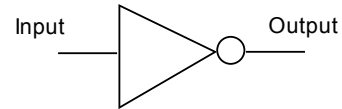
CMOS



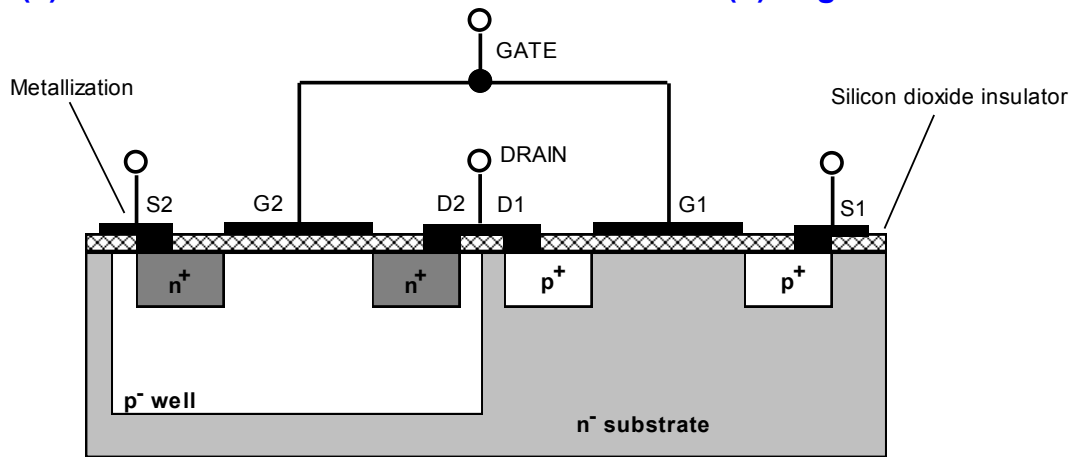
(a) CMOS Schematic.

Truth Table

Input	Output
0 (0V or Low)	1 (5V or Hi)
1 (5V or Hi)	0 (0V or Low)



(b) Logic inverter.

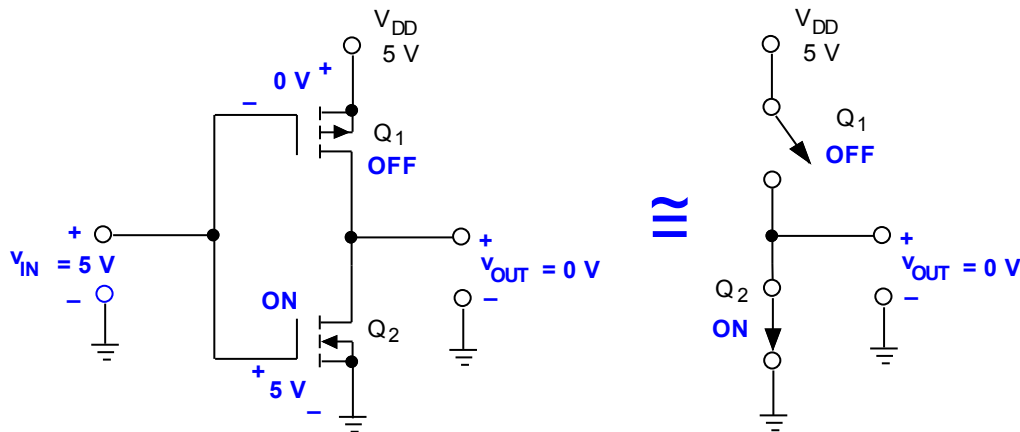


(c) CMOS structure.

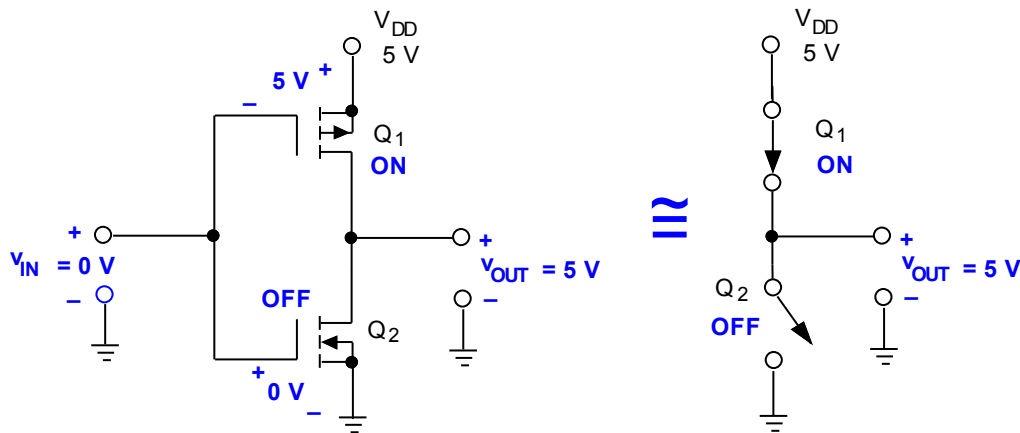
Figure 6-38.

In Fig. 6-39(a) we see that if v_{IN} is equal to 5 V, the p -channel E-MOSFET (Q_1) is non-conducting or OFF. This is true because its v_{GS} is zero. (An E-MOSFET that is OFF can be thought of as an open switch.) However, the v_{GS} of Q_2 is equal to 5 V. This voltage is assumed to be well beyond the threshold voltage $V_{GS(th)}$ for the n -channel device. Consequently, the n -channel E-MOSFET (Q_2) is well into conduction, or ON. (An E-MOSFET that is ON can be thought of as a closed switch.) Therefore, the output is effectively tied to ground by the n -channel E-MOSFET (Q_2), and v_{OUT} is approximately zero volts. Note that since Q_1 behaves like an open switch, no current is drawn from the 6-V supply.

CMOS Operation



(a) A HI input.



(b) A LO input.

Figure 6-39.

In Fig. 6-39(b) we see that if v_{IN} is equal to 0 V , the n -channel E-MOSFET (Q_2) is non-conducting or OFF. This is true because its v_{GS} is zero. However, the v_{GS} of Q_1 is equal to -5 V . This voltage is assumed to be well beyond the threshold voltage $V_{GS(th)}$ for the p -channel device. Consequently, the p -channel E-MOSFET (Q_1) is well into conduction, or ON. Therefore, the output is effectively tied to the 6-V supply by transistor Q_1 , and v_{OUT} is approximately 5 V . Note that since Q_2 behaves like an open switch, no current is drawn from the 6-V supply.

Essentially, we have just described the operation of a CMOS inverter logic gate found in digital logic applications. In digital applications, a voltage level of 0 V is also called “LO” or a “0”. A voltage level of 5 V is regarded as “HI” or a “1”. This discussion also reveals a significant advantage offered by CMOS logic – **a CMOS pair draws negligible current when its output assumes a HI or LO logic state**. This means that CMOS technology is ideal for battery-powered portable electronic products such as calculators, digital watches, cellular telephones, and notebook computers. It promotes a long battery lifetime. Further, a CMOS pair does draw current as it makes a transition from HI to LO or LO to HI in its output state.

CMOS technology has been adapted to linear applications. To understand the basic operation of the CMOS pair, we offer Fig. 6-41. In Fig. 6-41(a) we see a simple linear CMOS amplifier. Observe that the gate terminals have been biased to $V_{DD}/2$. Capacitors C_1 and C_2 serve as the input and output coupling capacitors, respectively. Since the E-MOSFETs employed in the CMOS pair reside on the same piece of silicon, it is assumed their electrical characteristics are matched closely. Therefore, they conduct equally. This means V_{DD} splits equally between the two transistors.

In Fig. 6-41(b) we see the effect of applying an input signal voltage. As v_{IN} goes positive, the n -channel E-MOSFET becomes more conductive, and the p -channel E-MOSFET becomes less conductive. The voltage divider action between the two FETs results in a decrease in v_D , and we obtain the negative half-cycle of v_{OUT} . Similarly, as v_{IN} goes negative, the gate-to-ground voltage decreases, the p -channel E-MOSFET (Q_1) becomes more conductive, the n -channel device (Q_2) becomes less conductive, and v_D increases. This produces the positive half-cycle of v_{OUT} . Note the input-output phase relationship is -180° as indicated in Fig. 6-41(b). Since the input signal is applied to the gate terminals, and the output signal is being taken from the drain terminals, *both* FETs are being used in their common-source configuration.

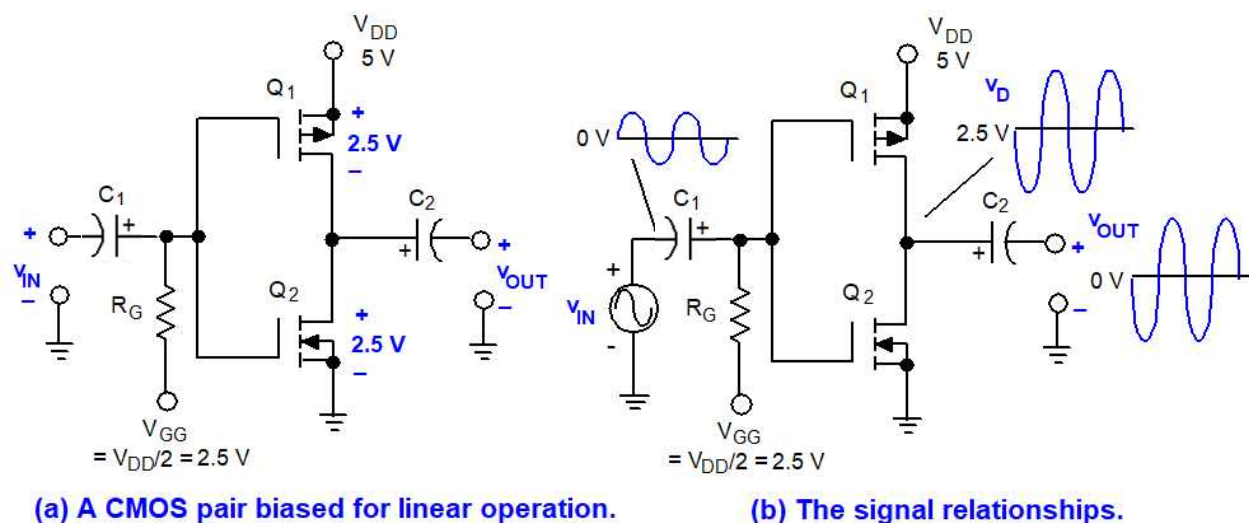


Figure 6-41.

6-10 MOSFET Latching Circuit.

A **latch** keeps something closed but does not **lock** it. In this application a normally open pushbutton is pushed momentarily to latch the system closed. When that same pushbutton is depressed momentarily again, the system will latch open. In this case a closed system applies power to a load. When the system is open, power is removed from the load.

Just as a BJT can be used as a switch, so can the MOSFET. The **IRF9540PBF** E-MOSFET is used in this application. It is a power device in a TO-220AB case style as illustrated in Fig. 6-42.

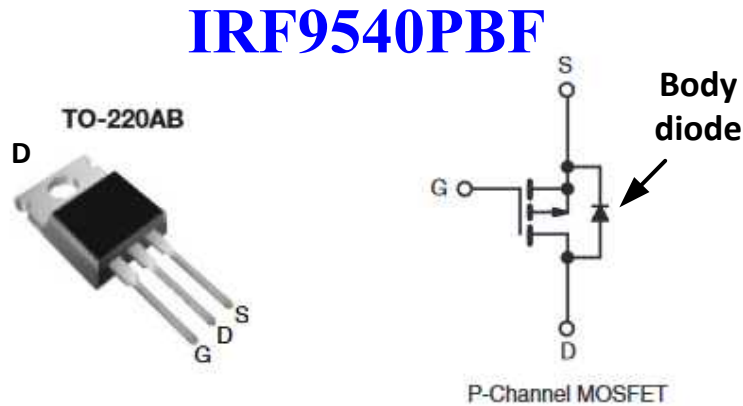


Figure 6-42.

The drain terminal is also connected to the device mounting tab. The schematic symbol also includes the body diode, which is regarded to be a useful parasitic device.

The E-MOSFET exhibits a low resistance (called $R_{DS(ON)}$) between its drain and source terminals when it is in hard conduction. Figure 6-43 depicts the basic operation. The E-MOSFET is being used as a controlled switch. When its gate is open [Fig. 6-43(a)] the E-MOSFET acts like an open switch and no voltage is applied to the load. If the gate is taken to ground as indicated in Fig. 6-43(b) the E-MOSFET behaves like a closed switch and voltage is applied to the load. The resistor R_1 is necessary to prevent the gate from floating. It ensures the E-MOSFET goes OFF.

Key parameters for the **IRF9540PBF** are obtained from a manufacturer's data sheet.

$V_{GS(th)}$: -2 to -4V
 V_{GS} : ± 20 V maximum
 V_{DS} : -100 V maximum
 I_D : -19 A maximum
 $R_{DS(ON)}$: 0.2 Ω maximum

With a V_{GS} of 12 V the threshold voltage will be exceeded, which means the E-MOSFET will be in hard conduction. Furthermore, the maximum V_{GS} will not be exceeded. The resistance between the drain and source terminals will be less than 0.2 Ω .

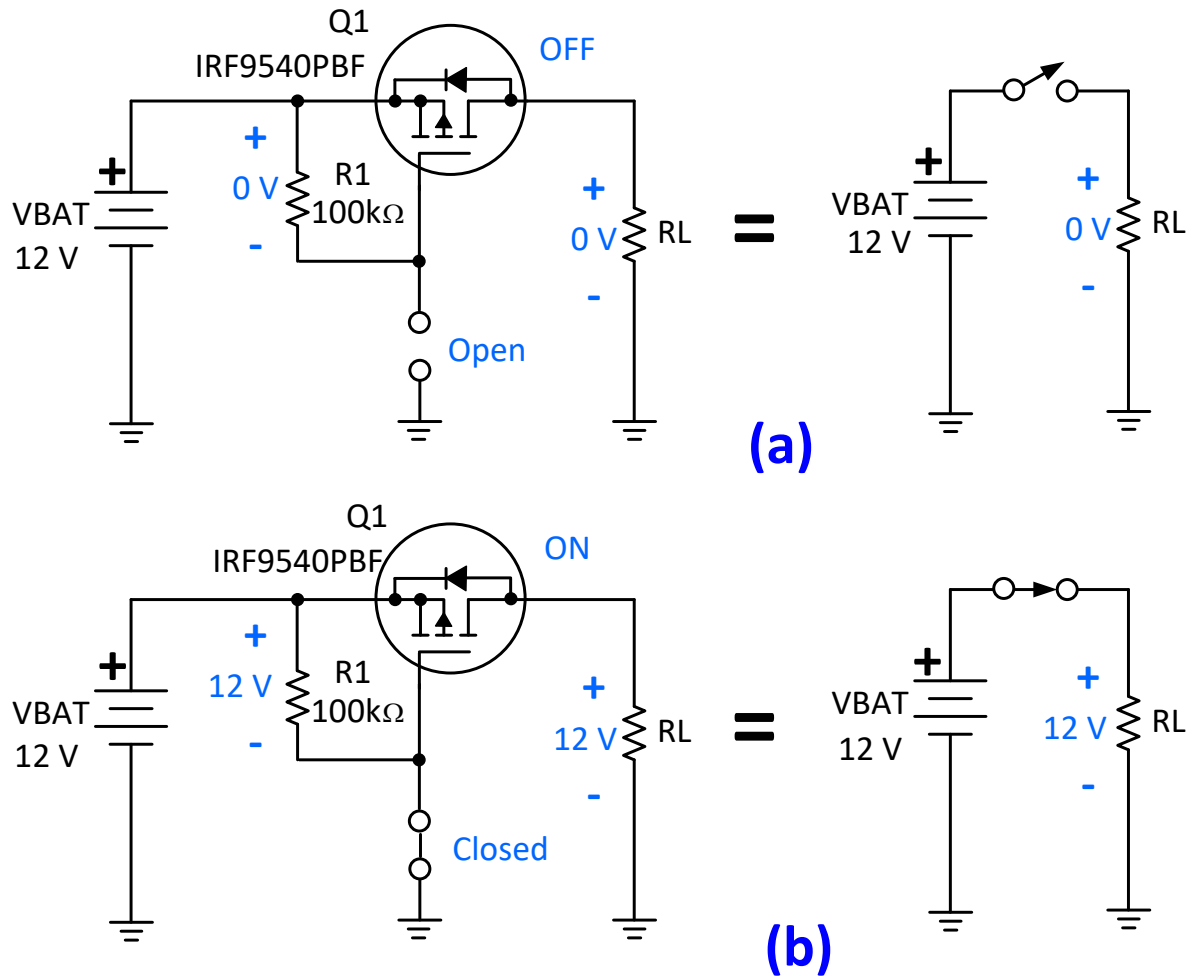


Figure 6-43.

The E-MOSFET can be controlled by a BJT (Q_2) as shown in Fig. 6-44. When the BJT is OFF the equivalent effect is the situation given in Fig. 6-42(a). When the BJT is ON the operation is equivalent to that shown in Fig. 6-42(b).

Resistor R_2 supports the latching action. When the E-MOSFET is in conduction the battery voltage will appear from the drain to ground. This provides the base current necessary to keep transistor Q_2 in saturation. More components are necessary to make the latch completely functional.

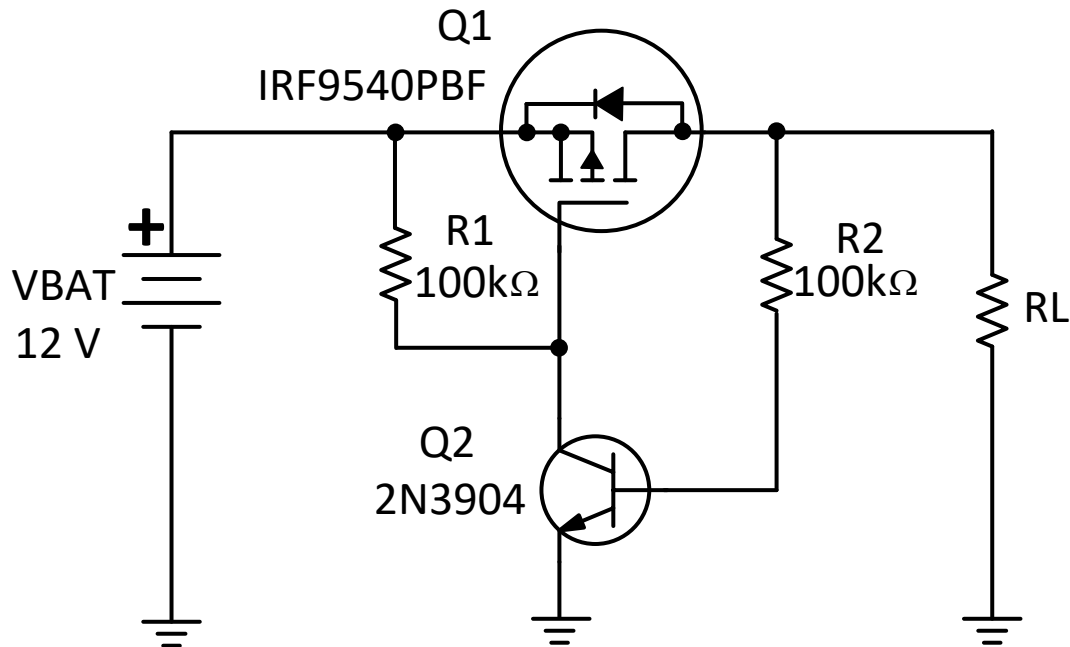


Figure 6-44.

When transistor Q_1 is ON, transistor Q_2 will be ON, which holds Q_1 ON. This is the latching action. Transistor Q_3 is necessary to control the circuit operation. Observe the transistor's collector resistor R_4 is connected to the battery voltage. This means its collector supply is present regardless of the condition of the E-MOSFET (Q_1). Its base terminal is connected via resistor R_3 to provide base current. The base current depends on the condition of the E-MOSFET.

Let's look at the operation of the circuit with the normally-open pushbutton (S_1) installed (see Fig. 6-45). Let's assume Q_1 is OFF. The voltage across R_L is zero. Both transistors Q_2 and Q_3 are OFF. The collector of Q_3 is pulled HI to 12 V.

If the pushbutton switch (S_1) is depressed, the base terminal of transistor Q_2 will receive forward bias through resistor R_4 . Transistor Q_2 will saturate and pull the gate terminal of Q_1 to ground. Transistor will turn ON and 12 V will appear across the load. This will cause transistor Q_2 will remain in saturation even after the pushbutton is released. The circuit is latched on.

The base of transistor Q_3 receives forward bias via resistor R_3 . It will be saturated. This means its collector will go to ground. If the pushbutton switch (S_1) is depressed again, the base of transistor Q_2 will be taken to ground. This causes transistor Q_1 to turn OFF and power is removed from the load. This condition will remain until the pushbutton switch (S_1) is depressed again. Hence, a single, low-cost pushbutton switch can control the on/off function of the system.

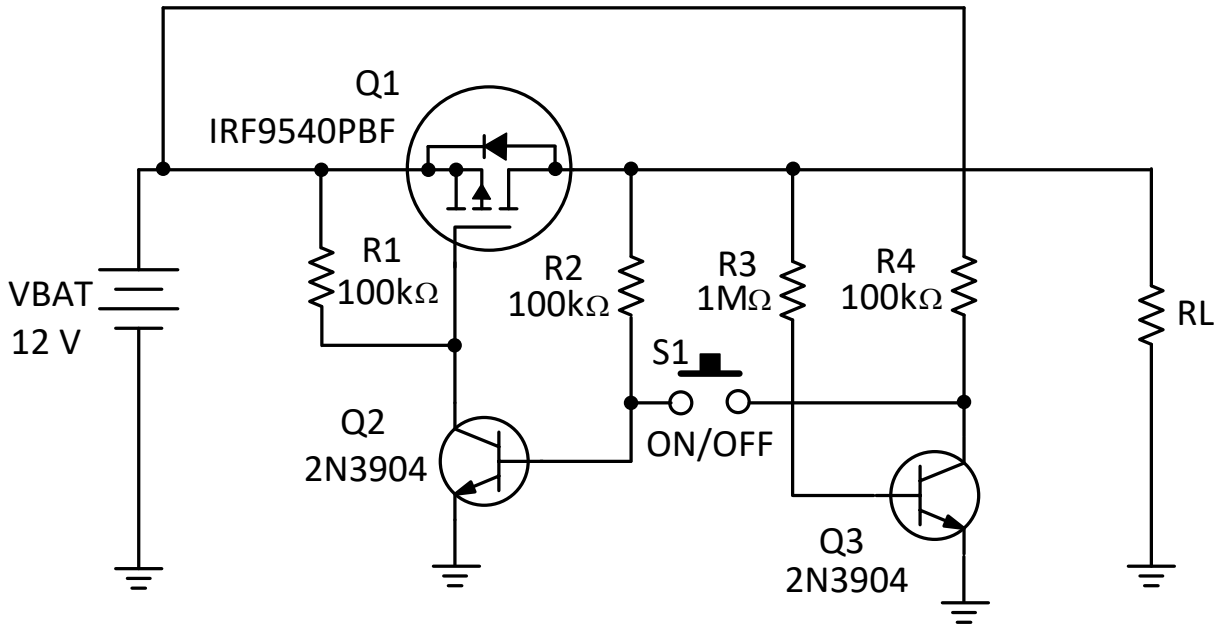


Figure 6-45.

To ensure reliable operation, two additional components. Resistor R_5 is added between the base-emitter of transistor Q_2 to make sure it turns OFF. Because mechanical switches exhibit contact bounce, capacitor C_1 is included. Without it, power to the load may switch between on and off very rapidly. The complete circuit is provided in Fig. 6-46.

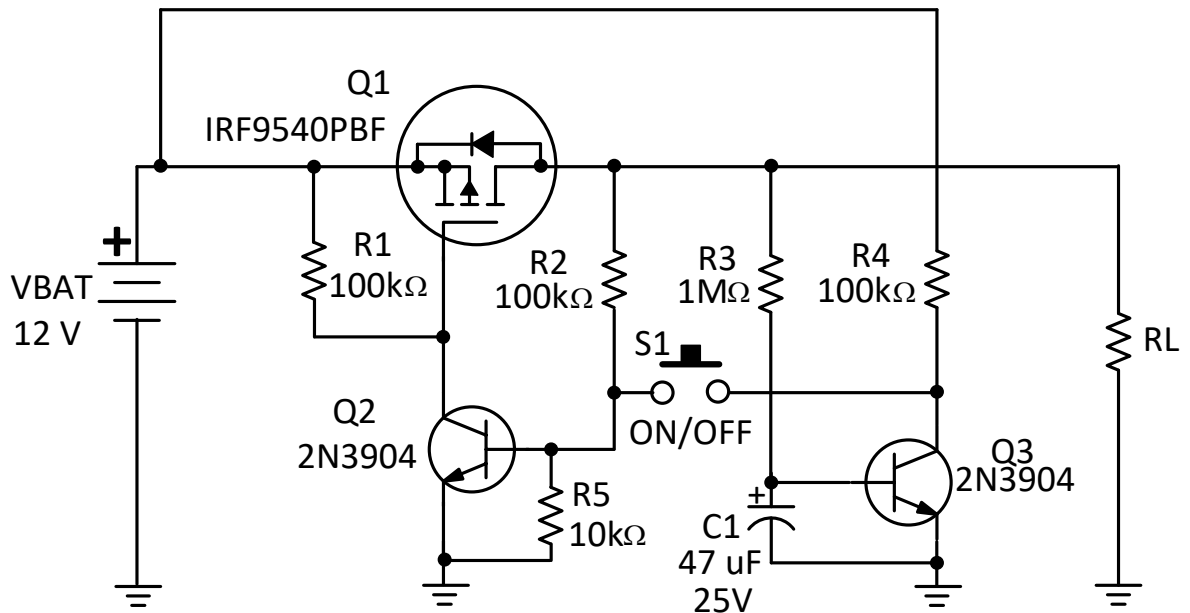


Figure 6-46.

6-11 Insulated Gate Bipolar Transistors (IGBTs)

Power electronics is covered in Chapter 15 found in Volume Three. Various power devices are examined in that chapter. However, this is a great opportunity to introduce the *insulated gate bipolar transistor (IGBT)*.

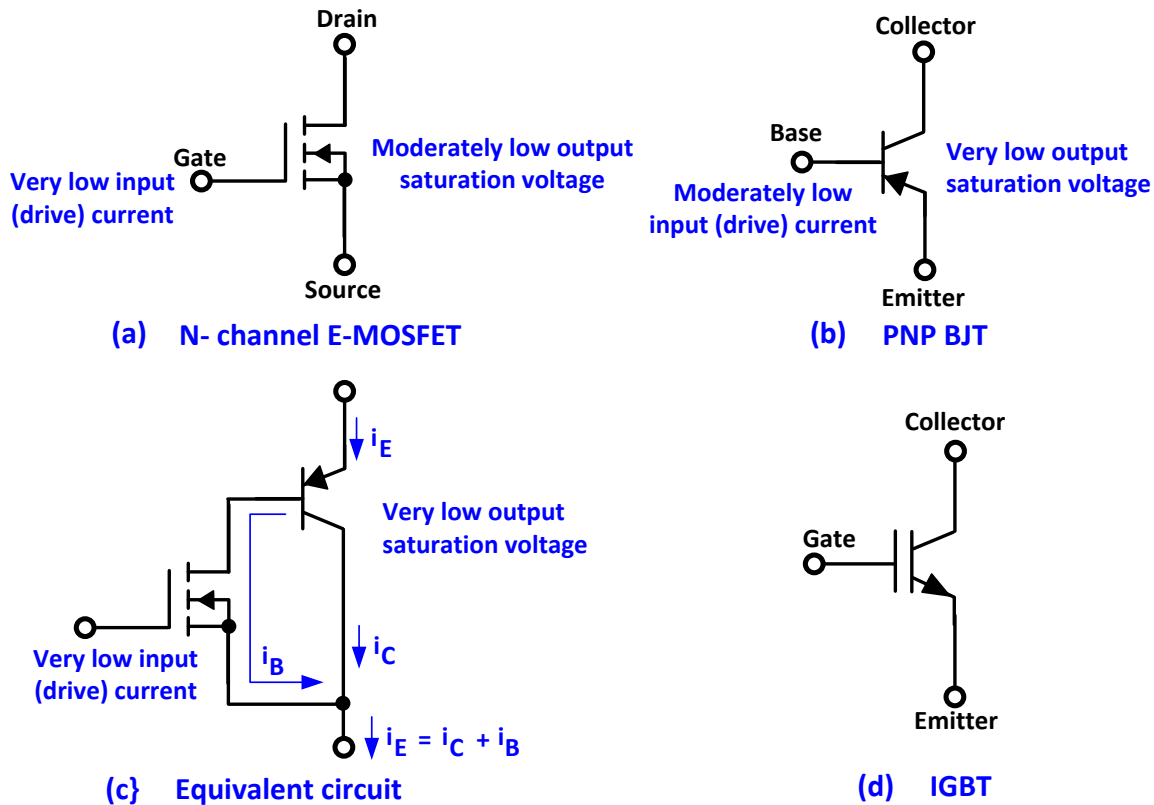


Figure 6-47.

Figure 6-47(a) shows an n-channel E-MOSFET. Two key characteristics here are its very low input current and its moderately low output saturation voltage. In Fig. 6-47(b) we have an npn BJT. The input current to a BJT is moderately low, but its output saturation voltage is very low. By combining the two devices as depicted in Fig. 6-47(c) the composite device captures the advantages of both devices. The composite device is the IGBT shown in Fig. 6-47(d). The IGBT has nearly zero gate current and otherwise behaves like an npn power transistor. As explained in Fig. 6-47(c) the IGBT collector current (i_C) is equal to its emitter current (i_E).

The IGBT can be used in analog applications like small-signal voltage amplifiers and the output stage of an analog audio power amplifier. However, it is favored as a high-frequency switching device in applications such as switching DC power supplies (Chapter 4), inverters (DC to AC conversion), and converters (DC to DC converters). DC to DC converters are used throughout industry. In aerospace converters are used to convert 270 VDC to 28 VDC. IGBTs can also be used in switching audio power amplifiers (Chapter 15 found in Volume Three).

Problems for Chapter 6

Drill Problems

Section 6-1

- 6-1 The n -channel JFET has _____ (n^+ , p^+) source and drain regions.
- 6-2 The p -channel JFET has _____ (n^+ , p^+) source and drain regions.
- 6-3 The n -channel JFET is like a(an) _____ (nnp , $pnnp$) BJT.
- 6-4 The p -channel JFET is like a(an) _____ (nnp , $pnnp$) BJT.

Section 6-2

- 6-5 The JFET operates in its *ohmic region* when V_{DG} is _____ (greater than, less than) the pinch-off voltage V_P .
- 6-6 The JFET operates in its *saturation region* when V_{DG} is _____ (greater than, less than) the pinch-off voltage V_P .
- 6-7 When the gate-to-source voltage of an n -channel JFET is made more negative, the drain current _____ (increases, decreases).
- 6-8 When a JFET is in its saturation region of operation, it behaves like a constant _____ (voltage, current) source.
- 6-9 An n -channel JFET has an I_{DSS} of 50 mA and a $V_{GS(OFF)}$ of -7 V. Assume that it is in pinch-off. What is its source terminal current (I_S) if V_{GS} is zero volts? What is its pinch-off voltage V_P ? Determine the minimum value of V_{DS} required to saturate the FET if V_{GS} is -3 V.
- 6-10 An n -channel JFET has an I_{DSS} of 25 mA and a $V_{GS(OFF)}$ of -12 V. Assume that it is in pinch-off. What is its source terminal current (I_S) if V_{GS} is zero volts? What is its pinch-off voltage V_P ? Determine the minimum value of V_{DS} required to saturate the FET if V_{GS} is -5 V.
- 6-11 An n -channel JFET has an I_{DSS} of 40 mA and a V_P of 15 V. What value of V_{GS} is required to place the JFET in cutoff?
- 6-12 An n -channel JFET has an I_{DSS} of 20 mA and a V_P of 5 V. What value of V_{GS} is required to place the JFET in cutoff?
- 6-13 The *drain* terminal of a JFET is like the _____ (base, emitter, collector) terminal of a BJT.
- 6-14 The *gate* terminal of a JFET is like the _____ (base, emitter, collector) terminal of a BJT.
- 6-15 The *source* terminal of a JFET is like the _____ (base, emitter, collector) terminal of a BJT.

Section 6-3

- 6-16 The _____ terminal serves as the input to a *common-drain* amplifier, while the _____ terminal serves as the output.
- 6-17 The _____ terminal serves as the input to a *common-source* amplifier, while the _____ terminal serves as the output.
- 6-18 The _____ terminal serves as the input to a *common-gate* amplifier, while the _____ terminal serves as the output.
- 6-19 The common-_____ (source, gate, drain) amplifier is like the *common-collector* (BJT) amplifier.
- 6-20 The common-_____ (source, gate, drain) amplifier is like the *common-emitter* (BJT) amplifier.
- 6-21 The common-_____ (source, gate, drain) amplifier is like the *common-base* (BJT) amplifier.
- 6-22 Modify the circuit shown in Fig. 6-21 to generate the drain characteristic curves for a *p-channel JFET*. Draw the schematic diagram neatly.
- 6-23 Modify the circuit shown in Fig. 6-22 to generate the transfer characteristic curve for a *p-channel JFET*. Draw the schematic diagram neatly.

Section 6-4

- 6-24 An *n*-channel JFET has an I_{DSS} of 50 mA and a $V_{GS(OFF)}$ of -12 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to 0 V, -4 V, -8 V, and -12 V.
- 6-25 An *n*-channel JFET has an I_{DSS} of 30 mA and a $V_{GS(OFF)}$ of -9 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to 0 V, -3 V, -6 V, and -9 V.
- 6-26 An *n*-channel JFET has an I_{DSS} of 50 mA and a $V_{GS(OFF)}$ of -12 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to $V_{GS(OFF)}/3.41$. What is significant about this value of $V_{GS(OFF)}$?
- 6-27 An *n*-channel JFET has an I_{DSS} of 30 mA and a $V_{GS(OFF)}$ of -9 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to $V_{GS(OFF)}/3.41$. What is significant about this value of $V_{GS(OFF)}$?

Section 6-5

- 6-28 When an *n*-channel JFET is *enhanced*, its V_{GS} is made _____ (positive, negative).
- 6-29 When a *p*-channel JFET is *enhanced*, its V_{GS} is made _____ (positive, negative).
- 6-30 An *n*-channel JFET has an I_{DSS} of 50 mA and a $V_{GS(OFF)}$ of -12 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to 0 V, 0.1V, and 0.2 V.
- 6-31 An *n*-channel JFET has an I_{DSS} of 30 mA and a $V_{GS(OFF)}$ of -9 V. Assume that it is in pinch-off. Find its drain current if V_{GS} is set equal to 0 V, 0.1V, and 0.2 V.

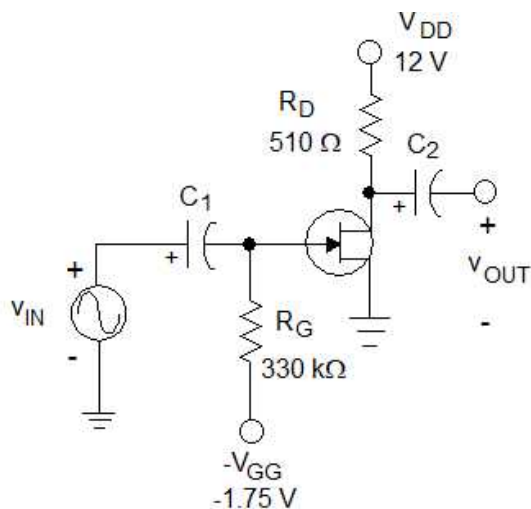
- 6-32 The *substrate connection* of a DE-MOSFET is normally connected to the FET's _____ (drain, source, gate) terminal.
- 6-33 The *substrate connection* of a DE-MOSFET can be used as another _____ (drain, source, gate) terminal.
- 6-34 An *n*-channel DE-MOSFET has an I_{DSS} of 60 mA, a $V_{GS(OFF)}$ of -3 V, and an $I_{D(MAX)}$ of 200 mA. Find its drain current if V_{GS} is set equal to -3 V, -2 V, -1 V, 0 V, 1 V, and 2 V. (Hint: Use Eq. 6-5.)
- 6-35 An *n*-channel DE-MOSFET has an I_{DSS} of 40 mA, a $V_{GS(OFF)}$ of -7 V, and an $I_{D(MAX)}$ of 100 mA. Find its drain current if V_{GS} is set equal to -7 V, -5 V, -3 V, 0 V, 1 V, and 3 V. (Hint: Use Eq. 6-5.)
- 6-36 Given the DE-MOSFET described in Prob. 6-34, determine the value of V_{GS} required to make $I_D = I_{D(MAX)}$. (Hint: Use algebra to solve Eq. 6-5 for V_{GS} .)
- 6-37 Given the DE-MOSFET described in Prob. 6-35, determine the value of V_{GS} required to make $I_D = I_{D(MAX)}$. (Hint: Use algebra to solve Eq. 6-5 for V_{GS} .)
- 6-38 Why are MOSFET devices shipped with shorting rings around their leads, or in conductive foam carriers? Explain briefly.
- 6-39 What does the acronym ESD indicate? What is meant by ESD handling precautions? Explain briefly.

Section 6-6

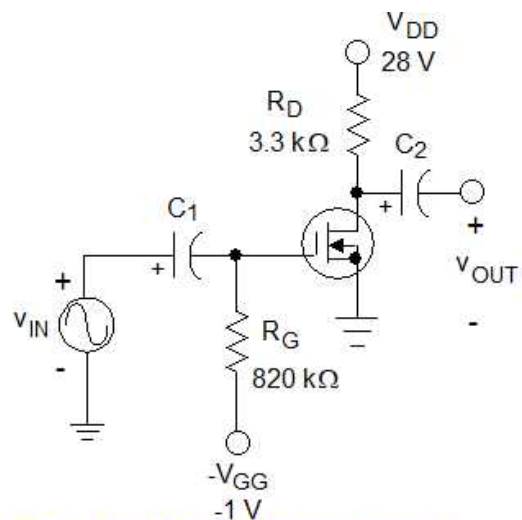
- 6-40 What is the key difference between the schematic symbol for an E-MOSFET and a DE-MOSFET?
- 6-41 The arrow employed in a *p*-channel E-MOSFET schematic symbol points _____ (toward, away from) the channel.
- 6-42 An *n*-channel E-MOSFET has a $V_{GS(th)}$ of 2.5 V, and an I_D of 40 mA when V_{GS} is 5 V. Determine its K and find its I_D when V_{GS} is 0 V, 4 V, and 6 V.
- 6-43 An *n*-channel E-MOSFET has a $V_{GS(th)}$ of 5 V, and an I_D of 60 mA when V_{GS} is 8 V. Determine its K and find its I_D when V_{GS} is 0 V, 6 V, and 10 V.

Section 6-7

- 6-44 Perform a DC analysis of the JFET common-source amplifier shown in Fig. 6-48(a). Assume that I_{DSS} is 25 mA and $V_{GS(OFF)}$ is -6 V. Find V_{GS} , I_D , I_S , and V_{DS} . Also, determine V_D , V_G , and V_S .
- 6-45 Perform a DC analysis of the DE-MOSFET common-source amplifier shown in Fig. 6-48(b). Assume that I_{DSS} is 4 mA and $V_{GS(OFF)}$ is -4 V. Find V_{GS} , I_D , I_S , and V_{DS} . Repeat the analysis if V_{GG} is *reversed*.
- 6-46 Find $I_{D(SAT)}$ and $V_{DS(OFF)}$ for the JFET circuit shown in Fig. 6-48(a).
- 6-47 Find $I_{D(SAT)}$ and $V_{DS(OFF)}$ for the DE-MOSFET circuit shown in Fig. 6-48(b).



(a) The circuit for even-numbered problems.



(b) The circuit for odd-numbered problems.

Figure 6-48.

- 6-48 Perform a DC analysis of the E-MOSFET common-source amplifier shown in Fig. 6-49. Assume that the E-MOSFET data includes $I_D = 10$ mA when $V_{GS} = 5$ V, and $V_{GS(th)} = 1.5$ V. Find V_{GS} , I_D , I_S , and V_{DS} . Also, determine V_D , V_G , and V_S .
- 6-49 Determine $I_{D(SAT)}$ and $V_{DS(OFF)}$ for the circuit given in Fig. 6-49.

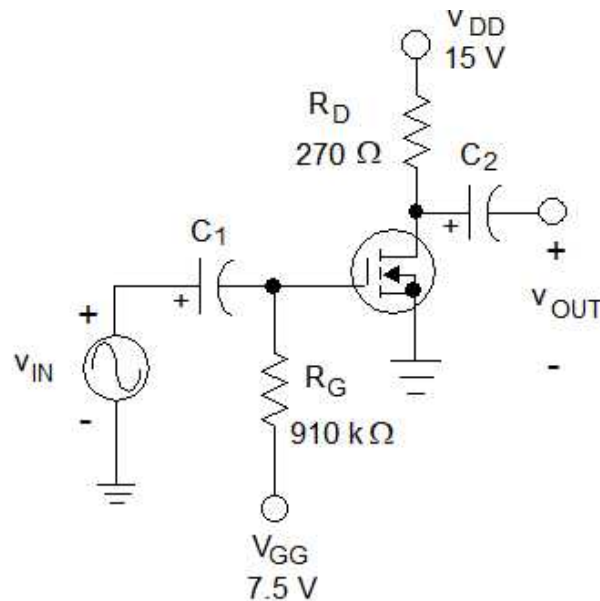


Figure 6-49.

Section 6-8

- 6-50 A common-source amplifier provides an output voltage signal that is _____ (in phase, 180° out of phase) with its input signal.

- 6-51 In general, an FET common-source amplifier provides a voltage gain (magnitude) that is _____ (larger, smaller) than that offered by BJT common-emitter amplifier.
- 6-52 A DC voltage source acts like a(an) _____ (open, short) to an ac signal. Explain your answer.

Section 6-9

- 6-53 The CMOS pair given in Fig. 6-38(a) has a V_{DD} of 3.3 V. Assume v_{IN} is equal to 3.3 V. Determine the gate-to-source voltage of Q_1 (v_{GS1}). Find the gate-to-source voltage of Q_2 (v_{GS2}). What is the approximate output voltage v_{OUT} ? Repeat the problem if v_{IN} is equal to 0 V.
- 6-54 The CMOS pair given in Fig. 6-38(a) has a V_{DD} of 6 V. Assume v_{IN} is equal to 6 V. Determine the gate-to-source voltage of Q_1 (v_{GS1}). Find the gate-to-source voltage of Q_2 (v_{GS2}). What is the approximate output voltage v_{OUT} ? Repeat the problem if v_{IN} is equal to 0 V.
- 6-55 When used as a linear amplifier, a CMOS pair behaves like a common- _____ (drain, gate, or source) amplifier.

Section 6-10

- 6-56 Explain the function of resistor R_I in Fig. 6-43(a).
- 6-57 Explain the purpose of capacitor C_I in Fig. 6-41.
- 6-58 Assume E-MOSFET Q_1 is OFF and the pushbutton S_1 is depressed. Calculate the current through resistor R_4 , the current through resistor R_5 (transistor Q_2 is silicon) and the base current flowing into transistor Q_2 .
- 6-59 Compute the voltage across capacitor C_I when it is fully charged.

Section 6-11

- 6-60 For what does the acronym IGBT stand?
- 6-61 The primary purpose of the IGBT is to serve as a(an) _____ (amplifier, switch).
- 6-62 What is the purpose of a converter?

Design Problems

- 6-63 An n -channel JFET has the following parameters: $I_{DSS} = 15$ mA, $V_{GS(OFF)} = -5$ V, and $I_{GSS} = 50$ nA. The JFET is to be used in a fixed-bias circuit such as the one indicated in Fig. 6-48(b). However, the drain supply V_{DD} is 15 V. Use the steps below to select values for the gate bias supply V_{GG} , the gate resistor R_G , and the drain resistor R_D .
- (a.) We want the drain current $I_D = I_{DSS}/2$. To accomplish this $V_{GS} = V_{GS(OFF)}/3.41$. Calculate the *target* values for I_D and V_{GS} .

- (b.) For the fixed gate bias circuit, $V_{GS} \cong -V_{GG}$. Select the nearest required value of $-V_{GG}$ from the following choices: -1 V, -1.5 V, -1.75 V, -2 V, or -2.5 V. Calculate the resulting I_D . (This serves as a “sanity check”, as well as providing us an expected value for I_D .)
- (c.) A (small) gate leakage current I_{GSS} flows out of the gate as shown in Fig. 6-33(b). We want the voltage drop it develops across the gate resistor to be negligibly small. Consequently, the gate resistor R_G should not be too large. Select the nearest 5% standard value. Use an internet search engine to find possible standard values.

$$R_G \leq \frac{0.01V_{GG}}{I_{GSS}} = \frac{V_{GG}}{100I_{GSS}}$$

- (d.) We would like $V_{DS} = V_{DD}/2$. This will center the DC operating point. This value of V_{DS} requires the voltage drop across the drain resistor R_D to be $V_{DD}/2$. Use the value of I_D determined in step (b.) to calculate the required value for R_D . Use the internet to select the nearest 5% tolerance standard resistor value.

$$R_D = \frac{V_{DD}/2}{I_D} = \frac{V_{DD}}{2I_D}$$

- (e.) As a final check, compute the expected value for V_{DS} using your selected value for R_D .

6-64 **Warning! This is an algebra problem.** It’s not too difficult. We can set I_D to $I_{DSS}/2$ by making $V_{GS} \cong V_{GS(OFF)}/3.41$. Derive this design requirement using the FET transfer equation Eq. 6-5. Show your work in systematic detail.

Troubleshooting Problems

- 6-65 In Example 6-4, the JFET bias circuit shown in Fig. 6-32(a) was analyzed. If the gate leakage current I_{GSS} is negligibly small, the gate-to-source voltage V_{GS} will be equal to -3 V. A common failure mode for a JFET is for its gate leakage current to increase. Determine the value of V_{GS} in Fig. 6-32(a) if I_{GSS} has increased to 2 μ A.
- 6-66 A power supply failure in Fig. 6-32(a) has made V_{GG} equal to 0 V. Calculate V_{GS} , V_G , I_D , V_{DS} , and V_D . The JFET data, provided in Example 6-4, is unchanged. Specifically, I_{DSS} is 30 mA and $V_{GS(OFF)}$ is -7 V.
- 6-67 A power supply failure in Fig. 6-32(a) has made V_{GG} equal to +3 V. Calculate V_{GS} , I_D , and V_{DS} . The JFET data, provided in Example 6-4, is unchanged. Specifically, I_{DSS} is 30 mA and $V_{GS(OFF)}$ is -7 V. If the JFET’s maximum gate current rating is 10 mA, should the JFET be replaced after the supply problem is corrected? Explain your answer.
- 6-68 Electrostatic discharge (ESD) has caused the DE-MOSFET in Fig. 6-33(a) to fail. Specifically, an internal short circuit has developed between its gate and source. An internal short circuit between its drain and source terminals has also been produced. Calculate V_{GS} , I_D , and V_{DS} . The DE-MOSFET data, provided in Example 6-5, is unchanged. Specifically, I_{DSS} is 30 mA, $V_{GS(OFF)}$ is -7 V, and $I_{D(MAX)}$ is 75 mA.

EDA Problems

- 6-69 Use Multisim to produce the transfer characteristic of the 2SK2553L *n*-channel E-MOSFET. The drain-to-source voltage V_{DS} is to be held constant at 15 V. V_{GS} is swept from 0 to 3 V in 0.25-V steps. Place text to label the schematic diagram “2SK2553L Transfer Characteristic”. Remember to place a current probe to monitor the drain current.
- 6-70 Use Multisim to produce the transfer characteristic of the 2N3823 *n*-channel JFET. The drain supply voltage V_{DD} is to be held constant at 15 V. V_{GS} is swept from -3 to 0 V in 0.25-V steps. Place text to label the schematic diagram “2N3821 Transfer Characteristic”. Remember to place a current probe to monitor the drain current.
- 6-71 Find the DC drain-to-ground voltage V_D using Multisim for the circuit given in Fig. 6-48(a). The JFET is a **2N5485**, the drain resistor R_D is changed to **1.8 k Ω** . The gate bias supply V_{GG} is changed to **0.704 V**. Everything else remains the same. The capacitors and the AC signal source are to be omitted.

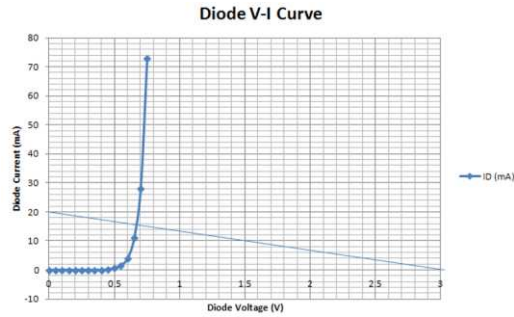
Answers to Selected Odd-Number Problems for Volume One

Chapter 1

1-1. Chemical, optical, mechanical, electrical, thermal, magnetic, acoustical, and nuclear; **1-3.** Yes, a loudspeaker is a transducer, electrical energy input and acoustical energy output; **1-5.** Electrons, protons; **1-7.** Metallic bonding, covalent bonding, and ionic bonding; metallic bonding occurs in electrical conductors; **1-9.** Decreased; **1-11.** A crystal (or crystalline solid) is a solid material whose constituents (such as atoms, molecules, or ions) are arranged in a highly ordered microscopic structure, forming a crystal lattice that extends in all directions; **1-13.** An electron volt is a unit of energy; it is the energy needed to raise a single electron through a potential difference of one volt, or 1.602×10^{-19} J; **1-15.** 0 eV; **1-17.** < 5 eV; **1-19.** Tetravalent; **1-21.** Silicon carbide; **1-23.** Intrinsic; **1-25.** Covalent; **1-27.** Gallium compounds have bandgaps wider than those for silicon because gallium compounds have both covalent and ionic bonding; **1-29.** Both (b) and (c); **1-31.** Same; **1-33.** Trivalent, *p*; **1-35.** Pentavalent, *n*; **1-37.** Electrons, holes; **1-39.** Modern chemistry defines carbon compounds to be organic; carbon can be used as an organic semiconductor; **1-41.** Amorphous and crystalline; **1-43.** Crystalline; **1-45.** Graphite and diamond; **1-47.** Thin, excellent, strong; **1-49.** Diffusion is the process by which mixtures of easily flowing materials naturally reach a final blend that is uniform in concentration; **1-51.** Barrier potential results from the ionization that occurs at the *p-n* junction; germanium is 0.3 V, silicon is 0.7 V and the gallium compounds range from 1.2 to 1.9 V; **1-53.** Negative, positive; **1-55.** *N* regions have an abundance of electrons so if a minority carrier hole is formed, it is quickly neutralized; *P* regions have an abundance of holes so if a minority carrier electron is formed, it is quickly neutralized; **1-57.** Diffusion current results when a concentration of either holes or electrons is formed because the like charge carriers tend to move away from one another, and charge carrier movement is called a current; **1-59.** Forward bias of a *p-n* junction results when the *p* material is more positive than the *n* material; **1-61.** Recombination occurs when an electron annihilates a hole; **1-63.** Decreases; **1-65.** Away from; **1-67.** Large; **1-69.** Reverse saturation; **1-71.** 3.5 nA; **1-73.** Cathode; **1-75.** *P*-type.

Chapter 2

2-1. Decreases; **2-3.** 0.7 V; **2-5.** 1.6 V; **2-7.** 8.05 mA; **2-9.** 14 V; **2-11.** At $V_D = 0.7$ V, $I_D = 24.6$ mA; **2-13.** Hint: Use Excel to graph the data provided, add major and minor gridlines, and insert a straight-line shape; the endpoints should be at 3 V (V_{oc}) and 20 mA (I_{SH}). $I_D = 15.5$ mA and $V_D = 0.68$ V;

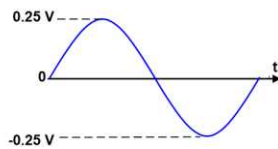


2-15. $V_D = 0$ V, $I_D = 12$ mA; **2-17.** $V_R = 12$ V, $I_R = 0$; **2-19.** $V_D = 0.7$ V, $I_D = 8.1$ mA;
2-21. $V_D = 0.3$ V, $I_D = 8.23$ mA; **2-23.** $V_D = 0.1$ V, $I_D = 0$; **2-25.** $V_R = 19.77$ V; **2-27.** p^+ ;
2-29. p^- ; **2-31.** Greater than, positive; **2-33.** $V_Z = 15$ V, $I_Z = 5$ mA; **2-35.** $V_Z = 12$ V, $I_Z = 0$;
2-37. $V_D = 0.7$ V, $I_D = 4.11$ mA; **2-39.** $R_{DC} = 70\ \Omega$ @ 20 mA, $R_{DC} = 34.3\ \Omega$ @ 70 mA, $r_Z = 20\ \Omega$;
2-41. $V_{Z0} = 1.9$ V, $r_Z = 30\ \Omega$, $V_Z = 3.1$ V @ $I_Z = 40$ mA; **2-43.** $I_Z = 7.129$ mA $\cong 7.13$ mA,
 $V_Z = 14.87$ V $\cong 14.9$ V; **2-45.** $R_{TH} = 3.377$ k Ω $\cong 3.38$ k Ω , $V_{TH} = 7.947$ V $\cong 7.95$ V, $V_D = 0.7$ V,
 $I_D = 2.146$ mA $\cong 2.15$ mA; **2-47.** $R_{TH} = 5.2$ k Ω , $V_{TH} = 17.0$ V, $V_D = 0.7$ V, $I_D = 3.13$ mA;
2-49. $R_{TH} = 2.75$ k Ω , $V_{TH} = 10$ V, $V_Z = 4.7$ V, $I_Z = 1.93$ mA.

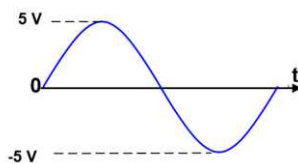
Chapter 3

3-1. An amplifier should take small voltage signals and increase their amplitude without altering their shape, the amplifier's input should act like an open circuit; **3-3.** Answer (e) both b and c;

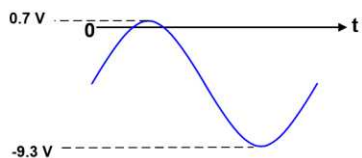
3-5.



3-7.

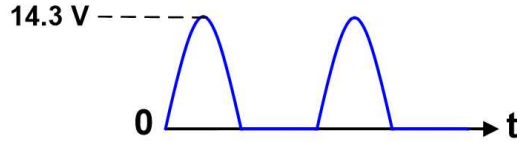


3-9. DC level = -4.3 V



3-11. Negative; **3-13.** $V_D(65^\circ\text{C}) = 0.24$ V, $V_D(20^\circ\text{C}) = 0.33$ V; **3-15.** $I_S(55^\circ\text{C}) = 16$ nA,
 $I_S(5^\circ\text{C}) = 0.5$ nA = 500 pA; **3-17.** Below; **3-19.** Negative; **3-21.** The voltage across the un-tripped

device $V_{UT} = 1.5 \text{ mV}$, while protecting the voltage across the device $V_{PTC} = 24 \text{ V}$, the current is limited $I_{LIM} = 104.2 \text{ mA}$, and the tripped resistance $R_T = 230.4 \Omega$; **3-23.** Zener diodes; **3-25.** $I_D = 14.4 \text{ mA}$; **3-27.** Peak laser diode current = 1.3 A ; **3-29.** Decreases; **3-31.** 3.42 V ; **3-33.**

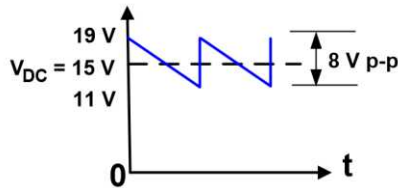


3-35. To turn off; **3-37.** Diffusion capacitance; **3-39.** Schottky barrier; **3-41.** $I_D = 1.41 \text{ mA}$; **3-43.** Increase; **3-45.** Reverse.

Chapter 4

4-1. (b) – heavier and simpler; **4-3.** $I_L = 1425 \text{ mA} = 1.425 \text{ A}$, $R_L = 15.44 \Omega$, $P_L = 31.35 \text{ W}$; **4-5.** Hot (black), neutral (white), and ground (green or bare); **4-7.** If the chassis is double insulated in portable equipment, no ground connection is required, but a polarized plug is required;

4-9.

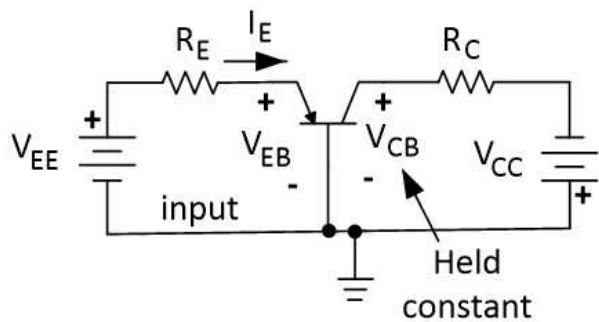


4-11. $V_{DC} = 4.77 \text{ V}$; **4-13.** $V_{DC} = 9.55 \text{ V}$; **4-15.** $V_{DC} = 0 \text{ V}$, $V_{RMS} = 8.49 \text{ V}$; **4-17.** $V_{DC} = 0 \text{ V}$, $V_{RMS} = 18 \text{ V}$; **4-19.** $V_m = 1 \text{ V}$, $V_{DC} = 0 \text{ V}$, $V_{RMS} = 0.577 \text{ V}$; **4-21.** $V_{DC} = 3.82$, $V_{RMS} = 6 \text{ V}$; **4-23.** $V_{DC} = 7.64 \text{ V}$, $V_{RMS} = 8.49 \text{ V}$; **4-25.** $N_2/N_1 = 0.0525$, $I_2 = 0.63 \text{ A rms}$, $I_1 = (N_2/N_1)I_2 = 33.075 \text{ mA rms}$, $P_{in} = P_{out} = 3.969 \text{ W}$; **4-27.** VA rating = 6.05 VA , %VR = 25%, $V_{FL} = 7.88 \text{ Vrms}$; **4-29.** $V_m = 56.6 \text{ V}$, $V_{dcm} = 55.9 \text{ V}$, $V_{DC} = 17.8 \text{ V}$, $V_{RM} = 56.6 \text{ V}$, $I_m = 559 \text{ mA}$, $I_{DC} = 178 \text{ mA}$, $I_{D(AV)} = 178 \text{ mA}$; **4-31.** $V_m = 19.8 \text{ V}$, $V_{dcm} = 19.1 \text{ V}$, $V_{DC} = 12.2 \text{ V}$, $V_{RM} = 38.9 \text{ V}$, $I_m = 191 \text{ mA}$, $I_{DC} = 122 \text{ mA}$, $I_{D(AV)} = 60.8 \text{ mA}$; **4-33.** $V_m = 17.8 \text{ V}$, $V_{dcm} = 16.4 \text{ V}$, $V_{DC} = 10.5 \text{ V}$, $V_{RM} = 17.1 \text{ V}$, $I_m = 547 \text{ mA}$, $I_{DC} = 348 \text{ mA}$, $I_{D(AV)} = 174 \text{ mA}$; **4-35.** $V_m = 19.8 \text{ V}$, $V_{dcm} = 19.1 \text{ V}$, $V_{DC} = 12.2 \text{ V}$, $V_{RM} = 38.9 \text{ V}$, $I_m = 318 \text{ mA}$, $I_{DC} = 203 \text{ mA}$, $I_{D(AV)} = 101 \text{ mA}$, $-V_{DC} = -12.2 \text{ V}$ (the lower load voltage relative to ground); **4-37.** Parallel; **4-39.** The key advantage provided by electrolytic capacitors is they offer large capacitance values for a relatively small physical size when compared to other types of capacitors; **4-41.** Aluminum and tantalum are the two types of electrolytic capacitors, aluminum electrolytic capacitors offer the higher voltage ratings; **4-43.** $WVDC_{(min)} = 36.6 \text{ V}$, a standard rating of 50 V should be used; **4-45.** $V_{dc(min)} = 16.5 \text{ V}$, $V_{DC} = 17.3 \text{ V}$; **4-47.** Increased; **4-49.** $V_{dc(min)} = 22.5 \text{ V}$, $V_{DC} = 23.75 \text{ V}$, $V_{r(rms)} = 0.722 \text{ Vrms}$, %r = 3.04%, $WVDC \geq 30 \text{ V}$;

4-51. 0%; 4-53. $V_{dc(min)} = 9.04$ V; 4-55. $V_{r(p-p)} = 1.25$ Vp-p; 4-55; 4-57. $V_m = 25.5$ V, $V_{dcm} = 24.8$ V, $V_{r(p-p)} = 4.08$ Vp-p, $V_{dc(min)} = 20.7$ V, $V_{DC} = 22.7$ V, $V_{r(rms)} = 1.18$ Vrms, $\%r = 5.14\%$, $WVDC \geq 29.7$ V; 4-59. $V_m = 35.6$ V, $V_{dcm} = 34.2$ V, $V_{r(p-p)} = 3.33$ Vp-p, $V_{dc(min)} = 30.9$ V, $V_{DC} = 32.6$ V, $V_{r(rms)} = 0.962$ Vrms, $\%r = 2.95\%$, $WVDC \geq 41.1$ V; 4-61. $V_m = 17.8$ V, $V_{dcm} = 17.1$ V, $V_{r(p-p)} = 2.66$ Vp-p, $V_{dc(min)} = 14.5$ V, $V_{DC} = 15.8$ V, $V_{r(rms)} = 0.768$ Vrms, $\%r = 4.86\%$, $WVDC \geq 20.5$ V, we have light loading since $V_{DC} = 15.8$ V exceeds the required minimum of 15.4 V; the voltage across the bottom load is -15.8 V; 4-63. Decreases, increases; 4-65. $I_{D(AV)} = 150$ mA, $I_o \geq 180$ mA, $t_c = 0.6976$ ms, $I_{D(PK)} = 7.17$ A, $I_{D(PK)}/I_{D(AV)} = 47.8$; 4-67. $R_S = 0.35$ Ω , $I_{D(SURGE)} = 141$ A; 4-69. $I_{r(rms)} = 751$ mArms; 4-71. $I_2 \geq 1.65$ Arms; 4-73. Axial leads protrude out the ends of a (usually cylindrical or rectangular) component. Radial leads lie on a radius and usually exit from the bottom of a cylindrical or rectangular component; 4-75. Decreases; 4-77. $V_{dc(min)} \geq 15.5$ V.

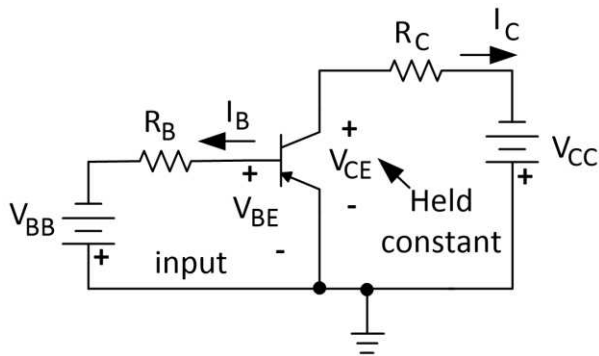
Chapter 5

5-1. The arrow points to the n material; 5-3. Base region; 5-5. False; 5-7. Pentavalent, electrons, n -; 5-9. Negative; 5-11. False; 5-13. Forward, reverse; 5-15. The base region is thin and lightly doped relative to the emitter region; 5-17. $I_B = 50$ μ A; 5-19. $V_{EB} = 0.4$ V; 5-21. I_B , I_E , and V_{BE} ; 5-23. Base, emitter; 5-25. Base, collector; 5-27. $I_C = 3$ mA, $I_E = 3.02$ mA, $\alpha_{DC} = 0.993$; 5-29. $I_E = 2.04$ mA, $I_B = 40.8$ μ A, $\beta_{DC} = 49$; 5-31. $I_C = 2.479$ mA; 5-33. $I_C = 1.495525$ mA, I_{CBO} is only 0.000025 mA and is therefore negligible; 5-35. $I_{CEO} = 1.005$ μ A; 5-37. $I_C = 3.0001$ mA, I_{CEO} is negligibly small; 5-39. Increase; 5-41. 200 mA; 5-43. Active; 5-45. Saturation; 5-47. Reverse, reverse; 5-49.



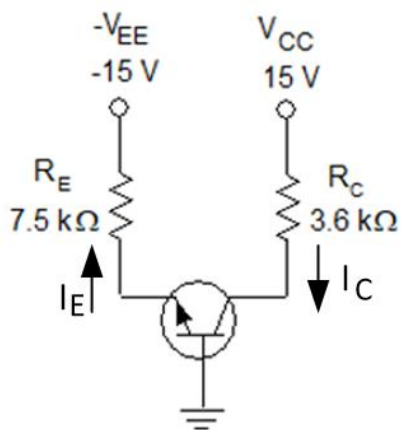
V_{EB} and I_E will have positive values while V_{CB} will have negative values.

5-51.

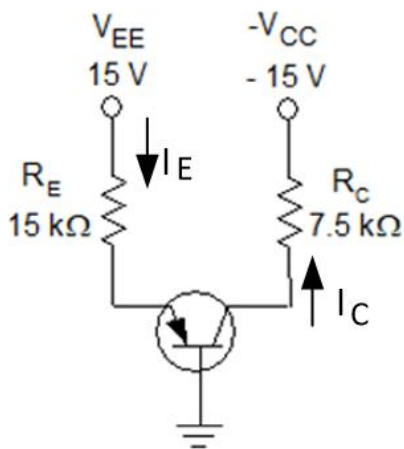


I_B , V_{BE} and V_{CE} will have negative values.

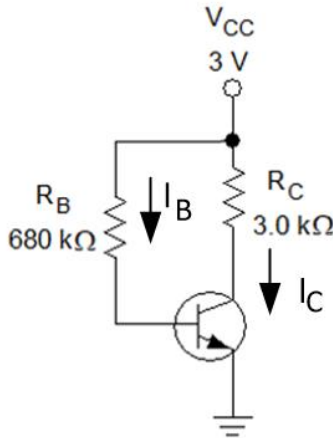
5-53. $I_E = 1.91 \text{ mA}$, $I_C = 1.89 \text{ mA}$, $V_{CB} = 8.20 \text{ V}$, $I_{C(\text{SAT})} = 4.17 \text{ mA}$, $V_{CB(\text{OFF})} = 15 \text{ V}$;



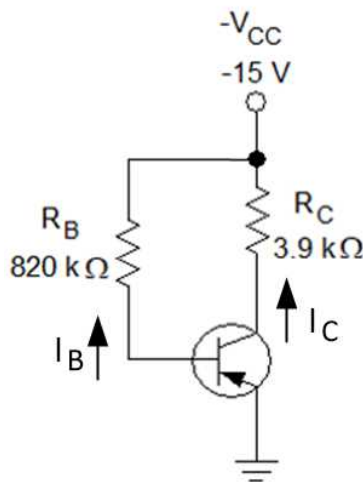
5-55. $I_E = 0.953 \text{ mA}$, $I_C = 0.906 \text{ mA}$, $V_{CB} = -8.21 \text{ V}$, $I_{C(\text{SAT})} = 2 \text{ mA}$, $V_{CB(\text{OFF})} = -15 \text{ V}$



5-57. $I_B = 3.38 \mu\text{A}$, $I_C = 0.507 \text{ mA}$, $V_{CE} = 1.48 \text{ V}$, $V_{CB} = 0.778 \text{ V}$, $I_{C(\text{SAT})} = 1 \text{ mA}$, $V_{CE(\text{OFF})} = 3 \text{ V}$



5-59. $I_B = 12.8 \mu\text{A}$, $I_C = 1.41 \text{ mA}$, $V_{CE} = -9.51 \text{ V}$, $V_{CB} = -8.81 \text{ V}$, $I_{C(\text{SAT})} = 3.85 \text{ mA}$, $V_{CE(\text{OFF})} = -15 \text{ V}$

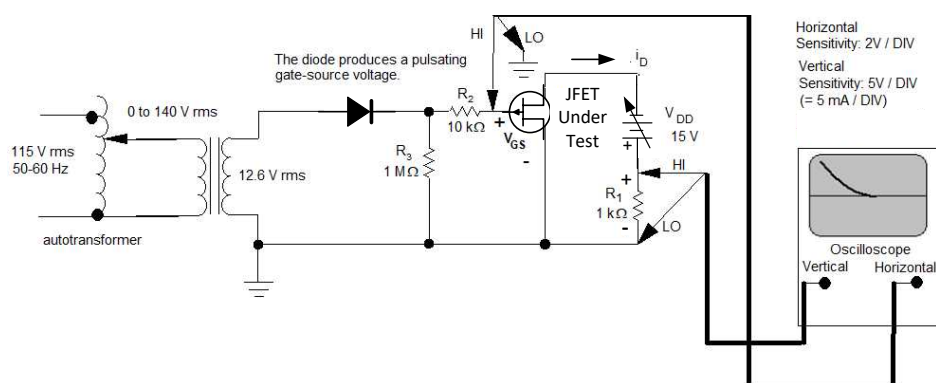


5-61. Inversely; **5-63.** $A_v = 25 \angle -180^\circ$; **5-65.** $I_B = 535 \mu\text{A}$, $I_{C(\text{SAT})} = 2.8 \text{ mA}$, $\beta_F = 5.23$; **5-67.**

Analog signals can have an infinite number of possible values between two finite limits. Digital signals have a finite number of possible values between two finite limits; **5-69.** The diode limits negative transients and is called a free-wheeling diode; **5-71.** Point C is LO, Point B is HI, Point A is LO, the LED is extinguished, and the DC motor will not be running; **5-73.** R_C works out to be 1250Ω so either $1.2 \text{ k}\Omega$ or $1.3 \text{ k}\Omega$ standard values can be used, but $1.3 \text{ k}\Omega$ works slightly better, R_E work out to be 2150Ω so a standard value of $2.2 \text{ k}\Omega$ should be selected; **5-75.** R_C is $10 \text{ k}\Omega$ which a standard value, R_B works out to be $2.58 \text{ M}\Omega$ so use a standard value of $2.5 \text{ M}\Omega$; **5-77.** $R_C = 2 \text{ k}\Omega$ (a standard value), $R_B = 17.2 \text{ k}\Omega$, use $18 \text{ k}\Omega$; **5-79.** Run; **5-81.** The motor will run continuously; **5-83.** (b) tie the base of transistor Q2 to ground if we tie point B to V_{CC} , transistor Q2 could be damaged if it starts conducting.

Chapter 6

6-1. p^+ ; **6-3.** npn; **6-5.** Less than; **6-7.** Decrease; **6-9.** The source current $I_S = 50 \text{ mA}$, $V_P = 7 \text{ V}$, to saturate the JFET, $V_{DS} = V_P + V_{GS} = 7 \text{ V} + (-3 \text{ V}) = 4 \text{ V}$; **6-11.** $V_{GS(\text{OFF})} = -V_P = -15 \text{ V}$; **6-13.** The drain terminal of a JFET is like the collector terminal of a BJT; **6-15.** The source terminal of a JFET is like the emitter terminal of a BJT; **6-17.** The gate terminal serves as the input to a common-source amplifier, while the drain terminal serves as the output; **6-19.** The common-drain amplifier is like the common-collector (BJT) amplifier; **6-21.** The common-gate amplifier is like the common-base (BJT) amplifier; **6-23.** The diode is reversed to supply positive pulses for v_{GS} . The drain supply is also reversed. The setup will produce the transfer characteristic in the first quadrant. The drain current is negative according to the transistor convention.



V_{GS}	I_D
0 V	30 mA
-3 V	13.3 mA
-6 V	10 mA
-9 V	0 mA

6-25.

6-27. $V_{GS} = -2.639 \text{ V}$, $I_D = 15 \text{ mA}$, that value of V_{GS} makes $I_D = I_{DSS}/2$; **6-29.** When a p -channel JFET is enhanced, its V_{GS} is made negative;

V_{GS}	I_D
0 V	30 mA
0.1 V	30.7 mA
0.2 V	31.3 mA

6-31.

Enhancement causes the drain current to increase beyond I_{DSS} . The same square law equation is used.

6-33. The *substrate connection* of a DE-MOSFET can be used as another gate terminal;

V_{GS}	I_D
-7 V	0 mA
-5 V	3.27 mA
-3 V	13.1 mA
0 V	40 mA
1 V	52.2 mA
3 V	81.6 mA

6-35.

6-37. $V_{GS} = 4.068$ V; **6-39.** ESD stands for Electrostatic Discharge, ESD handling is used to protect electronic components from damage by receiving a static discharge, shorting rings around terminals, conductive foam, conductive tubes, conductive trays, static straps are used to make sure engineers and technicians are grounded properly, work stations must also grounded properly; **6-41.** The arrow employed in a *p*-channel E-MOSFET schematic symbol points away from the channel;

6-43. $K = 1.983$ mA/V²

V_{GS}	I_D
0 V	0 mA
6 V	24.3 mA
10 V	111.5 mA

6-45. For $-V_{GG} = -1$ V, $V_{GS} = -1$ V, $I_D = I_S = 2.25$ mA, $V_{DS} = 20.6$ V for $V_{GG} = 1$ V, $V_{GS} = 1$ V, $I_D = I_S = 6.25$ mA, $V_{DS} = 7.38$ V; **6-47.** $I_{D(SAT)} = 8.48$ mA, $V_{DS(OFF)} = 28$ V; **6-49.** $I_{D(SAT)} = 55.6$ mA, $V_{DS(OFF)} = 15$ V; **6-51.** In general, an FET common-source amplifier provides a voltage gain (magnitude) that is smaller than that offered by BJT common-emitter amplifier; **6-53.** For $v_{IN} = 3.3$ V, $v_{GS1} = 0$ V, $v_{GS2} = 3.3$ V, Q1 is OFF, Q2 is ON, v_{OUT} is about 0 V and for $v_{IN} = 0$ V, $v_{GS1} = -3.3$ V, $v_{GS2} = 0$ V, Q1 is ON, Q2 is OFF, v_{OUT} is about 3.3 V; **6-55.** When used as a linear amplifier, a CMOS pair behaves like a common-source amplifier; **6-57.** Capacitor C1 is a DC blocking capacitor and is also called an AC coupling capacitor; **6-59.** Capacitor C1 will charge through the gate resistor R_G to 2.5 V with its right end positive – remember the average value of a sine wave is zero; **6-61.** The primary purpose of the IGBT is to serve as a switch; **6-63. (a.)** $V_{GS} = -1.47$ V, $I_D = 7.492$ mA, **(b.)** $-V_{GG} = -1.5$ V, $I_D = 7.35$ mA, **(c.)** $R_G = 300$ k Ω which is standard 5% tolerance resistor value, **(d.)** $V_{DS} = 7.5$ V, $R_D = 1.02$ k Ω and 1 k Ω is standard 5% tolerance resistor value, and **(e.)** using $I_D = 7.35$ mA and $R_D = 1$ k Ω , $V_{DS} = 7.65$ V which is only about 2% higher than our design target of 7.5 V; **6-65.** $V_{GS} = -2.56$ V; **6-67.** $V_{GS} = +3$ V (enhancement bis), I_D will try to go to 61.2 mA, the circuit is in saturation and $V_{DS} = 0$ V, the gate resistor limits the gate current to 10.5 μ A, which is far below the 10-mA maximum. The JFET should be fine.

Index to Volume One

A

AC, 177 - 178
Acceptor impurities, 19
Active device, 272
Active region, BJT, 288 – 289, 293
Active region, FET, (*See* pinch-off.)
Allotropes, 22
Allotropes, carbon, 22
Alpha (α_{DC}), BJT DC current gain, 280
Amorphous, silicon, 22
Amplifier, BJT, 306 - 310
Analog signal, (*See* signals, analog versus digital)
Anode, rectifier diode, 44
ANSI, American National Standards Institute, 351
Atom, 4
Autotransformer, 349
 A_v , (*See* gain, voltage)
Avalanche breakdown, 79 - 80
Average value, definition, 178 - 184
Average value, various waveforms, 186
Axial leads, 243

B

Bandgap, 10-11
Barrier potential, 35
Base width, effective, 272
Beta (β_{DC}), BJT DC current gain, 280
Biased clipper, 106 - 109

Bilateral device, 121
Bipolar Junction Transistor (BJT), 269
Bulk resistance, semiconductor, 83

C

Cadmium selenide (CdSe), 12, 138
Cadmium sulfide (CdS), 12, 138
Capacitance, diffusion, 154
Capacitance, junction, 156 – 157
Capacitor, coupling, (*See* Capacitor, DC blocking.)
Capacitor, DC blocking, 306
Capacitor, electrolytic, 216 - 218
Capacitor, filter, 215 – 217
Capacitor, ripple current, 238 - 240
Carbon, 22
Carbon nanotubes, 24 - 26
Cathode, rectifier diode, 44
Clamper, 109 - 110
Clipper, 105 – 106
Clipper, biased, 106 – 109
Clipping, 290
CMOS, complementary metal oxide semiconductors, 376
Collector region, BJT, 277 - 278
COMETMAN, 3
Common base (BJT), 279
Common base input curves, 287
Common base output curves, 288
Common collector (BJT), 279
Common drain (FET), 347

Common emitter (BJT), 279
 Common emitter input curves, 290
 Common emitter output curves, 291
 Common gate (FET), 347
 Common source (FET), 347
 Common source (FET) V-I curves, 349
 Conduction energy band, 8
 Contact resistance, 83
 Copper, 4-5,
 Covalent bonding, 13-14
 Crystals, 8
 Crystal lattice, 13
 Current probe, clamp-on, 237 - 238
 Current source, 77
 Cutoff region, BJT, 288 – 289, 292
 Cutoff, BJT circuit, (*See* Switch, BJT.)
 Cutoff, FET, (*See* $V_{GS(OFF)}$.)
 Cutoff FET circuit, (*See* Switch, FET.)

D

DC, 177, (and *See* average value.)
 DC load line, BJT, 300
 DC load line, diode, 67 - 69
 DE-MOSFET, 356
 Depletion mode, FET, 356
 Depletion region, rectifier diode, 29
 Depletion region, Schottky diode, 155
 Diffusion, 28
 Diffusion current, 31

Digital signal, (*See* signals, analog versus digital)
 Diode, 44
 Donor impurities, 20
 Doping level, 78 – 80, 272
 Drain, FET, 334 - 335
 Drift current, 31
 Dropout voltage, (*See* $V_{DROPOUT}$.)
 Dual complementary full-wave rectifier, 213 - 215
 Dynamic resistance, 85

E

EDA, Electronic Design Automation, 57
 Effective base region, 272
 Effective value, (*See* root mean square.)
 Electric field intensity, 78 - 79
 Electrons, 1
 Electron volt (eV), 10
 Electron volt (eV) Table
 Electronics, 1
 EMI filter, **E**lectro-**M**agnetic **I**nterference filter, 173
 E-MOSFET, 361 - 362
 Energy bands, 8-9
 Energy diagram, forward bias, 38 – 39
 Energy diagram, reverse bias, 40 - 41
 Energy levels, 6-7,
 Enhancement mode, FET, 356
 ESD, (Electrostatic Discharge), 360

Extrinsic (doped) semiconductors, 19

F

Field Effect, 332, 359

FET transfer equation, 354

FET/BJT comparison, 336, 345, 347

Filter, simple capacitor, 218 - 221

Floating input, 313

Floating source, 349

Forbidden region, 10

Forced Beta (β_F), 312

Forward bias, diode, 35 - 38

Forward biased gate, FET, 356 - 357

Free electrons, 8 - 9, 15

Free-wheeling diode, 315

Full-wave rectifier using a CT transformer, 202 - 207

Full-wave rectifier using a full wave bridge (FWB), 207 - 211, 213

G

Gain, voltage, (A_V), 310, 375 - 376

Gallium compounds, 13

Gate, FET, 334 - 335

Germanium, 11 - 12

Graphene, 22 - 23

Ground, earth, 175

H

Half-wave rectifier, 150 - 152, 192, 196 - 200

Hole, 16 - 18

Hole flow, 16 - 18

Heterojunctions, 12

Hot carrier, 154

Hot wire, 175 - 176

I

I_B , base current, 275

I_C , collector current, 275

I_{CBO} , 283 - 284

I_{CEO} , 284 - 285

$I_{C(SAT)}$, (See switch, BJT.)

I_D , FET, drain current, 343

$I_{D(AV)}$, average diode forward current, 229 - 230

I_{DC} , 198

$I_{D(MAX)}$, DE- or E-MOSFET maximum drain current, 360 - 361, 363

$I_{D(PK)}$, peak repetitive surge current, 230 - 233

$I_{D(SAT)}$, (See switch, FET.)

I_{DSS} , drain-source saturation current, 338 - 339

$I_{D(SURGE)}$, nonrepetitive surge current, 235 - 236

I_E , emitter current, 275

$I_{F(AV)}$, average forward current rating, 244 - 245

I_{FSM} , nonrepetitive surge current rating, 236

I_o , diode average forward current rating, 230

I_R , diode reverse current, 44, 54, 246

$I_{r(rms)}$, (*See* capacitor, ripple current.)
 $I_{r(rms - rating)}$, capacitor rms current rating, 241
 I_S , diode, reverse saturation current, 43
 I_S , FET,
 I_{SC} , short-circuit current, 69 - 70
 I_{SL} , (reverse) surface leakage current, 43
Ideal diode, 70 - 71
Ideal transformer, (*See* transformer, ideal.)
Ideal zener diode, 81 - 83
IEC (International Electrotechnical Commission), 119
Inert, 13
Insulated gate bipolar transistor (IGBT), 384
Intrinsic semiconductor, 13
Ionic bonding, 14 - 15
Isolation, transformers, 188

J - K

JEDEC, 243
JFET, 333 - 336
Knee voltage, 53
Knee-voltage diode model, 72 - 74

L

Laser, 131 - 133
Laser diode, 133 - 135, 137
Laser printer, 135 - 136
Latch, 380
LED (light-emitting diodes), 127 - 131
Light loading, 223

Limiter, (*See* clipper.)
Linear DC power supply, 172
Load, DC power supply, 173 - 174
Loudspeaker, 318 - 319

M

Majority carriers, 21
Metallic bonding, 6
Minority carriers, 21
Model, 70
Multisim, 57

N

N-channel DE-MOSFET, 358
N-channel E-MOSFET, 362
N-channel JFET, 334
Negative ion, 4
Negative temperature coefficient (negative tempco),
NEMA (National Electrical Manufacturers Association), 176
Neutral wire, 175 - 176
NPN BJT, 271
N-type semiconductor, 20
NTC thermistor, 119

O

Ohmic connection, 154 - 155
Ohmic region, (JFET), 338
OLED, 27
Organic semiconductors, 22

Oscillation, 248

P

Parameter, 287

Passivation, 358

P-channel DE-MOSFET, 358

P-channel E-MOSFET, 362

P-channel JFET, 335

Pentavalent, 13

Periodic table, partial, 12

Photoconductive cell, 131 - 141

Photoresistors, (*See* photoconductive cell.)

PIN photodiode, 141 – 146

Pinch-off, 338, 343 - 344

Pinch-off voltage, (JFET), 339

P-N junction, 27 – 29,

P-N junction, energy diagram, 34

P-N junction, unbiased drift and diffusion currents, 31 – 33

P-N junction forward bias, (*See* forward bias, diode)

P-N junction, forward-bias temperature effects, 113 – 115

P-N junction, frequency effects, 151 - 152

P-N junction, reverse-bias temperature effects, 118 - 119

PNP BJT, 271

Polarity protection, 122 - 123

PolySwitch, 121 - 125

Positive ion, 4

PTC thermistor, 121

Q

Q-point, diode, 70

Q-point, BJT, 288, 291, 298 – 305

Q-point, JFET, 365 – 367

Q-point, DE-MOSFET, 367 - 368

R

Radial leads, 218, 243

Recombination, 43

Resistance, dynamic, (*See* dynamic resistance.)

Resistance, static, (*See* static resistance.)

Reverse current-source model, 77

Reverse recovery time (t_{rr}), 153

Ripple current, (*See* capacitor, ripple current.)

Ripple factor (%r), 221 - 222

Ripple rejection, 249 - 250

Ripple voltage, 224 – 227

RoHS, restriction of hazardous substances, 244

Root Mean Square (RMS) value, 178, 184 – 186

RMS values, various waveforms, 186

S

Saturation, BJT circuit, (*See* Switch, BJT.)
Saturation region, BJT, 288 – 289, 292
Saturation region, FET, 339
Saturation, FET circuit, (*See* Switch, FET.)
Semiconductors, 11-12
Schottky diode, 154 - 155
Shockley diode equation, 66 - 67
Signals, (analog versus digital), 315
Silicon, 11 - 12
Silicon dioxide (SiO₂), 11, 278, 358
Solar cells, 146 – 148
Solar module, 149 - 150
Solid-state devices, 2
Source terminal, FET, 334 - 335
Static resistance, 83 - 85
Superposition theorem, 372
Surface leakage current, I_{SL} , (*See* I_{SL} .)
Switch, BJT, 311
Switch, FET, 368 - 369
Switching power supply, 171 - 173

T

Tetravalent, 11
Thermal runaway, 286
Thermistors, 119 - 125
Thevenin's theorem, 92 – 95
Three-terminal voltage regulator, 248 - 250

Three-wire power distribution system, 175 - 176

Transducer, 4

Transformers, 186 – 190, 192

Transformer, ideal, 189

Transformer secondary current rating, 241 - 242

Transformer, voltage regulation, 190 - 191

Transistor convention, 286, 348

Trivalent, 13

t_{rr} , (*See* reverse recovery time)

U

Unipolar device, (*See* Schottky diode.)

USB, Universal Serial Bus, 173 - 174

V

V_{CC} , collector DC bias supply, 273

V_{DC}

V_{DC} , diode blocking voltage,

V_{dc} , peak rectified voltage, 196

$V_{dc(min)}$, minimum instantaneous voltage across the filter capacitor, 220

$V_{DROPOUT}$, 249

V_{EE} , emitter DC bias supply, 273

V_F , diode maximum instantaneous forward voltage, 246

$V_{GS(OFF)}$, JFET, 342

$V_{GS(th)}$, E-MOSFET, 364

V_K , (*See* knee voltage)

V_m , peak voltage, 196

V_{OC} , open-circuit voltage, 69 – 70

$V_{r(p-p)}$, peak-to-peak ripple voltage, 222, 224 - 227

V_{RM} , peak reverse voltage, 197

V_{RRM} , diode peak repetitive reverse voltage rating, 197

V_{RMS} , rms value of the diode reverse voltage rating, 245

$V_{r(rms)}$, RMS value of the ripple voltage, 222

Valence, 4

Valence energy band, 8

Varactor diode, 156 - 157

Varistors, 4, 12, 125 - 127

V-I characteristic curve, diode, 52 - 53

Voltage, DC level, 183

Voltage, instantaneous, 307, 374

Voltage, total instantaneous, 307, 374

W

WVDC, Working Voltage Direct Current, 217

X - Y

Z

Zener/avalanche diodes, 80 - 81

Zener breakdown, 77 - 79

Zener dynamic resistance model, 88 - 91

Zener effect, (*See* Zener breakdown)